Semiconductors: Underpinning Power Electronics

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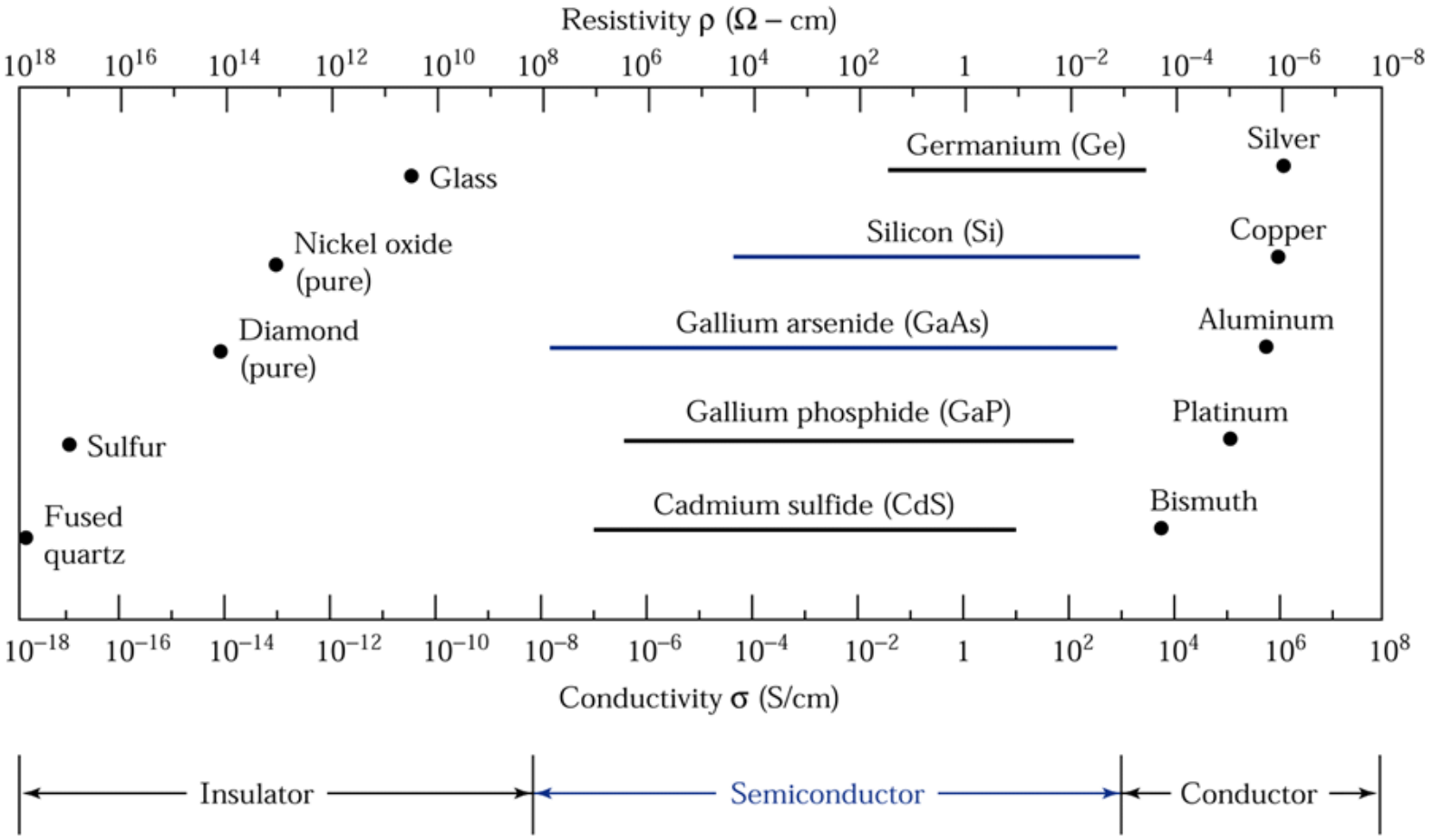
Outline:

- Semiconductors 101
- MOSFETs
- A global perspective of semiconductors
- Beyond silicon?

Semiconductor Properties: doping

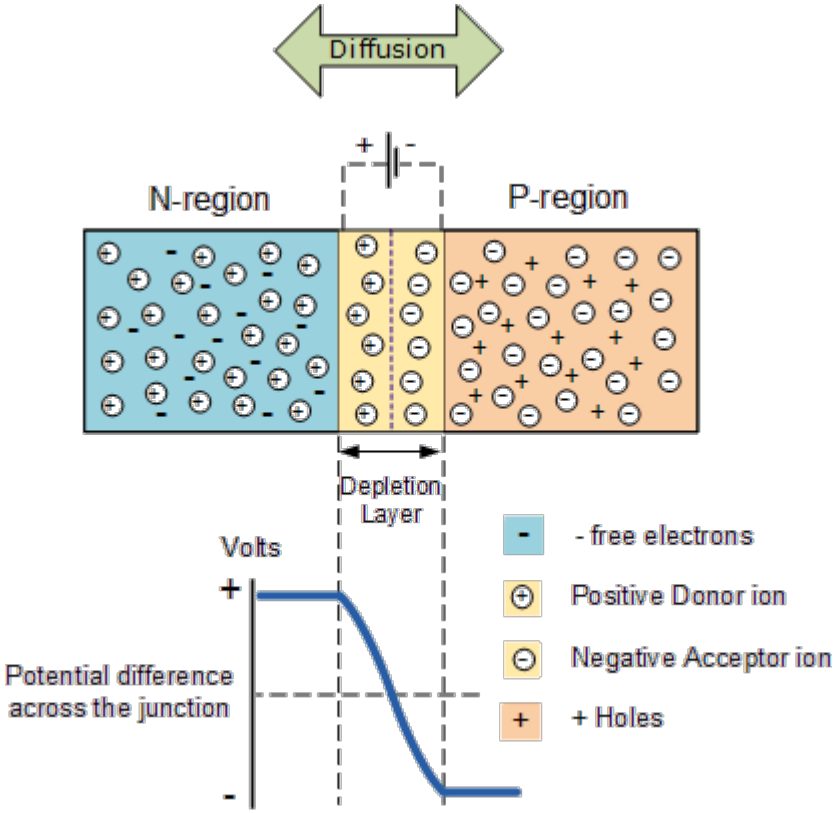
- ~ppm doping → engineer conductivity

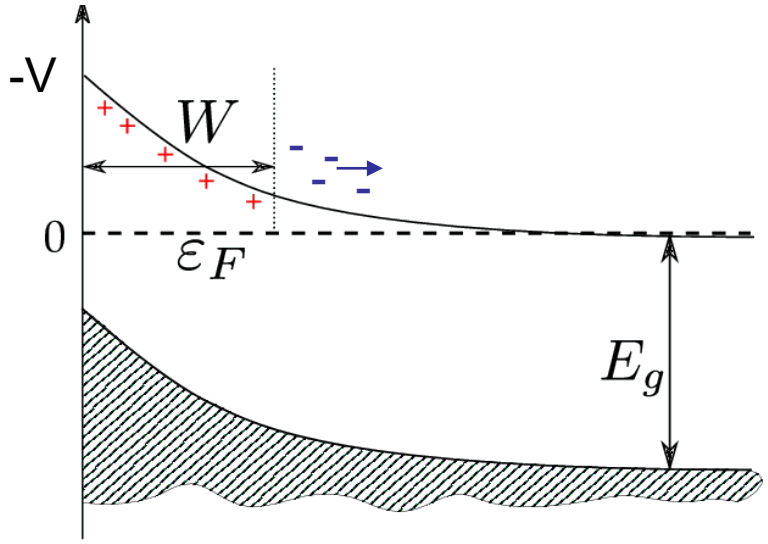


➢ Current can be flow of -ve charge (N-type) or +ve (P-type)

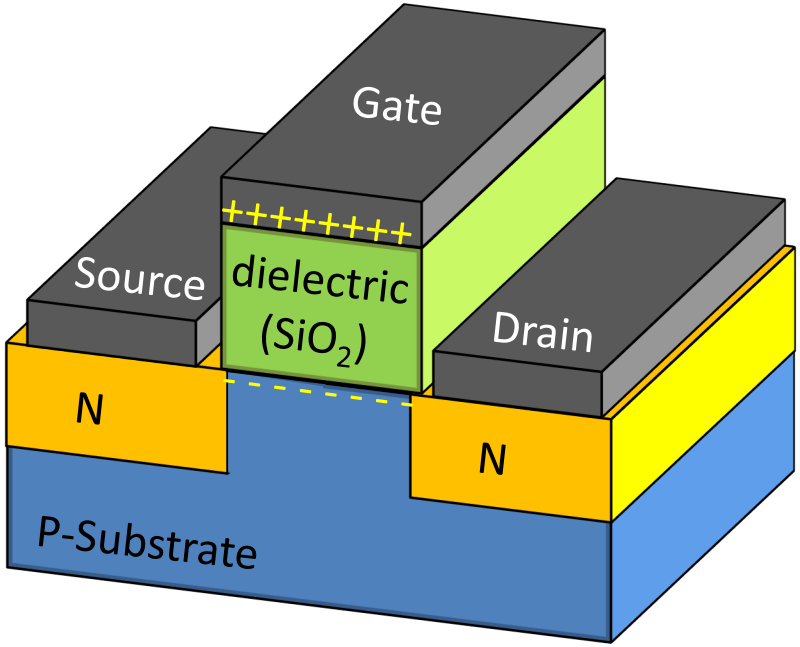
Semiconductor Properties: voltage

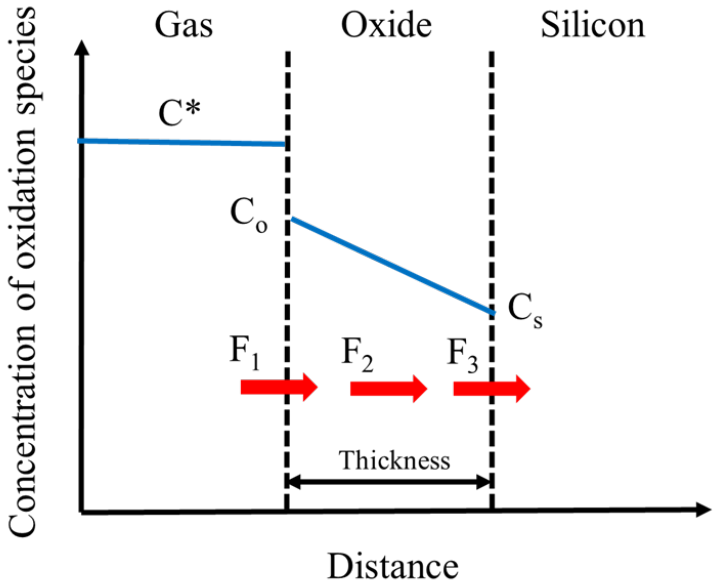
- voltage → engineer conductivity
- voltage can be internal (pn junction) or applied externally

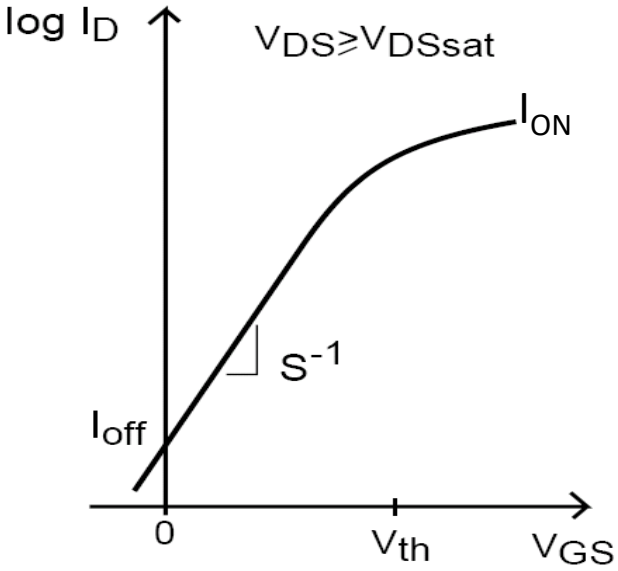




MOSFET



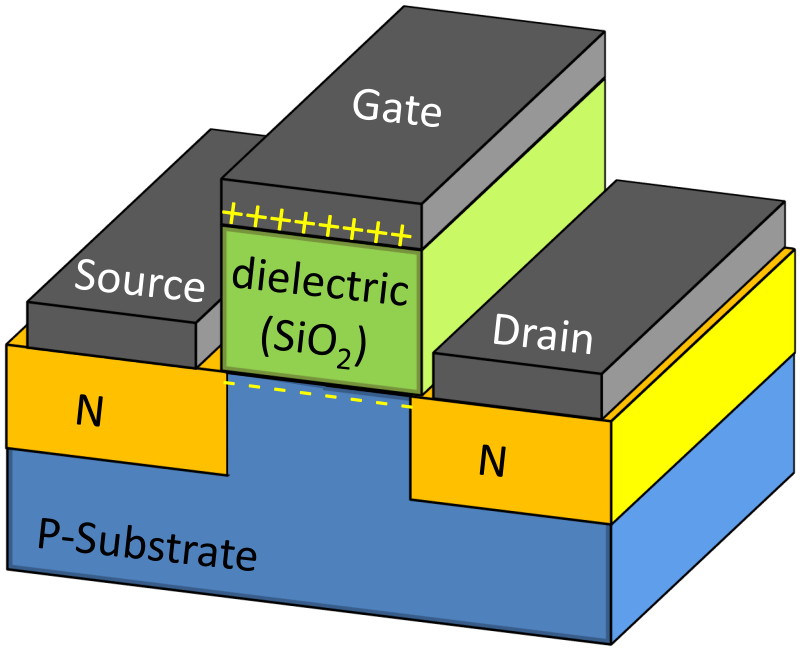


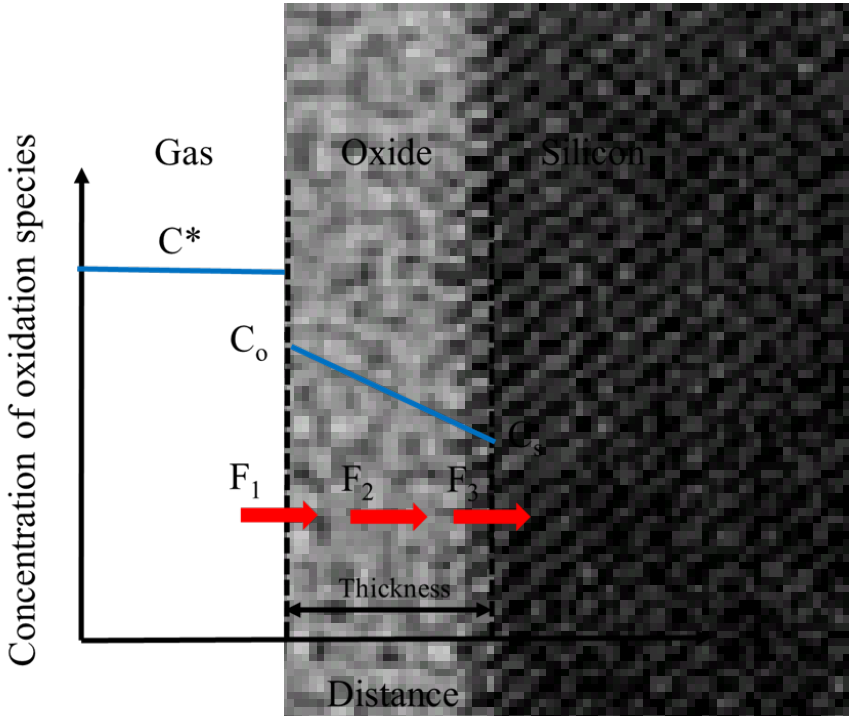


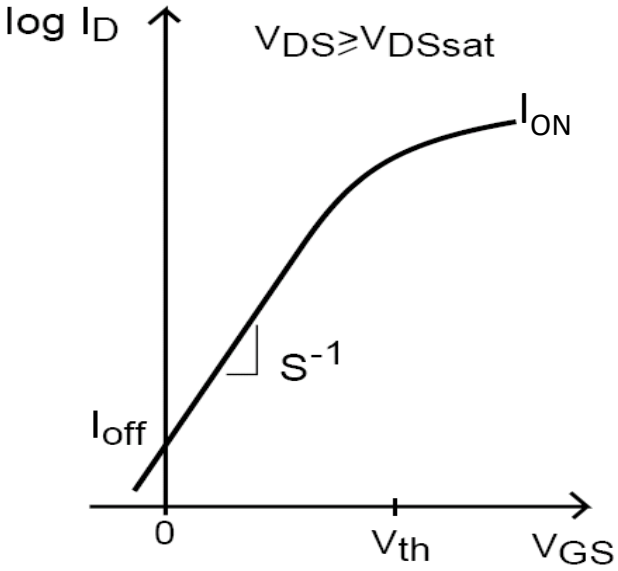
Deal-Grove Model (1965)

- oxygen arrives at oxide surface;
- crosses oxide film to Si;
- arrives at Si surface and reacts: $Si + O_2 \rightarrow SiO_2$
- SiO_2 is great insulator
- Si/SiO_2 monolayer, low defects

MOSFET







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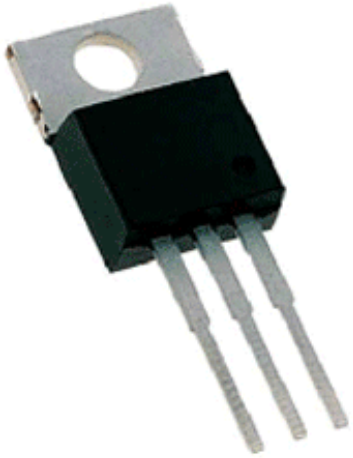
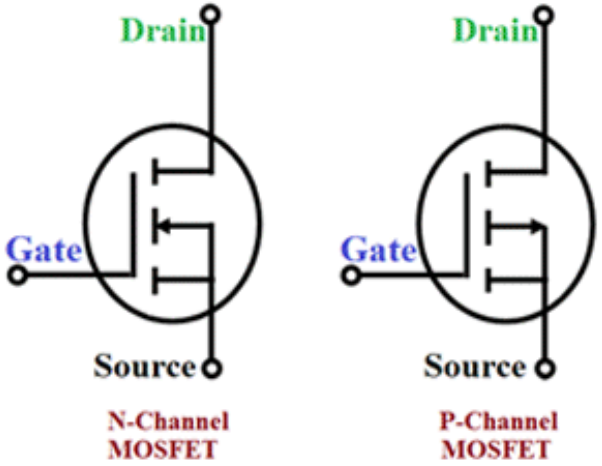
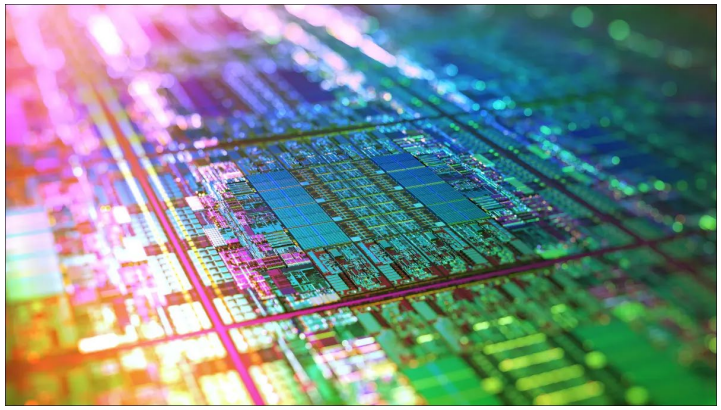
MOSFET

1959 Mohamed Atalla, Dawon Kahng







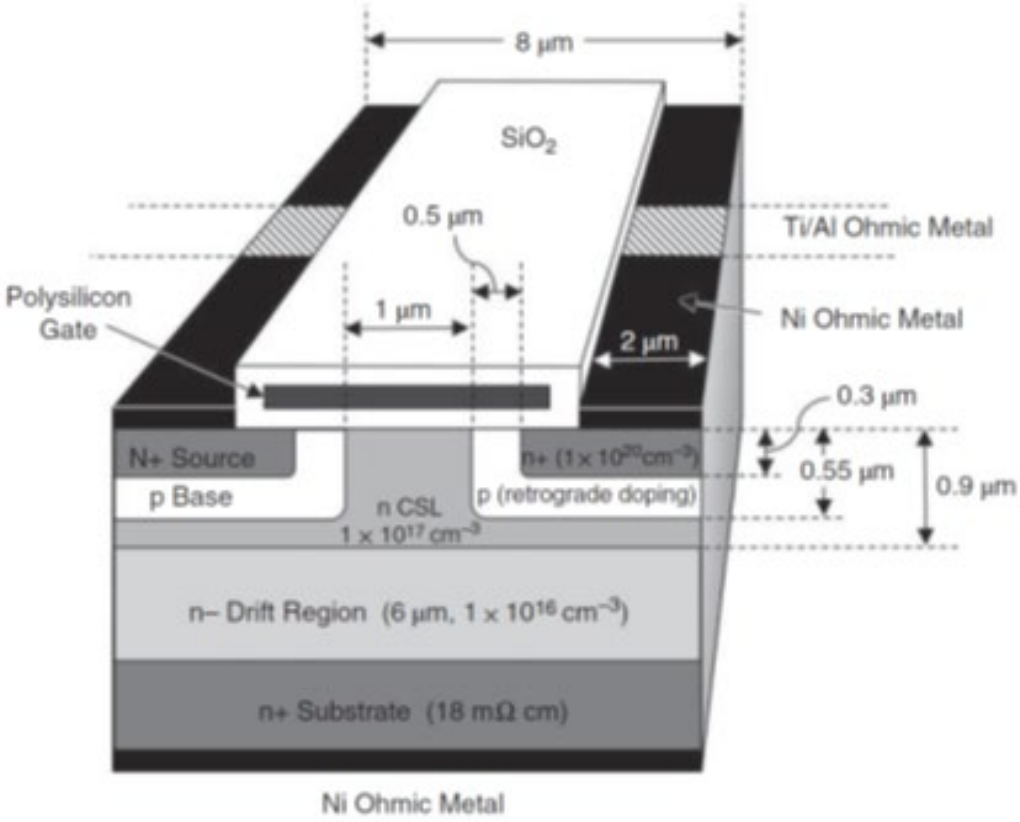
Circuit symbol

100V Power MOSFET

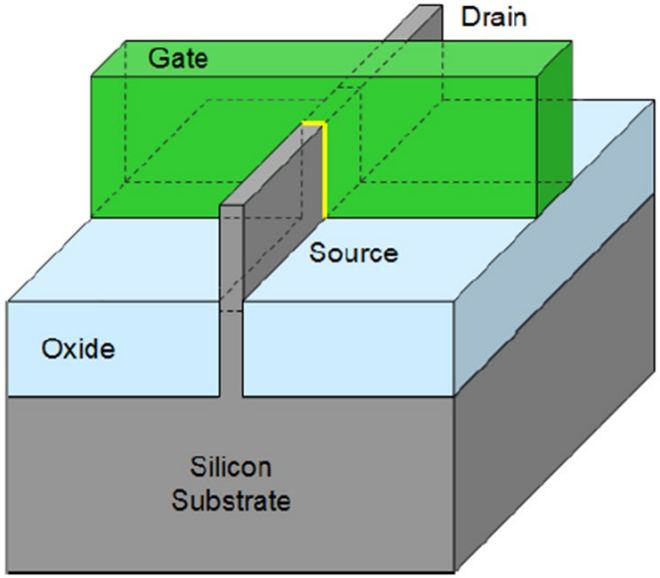
Billions of 4 nm
MOSFETs on microchip

MOSFET

2024 MOSFETs in production



Power MOSFET



4 nm MOSFET on microchip

(image: Kimoto&Cooper)

1965
Moore's Law

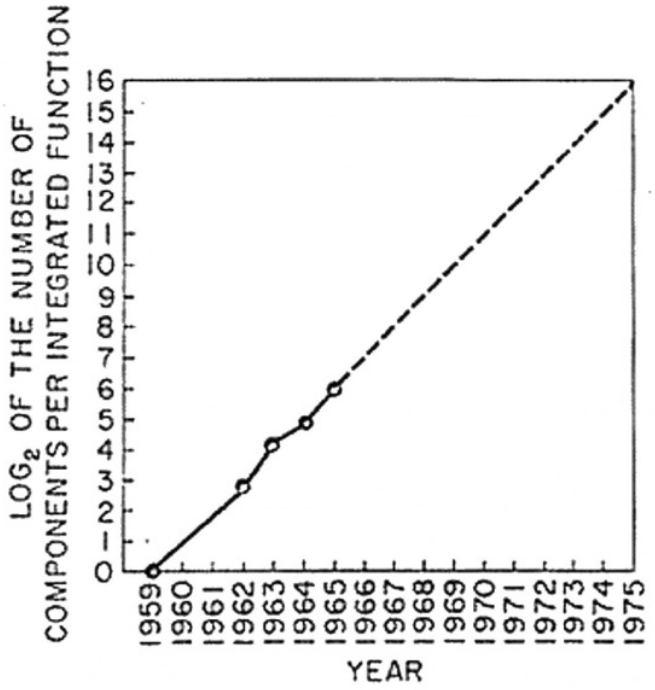


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

2^6 = 64 components
on single chip by 1965

2^{16} = 65,536 components
on single chip by 1975

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

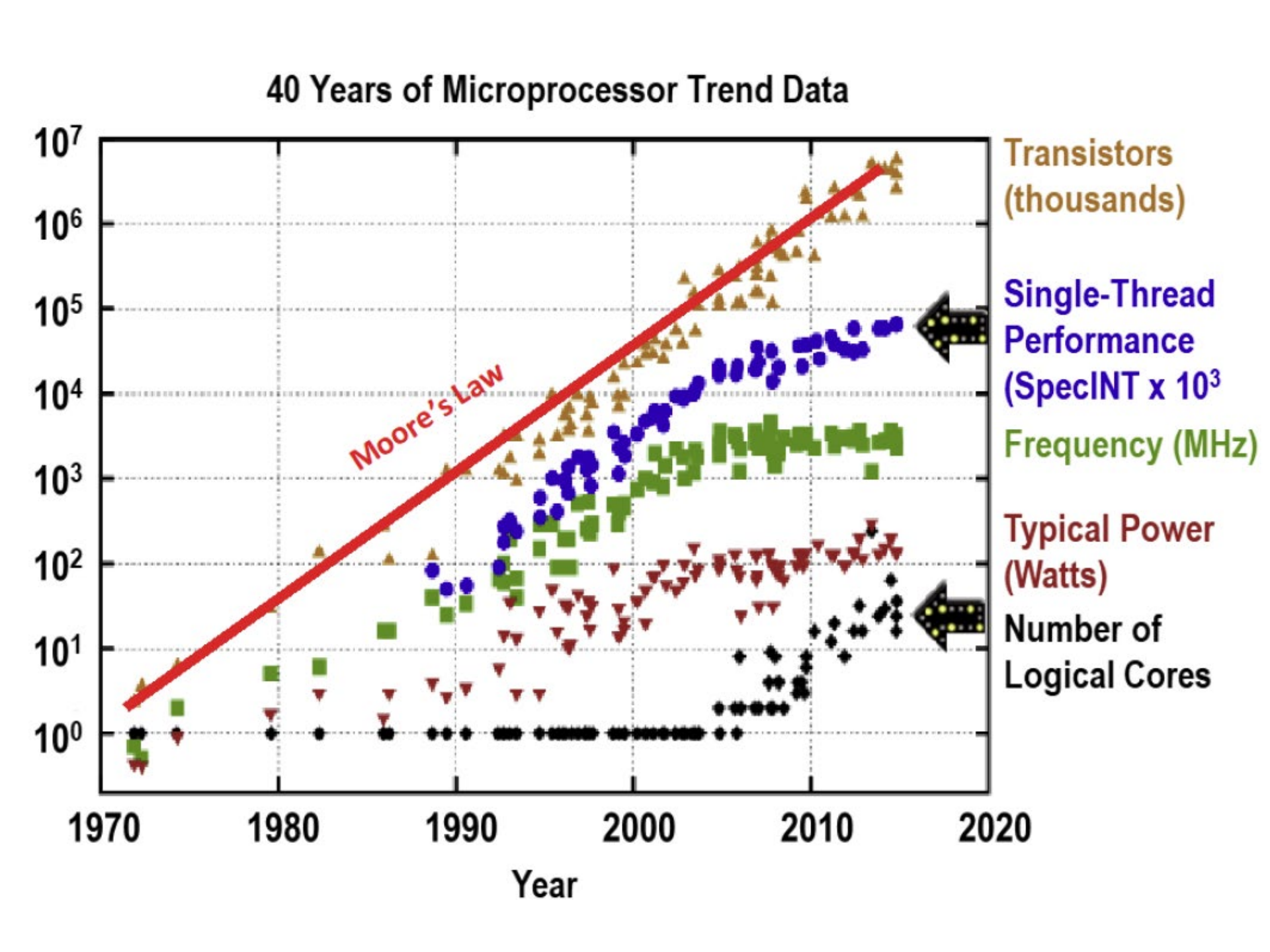
Both approaches have worked well and are being used in equipment today.

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Year	Processor Name	Transistor Count	Process Technology (μm)
1971	4004	2,300	10
1972	8008	3,500	10
1974	8080	6,000	6
1976	8085	6,500	3
1978	8086	29,000	3
1982	80286	134,000	1.5
1985	80386	275,000	1.5
1989	Intel486	1,200,000	1
1993	Pentium	3,100,000	0.8
1995	Pentium Pro	5,500,000	0.6
1997	Pentium II	7,500,000	0.35
1999	Pentium III	9,500,000	0.25
2000	Pentium IV	42,000,000	0.18
2002	Pentium IV (Northwood)	55,000,000	0.13
2004	Pentium IV (Prescott)	169,000,000	0.09
2005		230,000,000	0.09
2006	Core 2	291,000,000	0.065

~ 6,000 components
on processor chip by 1974

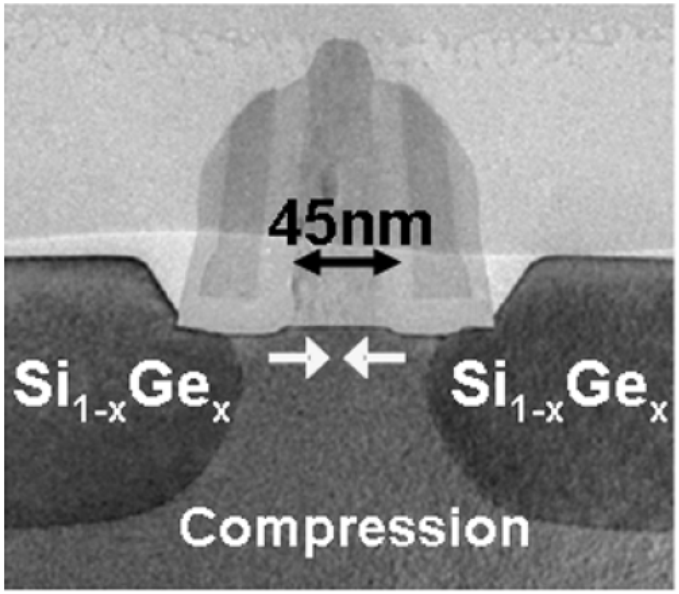

40 Years of Microprocessor Trend Data
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
Moore's Law
Transistors (thousands)
Single-Thread Performance (SpecINT x 10^3
Frequency (MHz)
Typical Power (Watts)
Number of Logical Cores
1970
1980
1990
2000
2010
2020
Year

More of Moore 1970 - 2002

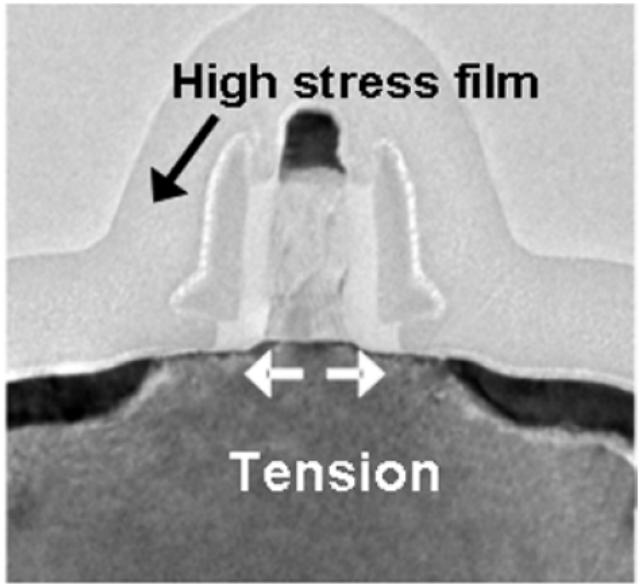
- **Classic Silicon Scaling**
  - Reduce dimensions, constant E field → electrostatic integrity (gate control)
  - Modifications for short channel effects
  - stopped at 130 nm

90 nm Technology Generation – 2003 (Intel)

Equivalent scaling 1: Strained silicon



pMOSFET



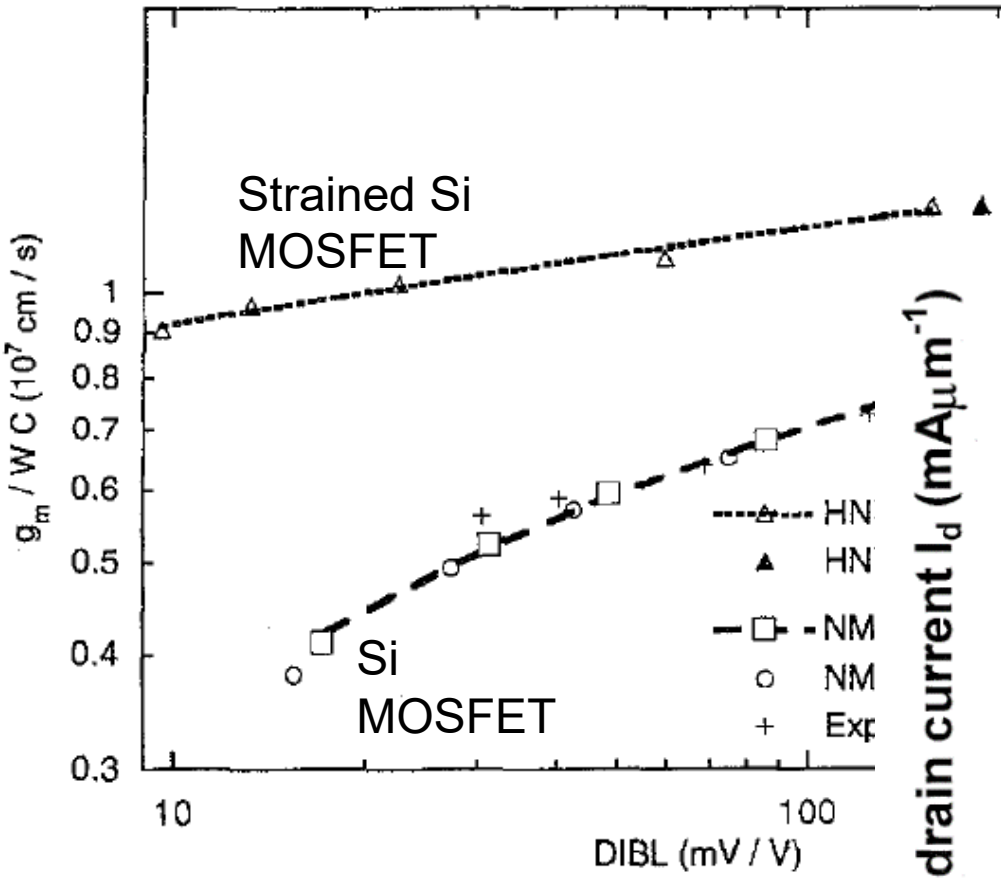
nMOSFET

Major change in technology:

- strained silicon: improved speed with no extra power and no loss of electrostatic integrity (gate control)

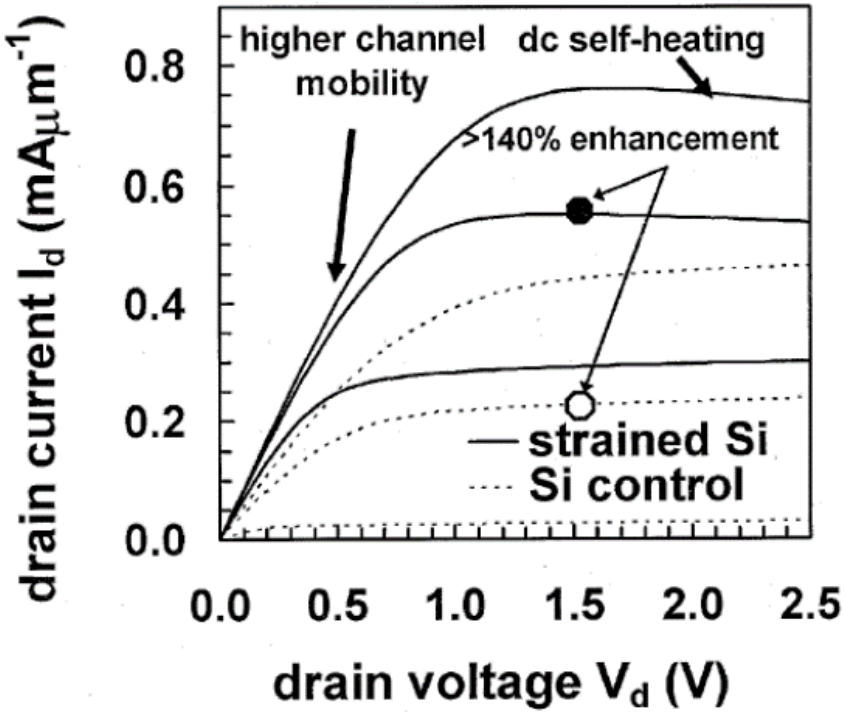
Deep Submicron CMOS Based on Silicon Germanium Technology

A. G. O'Neill and D. A. Antoniadis, *Fellow, IEEE*

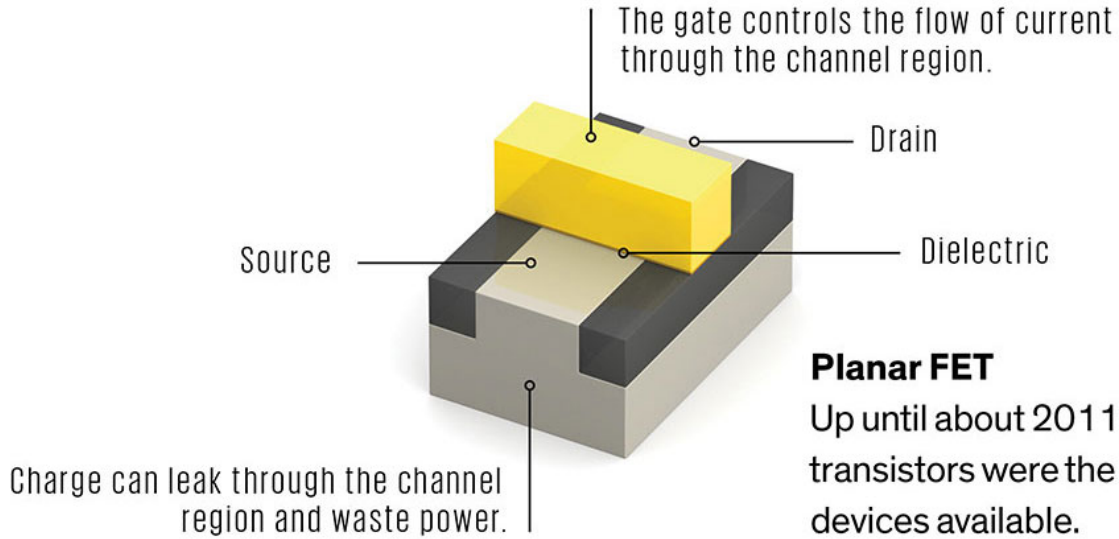


0.1 μm NMOSFET's and 67 GHz for 0.1 μm PMOSFET's. Elsewhere, Yan *et al.* [3] report a f_t of 116 GHz for 0.1 μm and 89 GHz for 0.15 μm NMOSFET's and at the same laboratory Lee *et al.* [4] demonstrated 0.1 μm PMOSFET's operating at

een device speed, described
annel length as an implicit
width and C_{ox} is the gate
his relationship was found
ers such as oxide thickness.

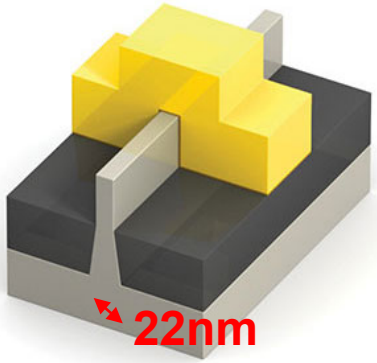


Electrostatic integrity (gate control)



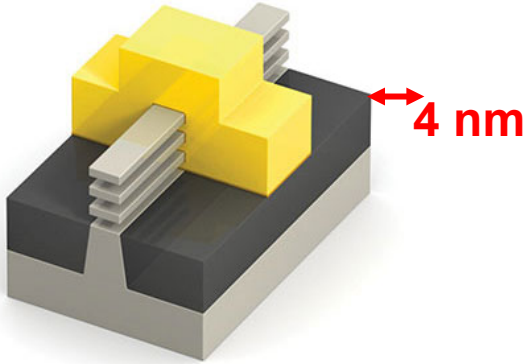
Planar FET

Up until about 2011, planar transistors were the best devices available.



FinFET

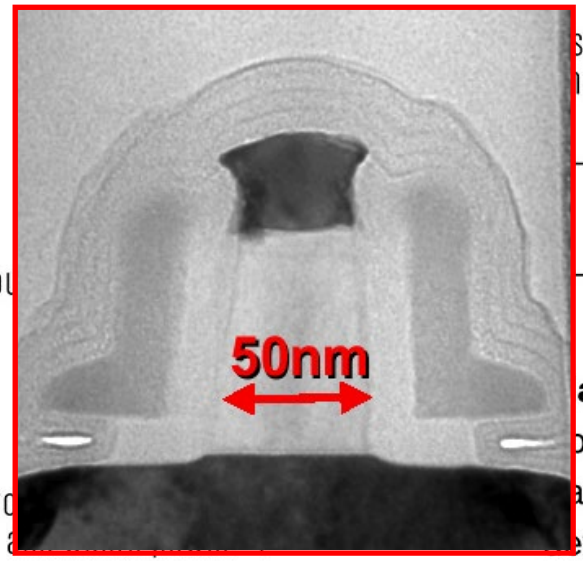
Surrounding the channel region on three sides with the gate gives better control and prevents current leakage.



Stacked nanosheet FET

The gate completely surrounds the channel regions to give even better control than the FinFET.

Electrostatic integrity (gate control)



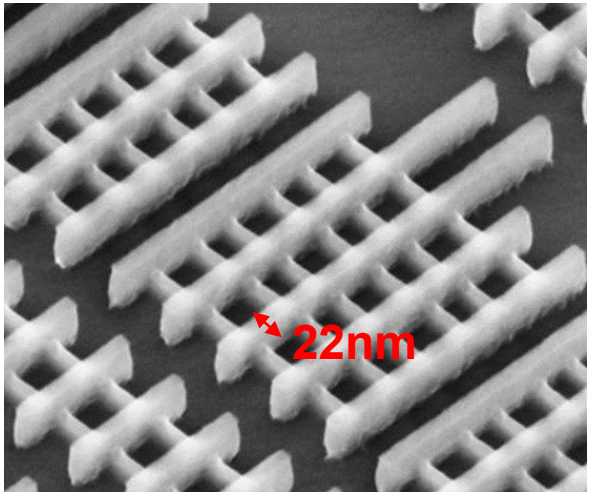
s the flow of current
nnel region.

– Drain

Sou — Dielectric

Charge can leak thro
region a

anar FET
o until about 2011, planar
ansistors were the best
evices available.



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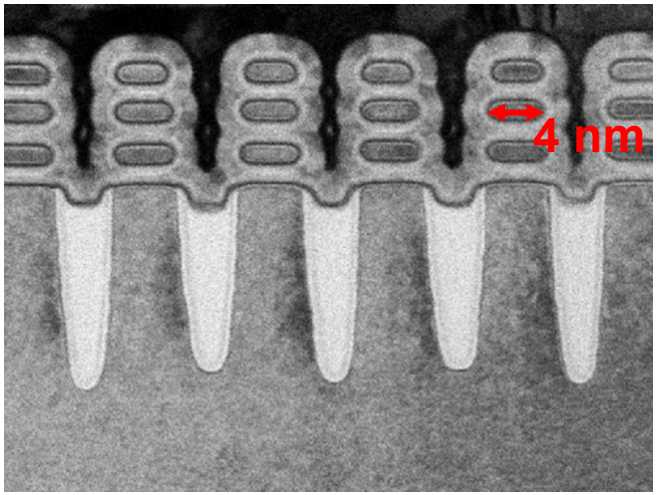
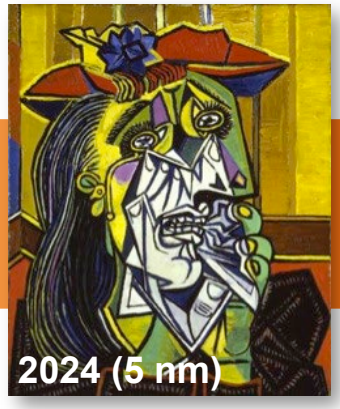


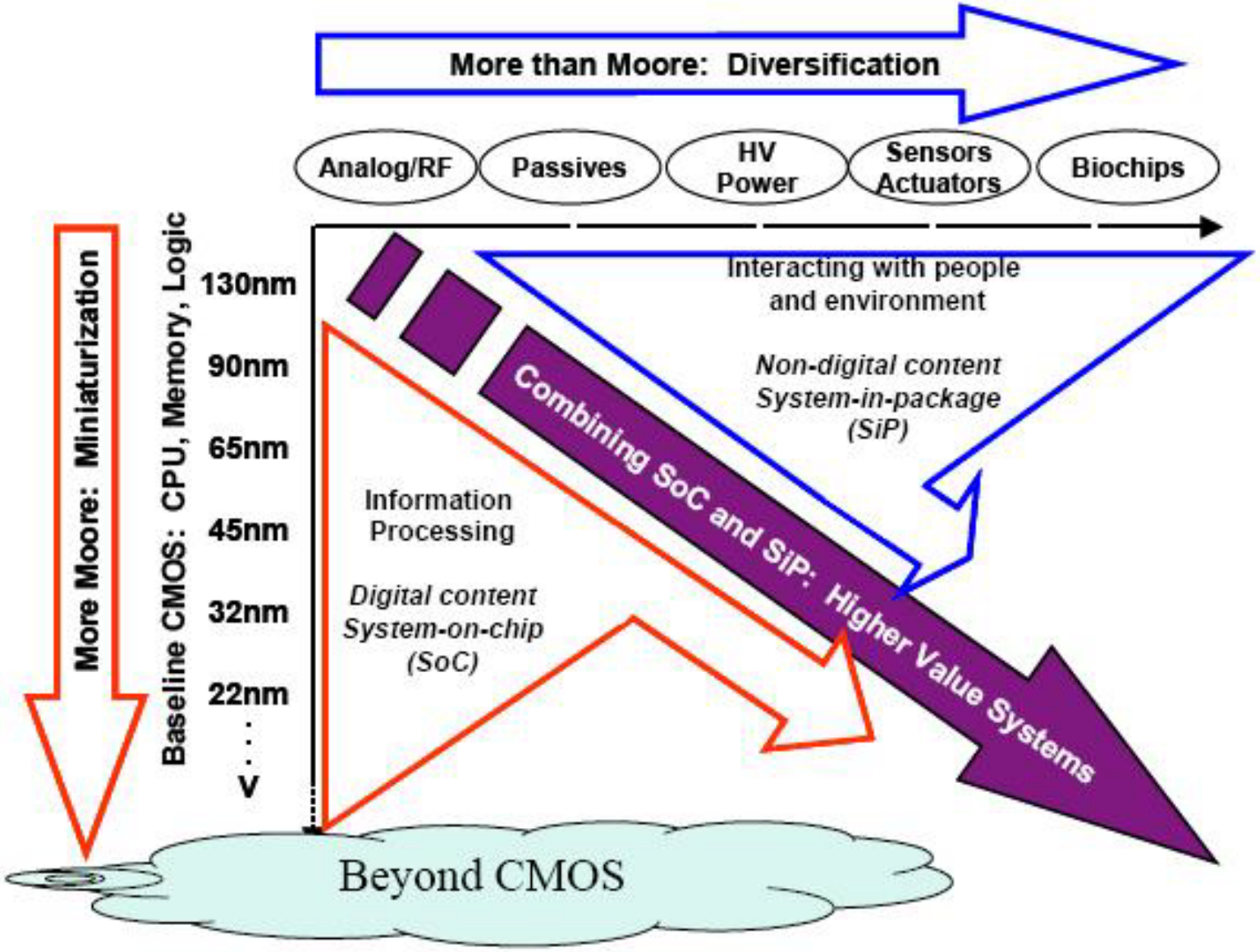
channel regions to give even better control than the FinFET.

More of Moore



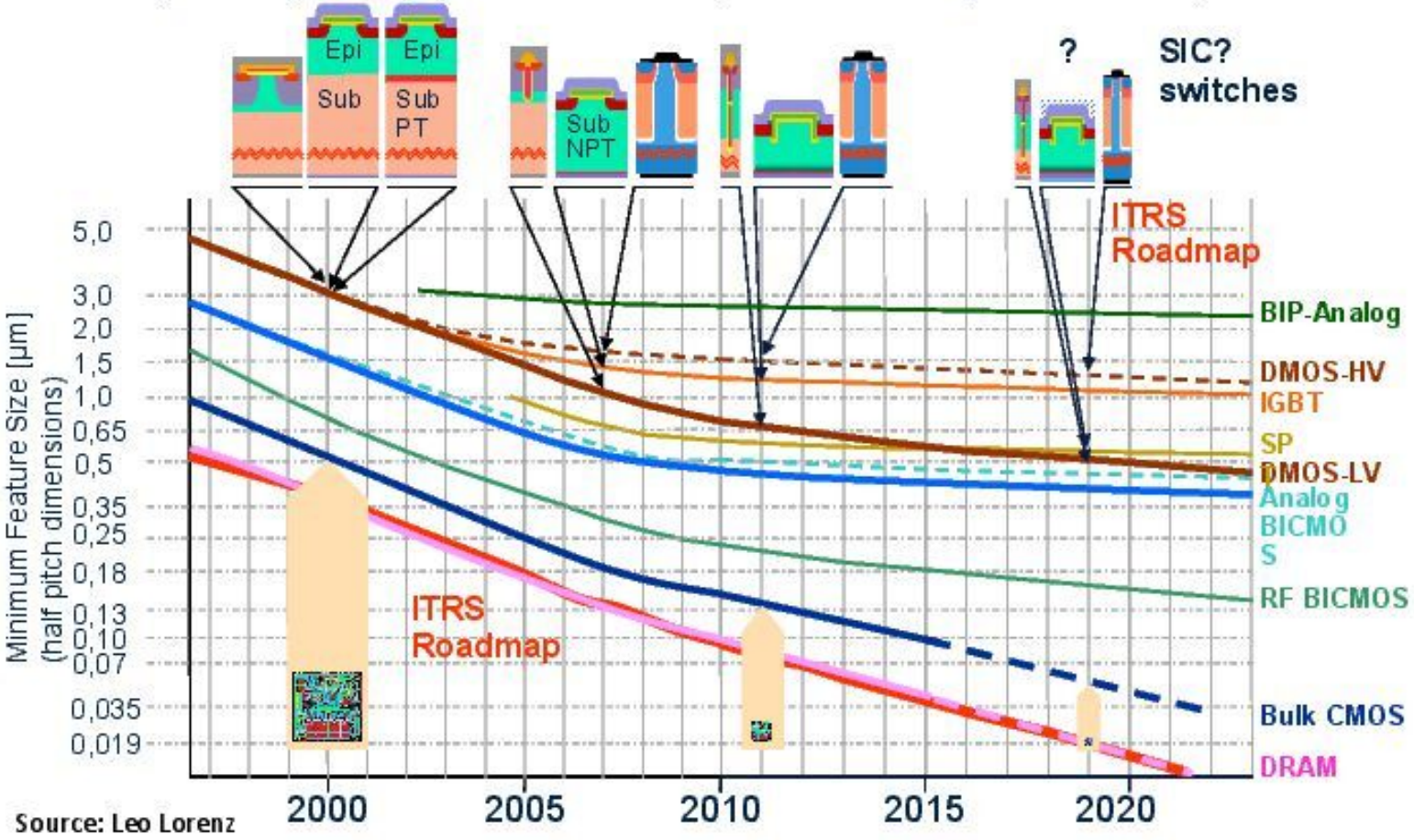
- **Classic Silicon Scaling**
  - Reduce dimensions, constant E field
  - Modifications for short channel effects
  - stopped at 130nm
- **Equivalent scaling**
  - Reduce dimensions less
  - Strain, hi-k dielectric, finFET, nanosheet
- **System innovations**
  - Multi-core
  - Mixed technology platforms

More than Moore



Technologies for an Increasing Number of Applications hit Scalability Limits

Only Memory and high performance microprocessors strictly follow Moor's predictions



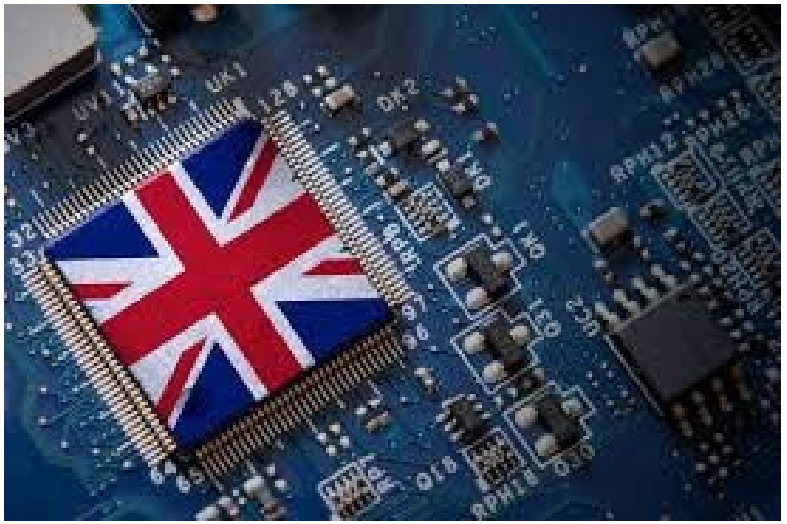
Source: Leo Lorenz

A global perspective of semiconductors

- The global semiconductor industry is one of the largest in the world
  - 1990's: 80% of manufacturing was in the US or Europe – including UK.
  - 2020: revenue from semiconductors was 0.5% of global GDP
- 2021: 1.1 trillion microchips produced
  - 125 microchips per person on Earth
  - Global microchip market was $614 Billion
  - Bigger than global software market of $569 Billion
  - Global power semiconductor market was $39.5 Billion
  - Around 80% of the market is silicon
  - Around 0.5% of the market is from UK
- 2024:
  - Smartphone logic > 20 billion = 2×10^{10} MOSFETs
  - Data storage 128 GB (£5) = $128 \times 8 \times 10^9 = 10^{12}$ floating gate MOSFETs
  - Taiwan (TSMC) and Korea (Samsung) account for 80% of processor and memory chips. Chip production is not globally distributed
  - Wafer fabs in UK:
    - < 20k gates = 2×10^4 of logic, clock speed 10Mhz

A UK perspective of semiconductors

- Semefab. ASICS 3 to 20V analogue and digital content - typically <20k gates of logic, clock speed 10Mhz.
- Diodes. Discrete, logic gates, power management, auto
- Dynex Semiconductor. Power devices (IGBT, bipolar, thyristor) and power assemblies
- Newport Wafer Fab is the UK's largest chipmaking facility. In 2024 it was sold to Vishay for compound semiconductors
- Clas-SiC SiC foundry for power semiconductors
- Pragmatic Flexible substrates



A UK perspective of semiconductors

- Government: Dept of Science, Innovation & Technology identifies semiconductors as one of five critical technologies
- UK declared investments in semiconductors:
  - 2022 £0.1 billion to "replicate silicon valley" (Levelling Up)
  - 2024: £1Bn announced for semiconductors (over 10 yrs)

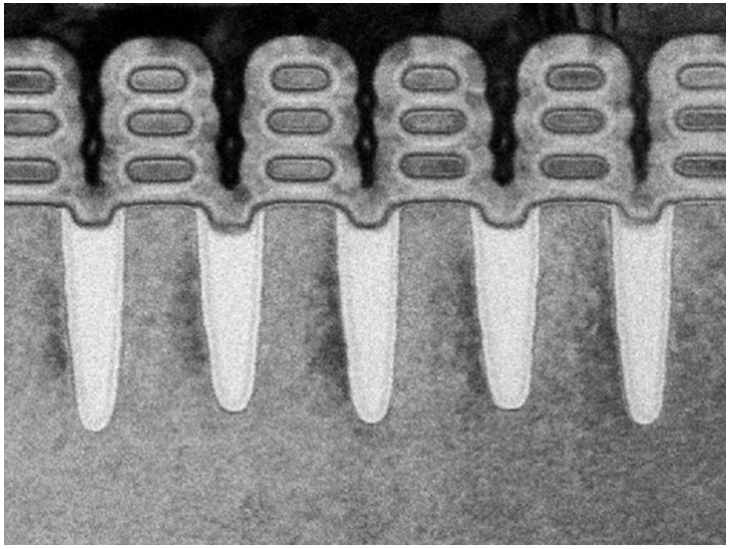
	Semiconductor investment ($Bn)	GDP ($Tn)	Semiconductor Investment (/%GDP)
UK	1.27	3.1	0.04
USA	53	25.4	0.21
EU	216	15.8	1.37
China	150	17.96	0.84
S Korea	470	1.7	27.65
Japan	26.7	4.2	0.64
India	15	3.4	0.44
UK	**7**	**3.1**	**0.23**

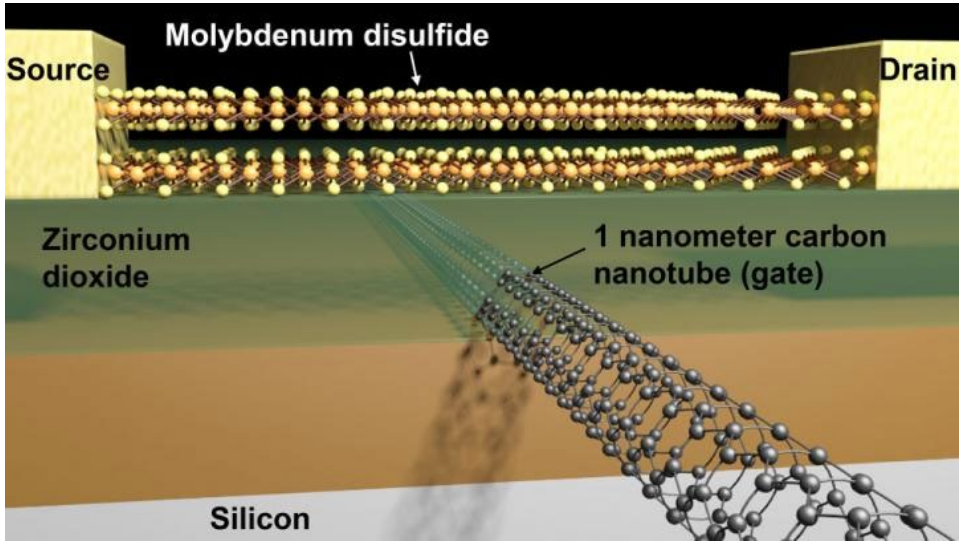
A future UK semiconductor industry

- UK needs a semiconductor industry for security and economic reasons
- We have some world class power semiconductor manufacturing, design and compound semiconductors.
  This is necessary but not sufficient for UK
- **We need: < 50nm CMOS foundry & mixed technology packaging**
  for more than Moore, automotive, 5G, and Internet of Things (IoT) devices that rely on devices like power management, analog and display driver integrated circuits (ICs), MOSFETs, microcontroller units (MCUs) and sensors.
- A 200mm fab with 50,000 wafers/month can cost as much as $1 billion, including construction and equipment.
- Getting a state-of-the-art >300mm fab is possible in ~10 years, but with fab cost $10-20 billion.
- UK investing at least $7 billion would be consistent with comparators, based on investment as % of GDP
- New mindset: maximise our gains, not minimise our losses

- ***UK can have a semiconductor industry but needs:***
  realistic investment of £billions + commercial incentives + university strengths
- ***Will our new government act?***

Beyond silicon?





- **Silicon / CMOS is *really* good!**
  - Si is abundant, an element
  - SiO_2 is stable oxide giving excellent isolation (> 3nm)
  - Si/SiO_2 interface is monolayer, low defects
  - MOSFET $I_{ON} / I_{OFF} > 10^6$
  - CMOS only consumes power when switching states
  - Globally, Si industry is mature AND innovative

Beyond silicon? – Wide bandgap semiconductors

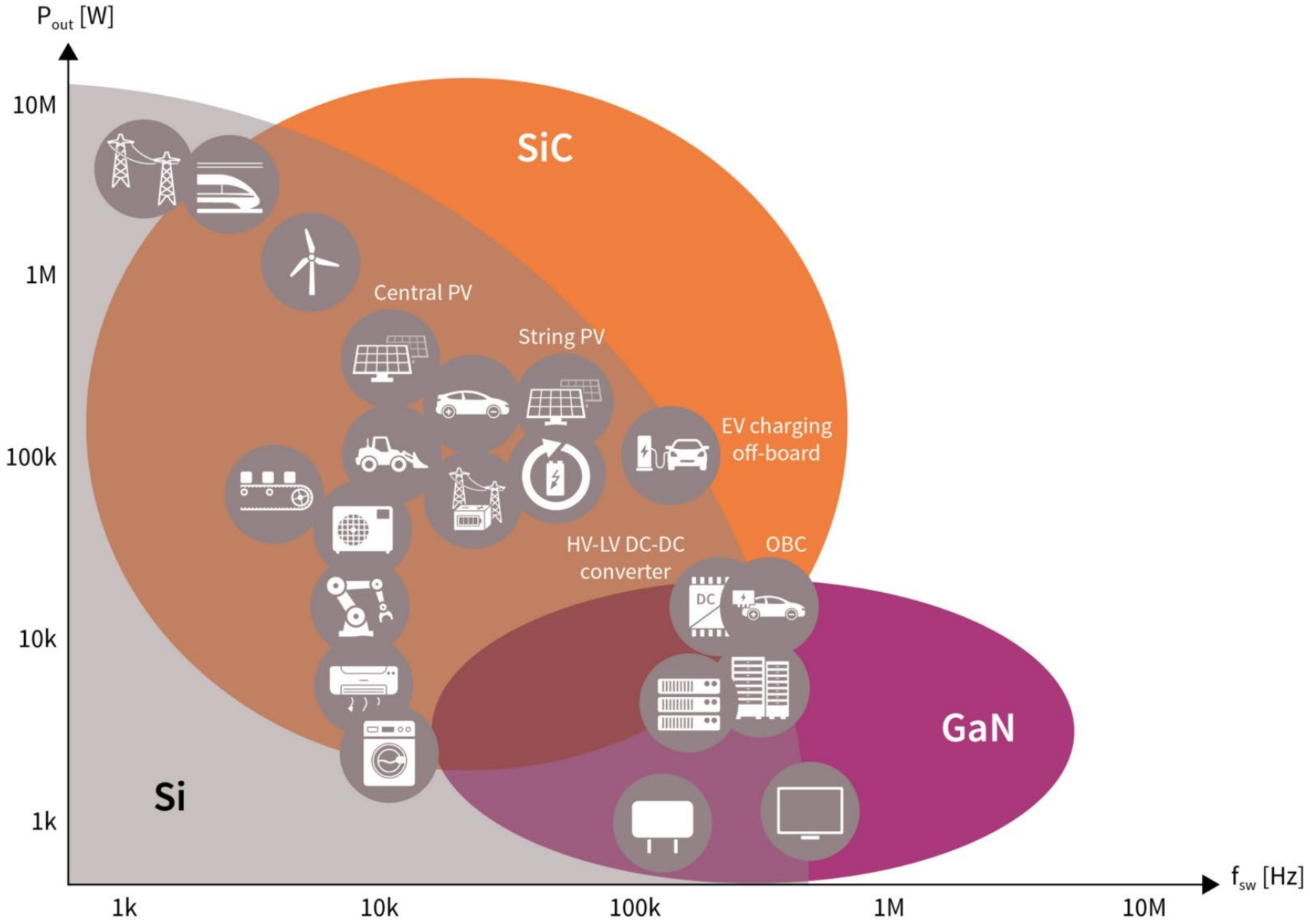
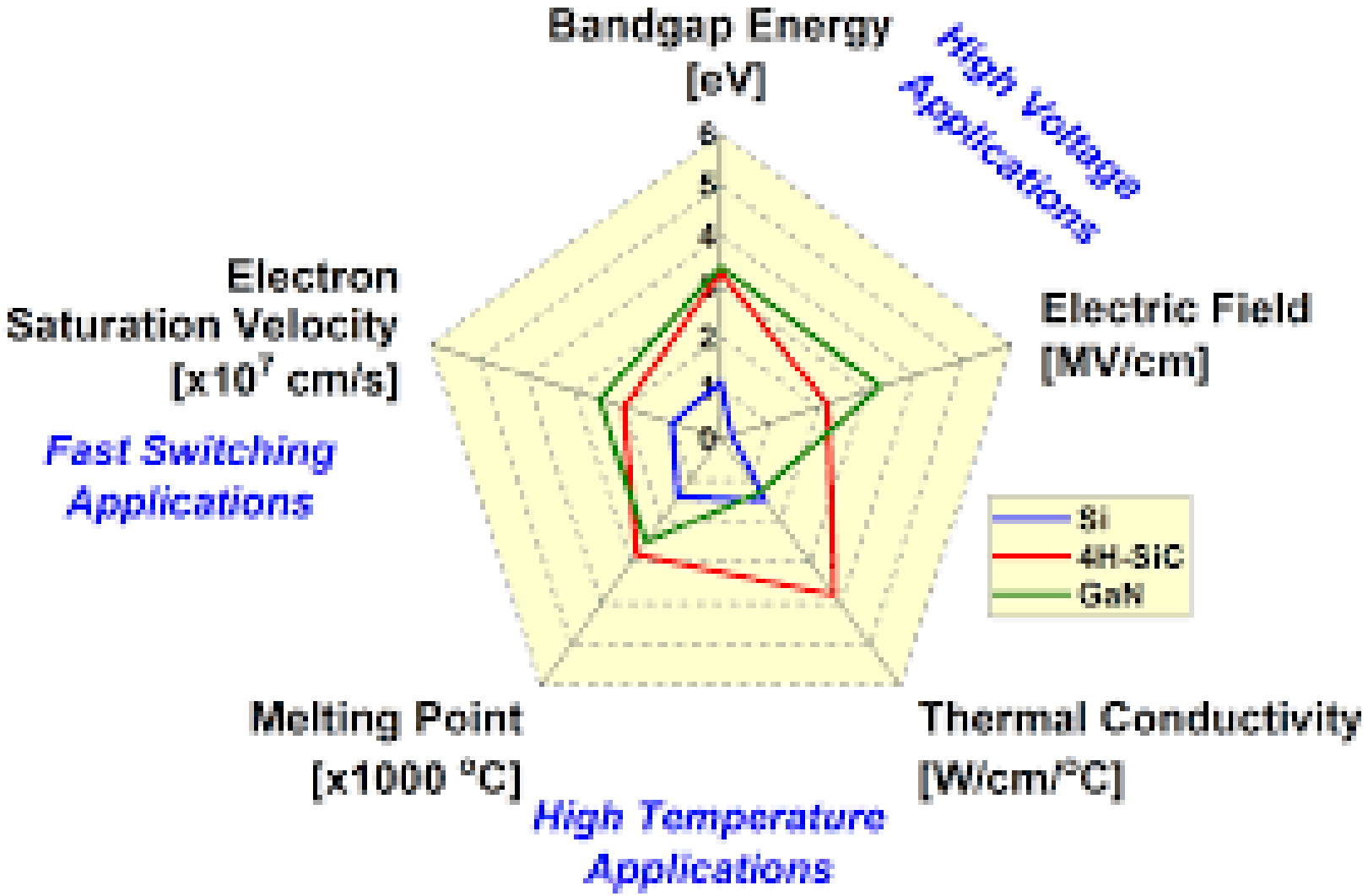


Image: Infineon

Beyond silicon? – Wide bandgap semiconductors

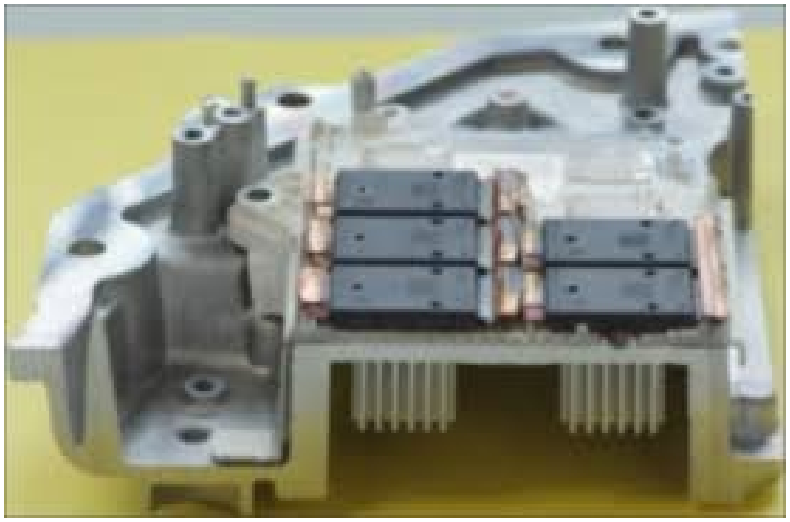


- **The truth, but not the whole truth..**

image: MDPI

Beyond silicon? – Silicon Carbide MOSFETs

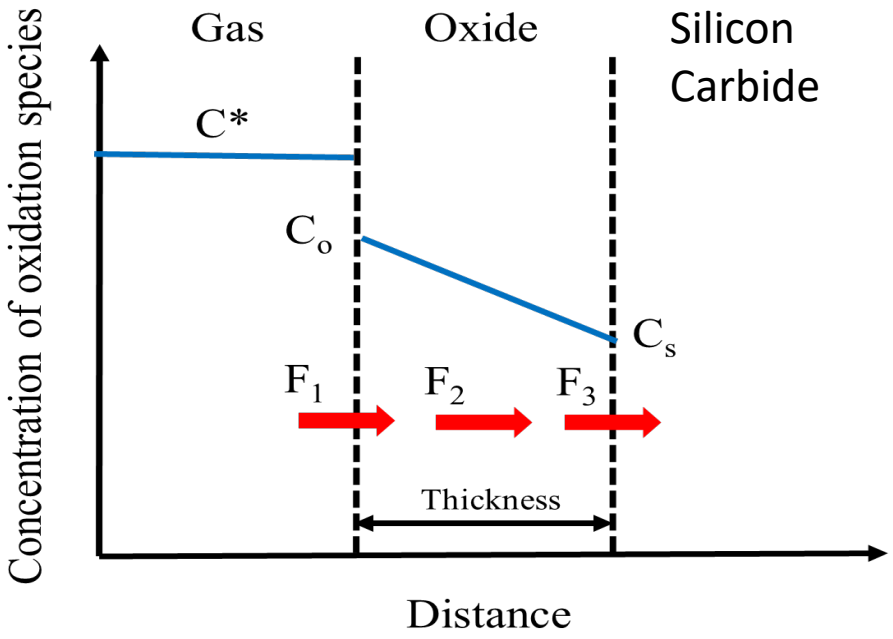
2017 Tesla Model 3 – wot, no engine?



SiC Inverter (STMicroelectronics)

- **Silicon Carbide ~~is~~ will be *really* good!**
  - Si and C are abundant
  - Material quality needs to improve
  - SiC MOS technology lies decades behind Si
  - Si/SiO_2 interface is possible, but with defects
  - So MOSFETs are possible but gate engineering needed…

Gen1: SiC oxidation



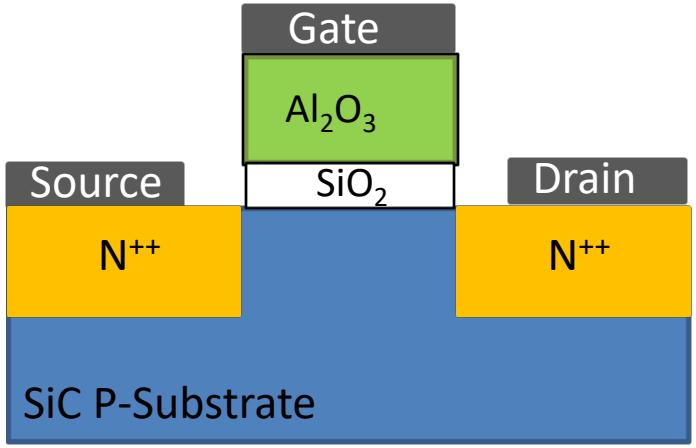
- Some residual C may out-diffuse through the oxide film

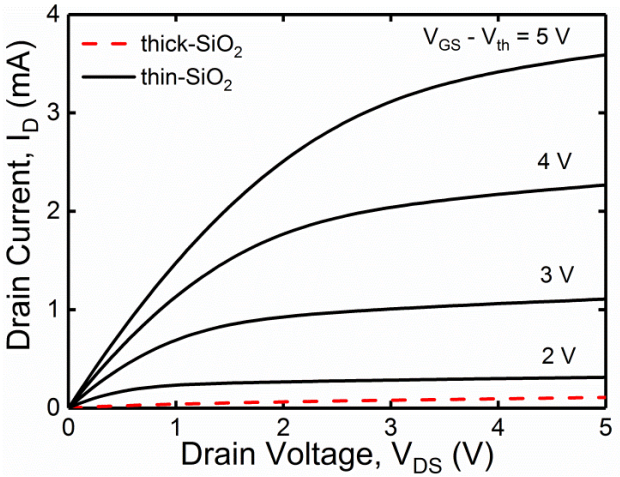
  $SiC + 3/2\ O_2 \rightarrow SiO_2 + CO$

  $SiC + 2\ O_2 \rightarrow SiO_2 + CO_2$
- Some residual C may remain,

  $SiC + O_2 \rightarrow SiO_2 + C$
- thin grown SiO_2 → Fewer defects

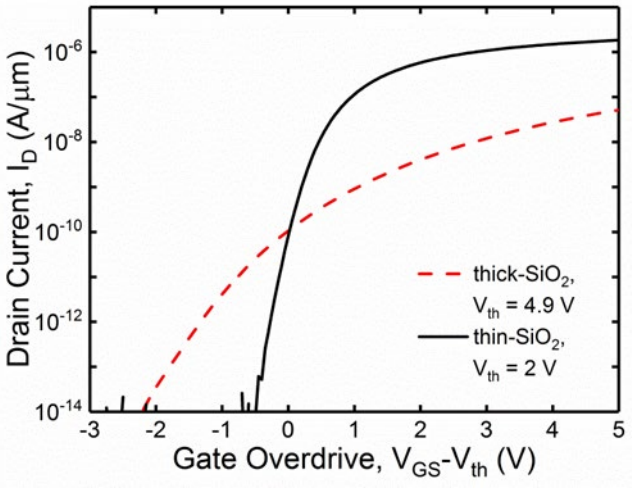
Re-engineering the Gate Stack: ICSCRM 2017





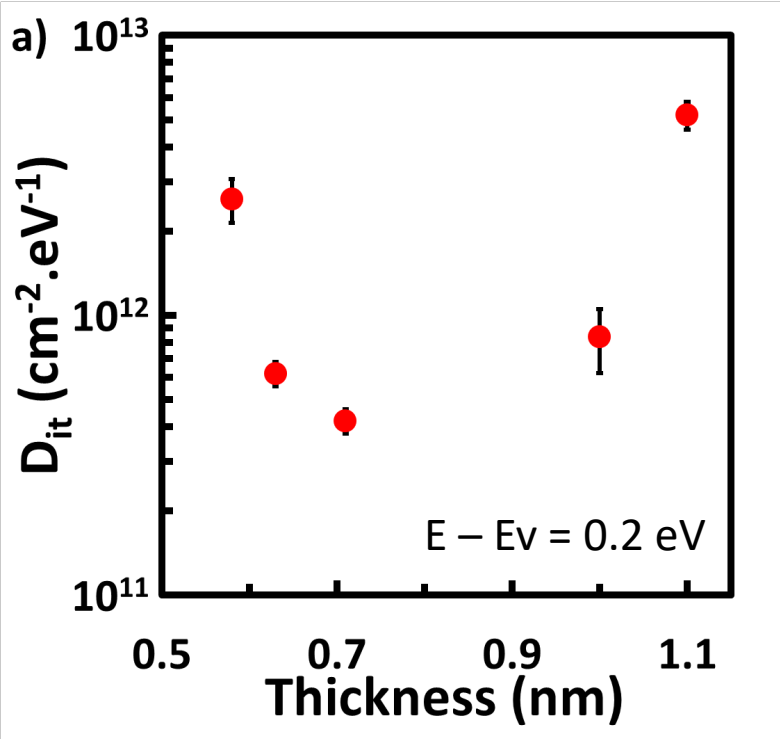
- Ultra-thin (0.7 nm) oxidation
  → low Temperature (<600 °C) , short time (<3 min)
- High field effect mobility, μ_{FE} = 154 $cm^2/V.s$
- Steep subthreshold slope S = 127 mV/dec
- Good temperature stability 25 - 300 ˚C
- Low interface trap density,

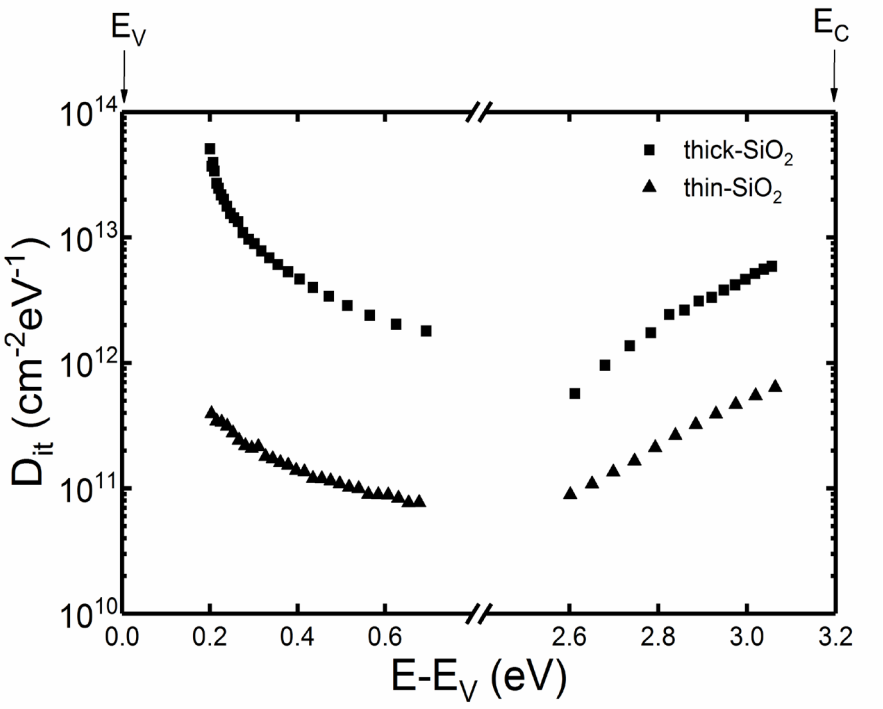
$$6\times10^{11} < D_{IT} < 5\times10^{10}\ cm^{-2}eV^{-1}$$



- *Urresti et al ICSCRM 2017 (MSF Vol 924, p494, 2018)*
- *Arith et al IEEE Electron Dev Lett Vol39, p564, 2018*
- *Urresti et al IEEE Trans Electron Dev Vol66, p1710, 2019*

4H-SiC MOS Capacitor

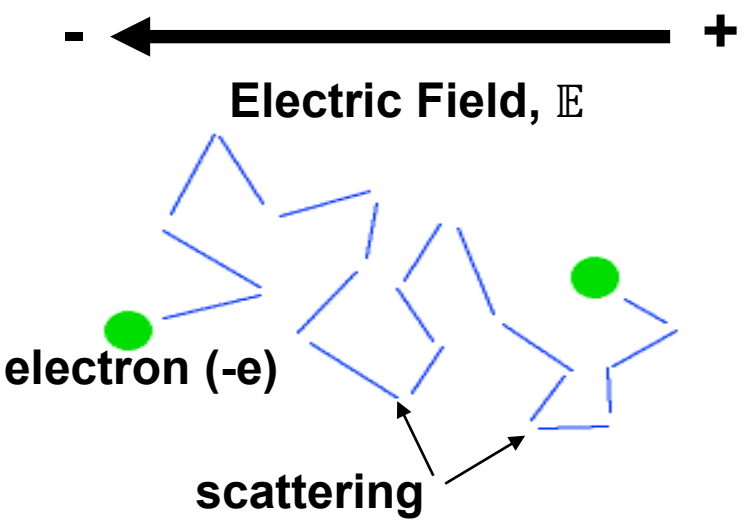




- D_{it} passes through a minimum corresponding to 0.7 nm SiO_2 layer
- minimum D_{it} occurs for a thermal budget of 600 °C for 3 min
- corresponds with 0.7-nm growth of SiO_2

- MOS capacitors have the same gate stack as MOSFETs
- For thin SiO_2
  $D_{it} = 6\times10^{11} - 5\times10^{10}\ cm^{-2}eV^{-1}$

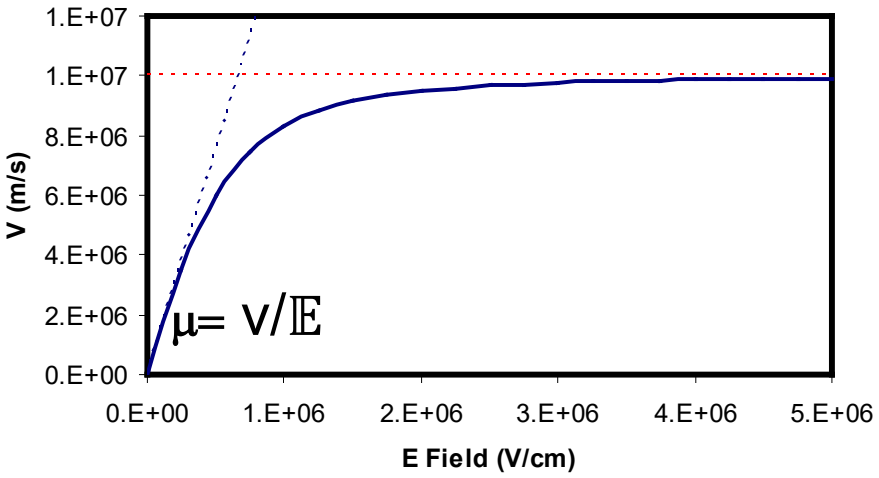
Semiconductors 101: carrier mobility μ



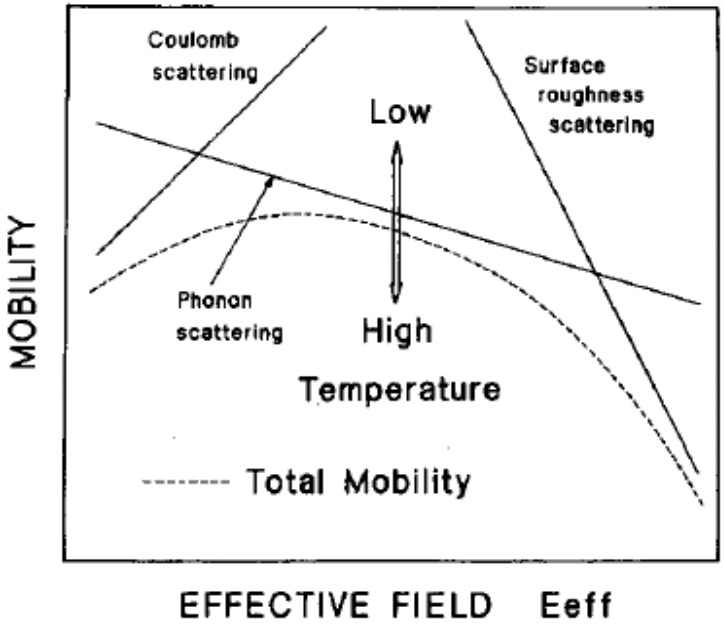
electron drifts in electric field:

- Coulomb scattering (from charge)
- Phonon scattering (from crystal)
- Surface scattering (from SiO_2/Si)

velocity-field relation $v = \mu \mathbb{E}$

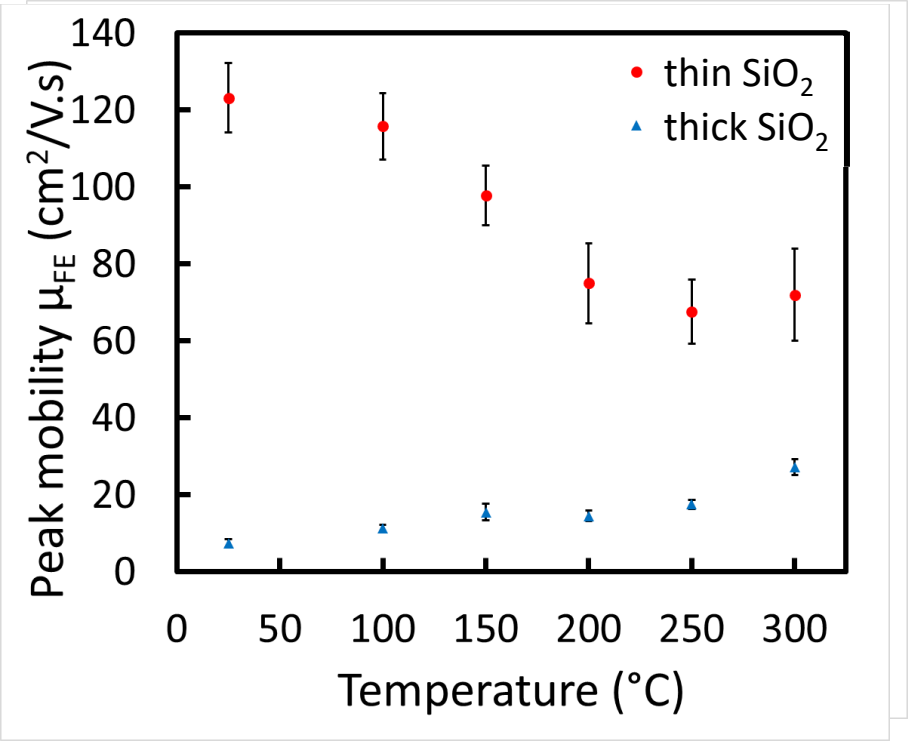


- Universal mobility



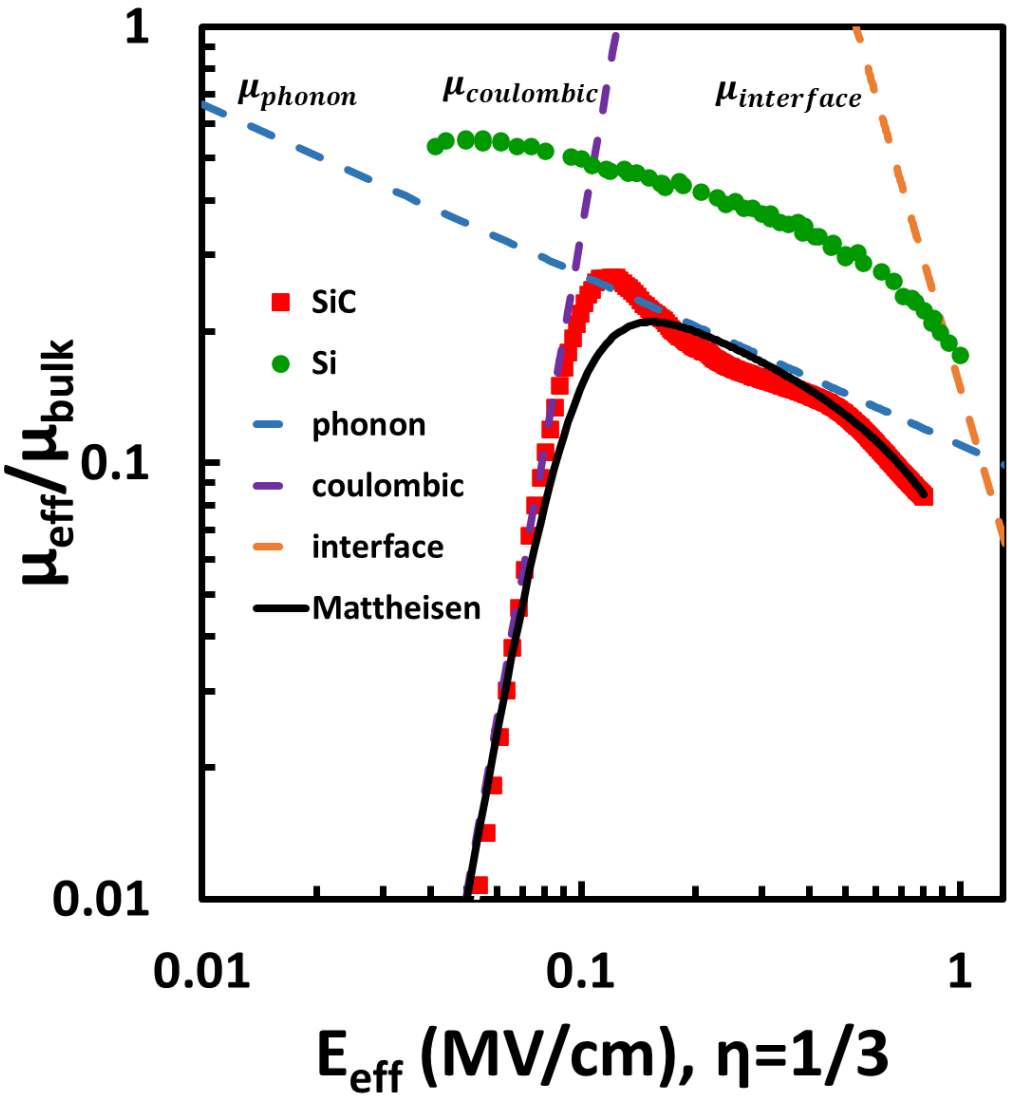
Experimental: mobility $\mu_{FE}(T)$

- μ_{FE} reduces by 40% at T=300°C
  - sustains high mobility
- μ_{FE} ↓ as T ↑ for thin SiO_2
  - phonon scattering
  - greater lattice vibration as T ↑
- μ_{FE} ↑ as T ↑ for thick SiO_2
  - coulomic scattering
  - interaction time reduces as T ↑



- The temperature dependence of mobility for the thin-SiO_2 MOSFETs shows that it is dominated by phonon scattering
  - fewer C related defects reduces coulombic scattering
  - gives rise to its high mobility .

Experimental: SiC versus Si mobility



- Si, SiC bulk mobilities are similar:
  Si μ_{bulk} = 1450 cm2/Vs
  4H-SiC μ_{bulk} = 900 cm2/Vs
- Universal mobility plot reveals:
  - SiC devices ~50% of Si devices
  - contributions to scattering:

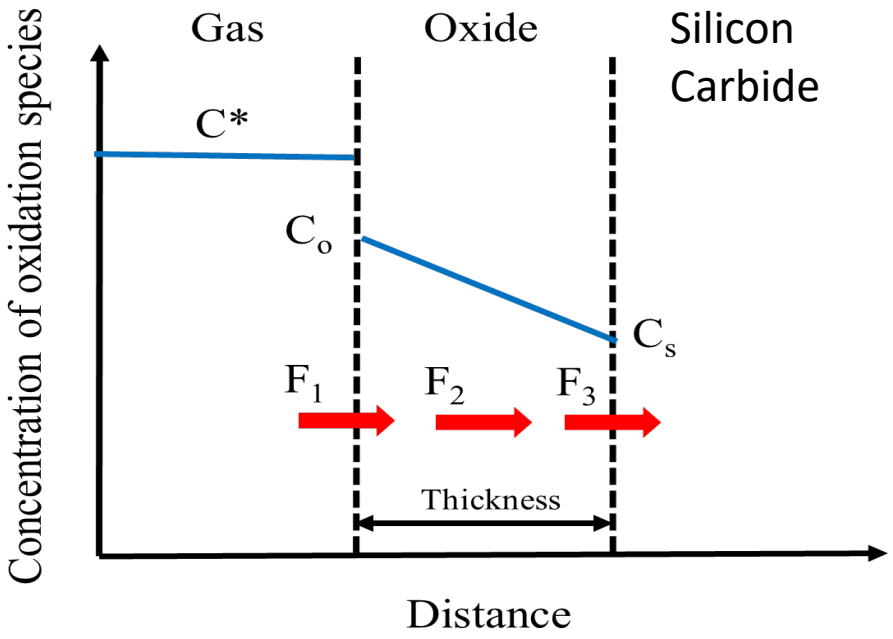
$$\frac{1}{\mu} = \frac{1}{\mu_{coulombic}} + \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{interface}}$$

  - Fitting to the data gives:

$\mu=Ae^B$	η=1/3		η=1/2	
	A	B	A	B
coulombic	$3x10^7$	5	$5x10^5$	3.4
phonon	99	-0.39	117	-0.39
interface	135	-3	360	-2

$$E_{eff} = \frac{q}{\varepsilon_0 \varepsilon_{SiC}} (N_{depl} + \eta N_s)$$

Gen2: SiC oxidation

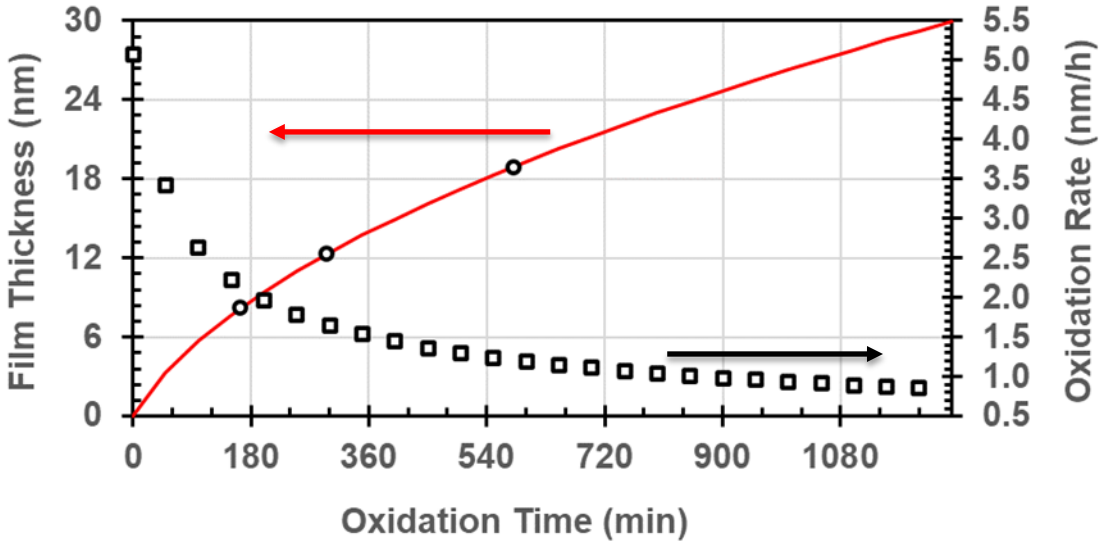


- Some residual C may out-diffuse through the oxide film

  $SiC + 3/2\ O_2 \rightarrow SiO_2 + CO$

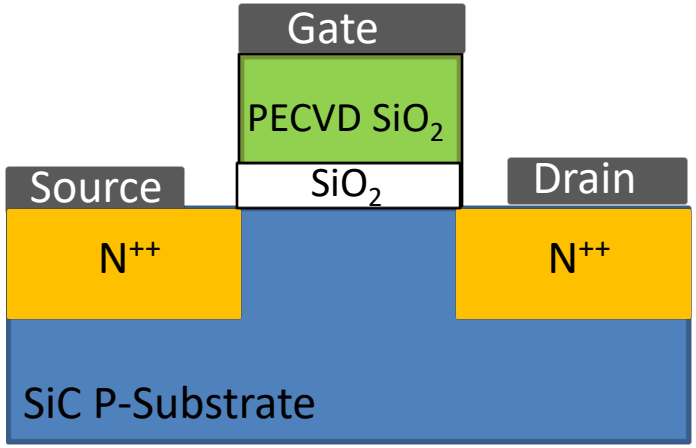
  $SiC + 2\ O_2 \rightarrow SiO_2 + CO_2$
- Some residual C may remain,

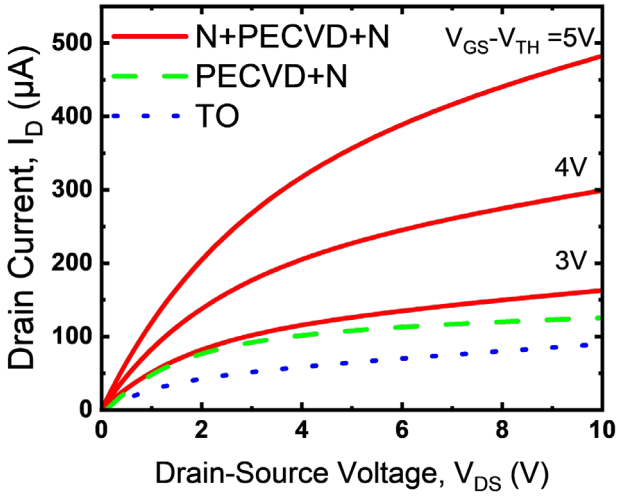
  $SiC + O_2 \rightarrow SiO_2 + C$
- thin grown SiO_2 → Fewer defects



- Oxide thickness increases with oxidation time.
- Oxidation rate reduces with oxidation time as oxide thickness increases.

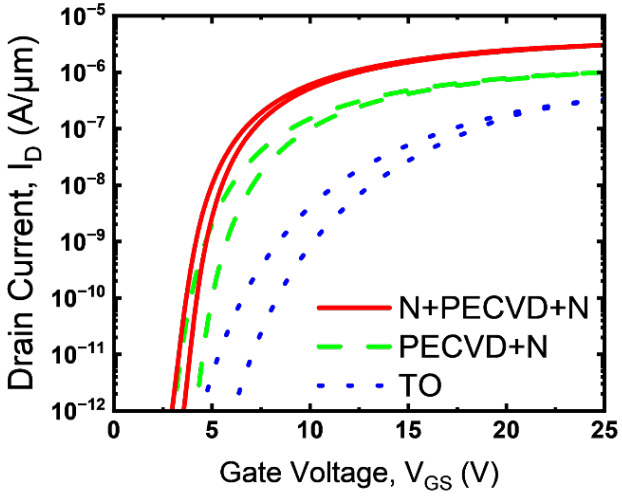
Re-engineering the Gate Stack: ICSCRM 2023





- Ultra-thin oxidation
- New paradigm:
  - N_2O pre-treatment; SiO_2 by PECVD;
- High T anneal (>1100°C), longer t (~100min)
- High field effect mobility 94 $cm^2/V.s$
- Reduced V_{TH} instability
- Low D_{it} 1.2×10^{11} - $<10^{10}$ $cm^{-2}eV^{-1}$

- *Yakut et al ICSCRM 2023*



Summary:

- Semiconductors underpin electronic systems
- MOSFETs rule!
- Semiconductors in the UK - crisis? what crisis?
- Silicon Carbide has promise for power electronics