Going Vertical: Can GaN Compete above 650V?

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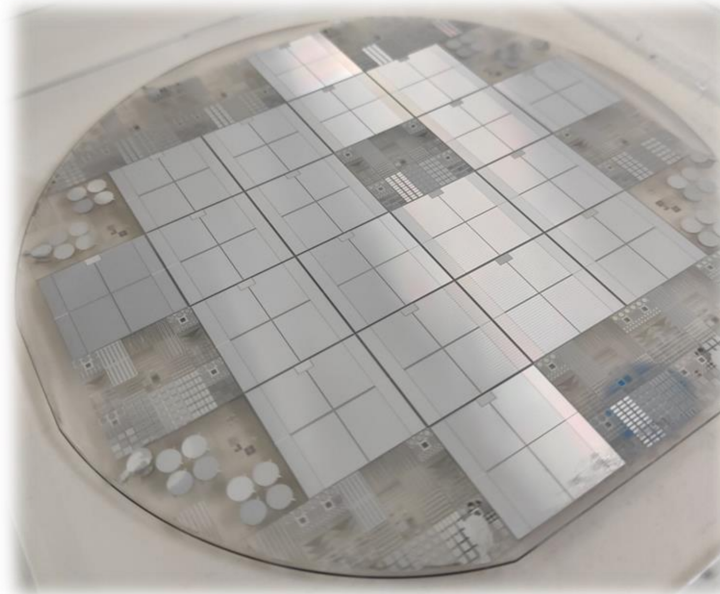

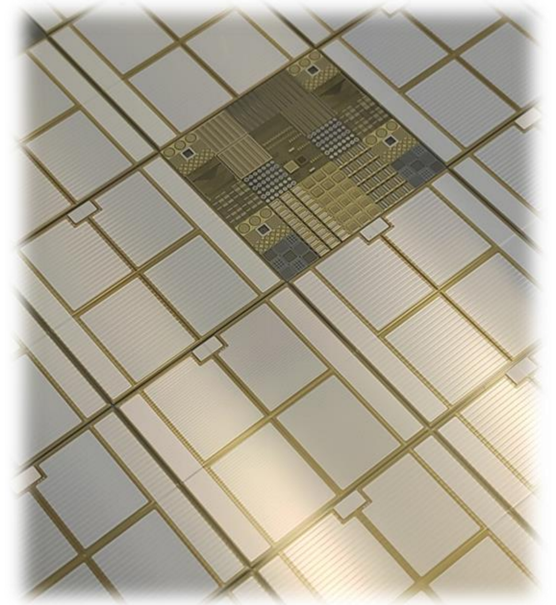

3rd July 2023

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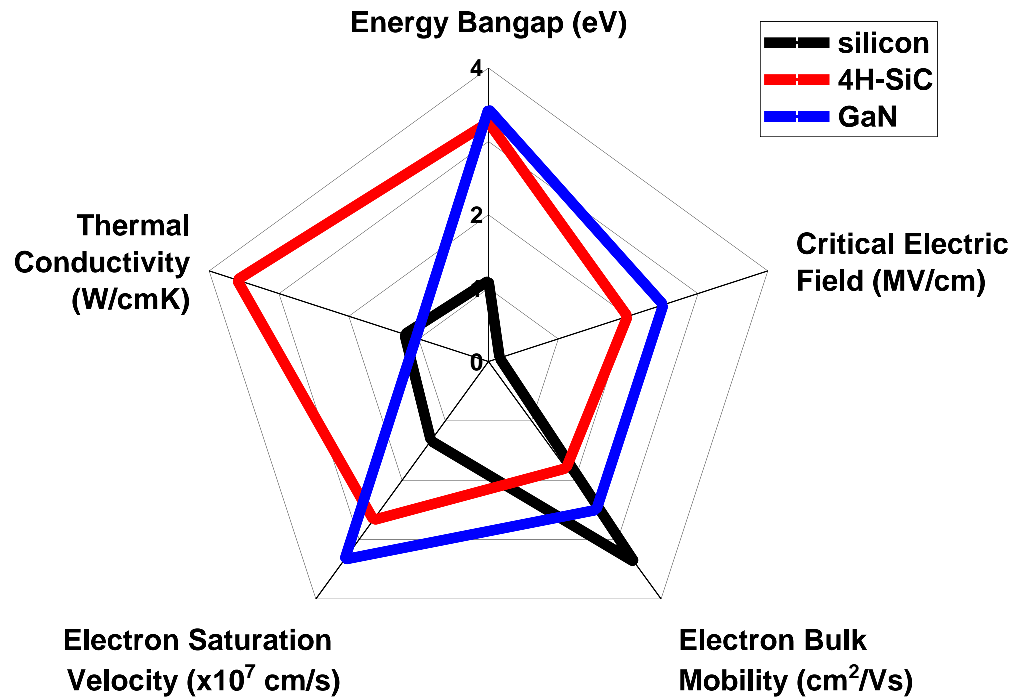
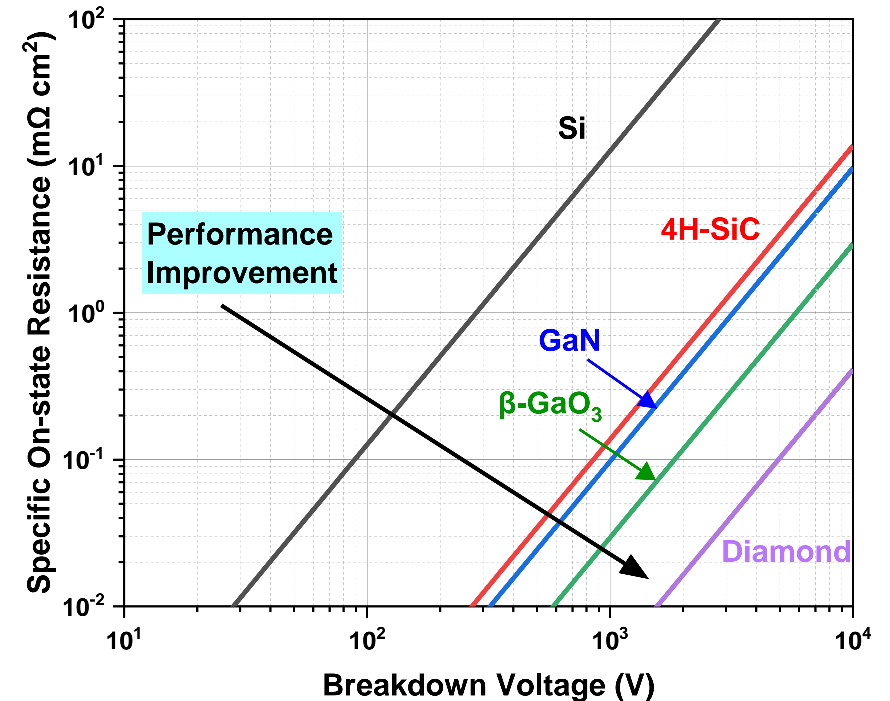
Motivation to move to WBG Materials





Increase in E_g → Higher E_c → Thinner, lower resistivity drift region → Lower $R_{ds,on(sp)}$ → Reduced **Conduction losses**

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3}$$

→ BFOM

1. T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," pp. 402-405, doi: 10.1109/WiPDA.2015.7369328.

Scaling for WBG Devices

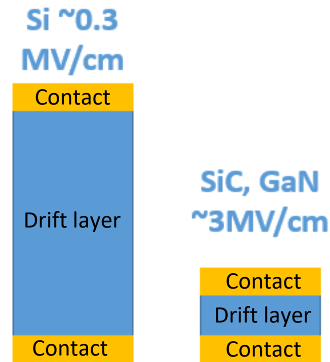
Lower $\mathbf{R_{on,sp}}$ ($\mathbf{R_{on}}$ **A)**

Smaller **Area** for same current

Lower **Capacitance**

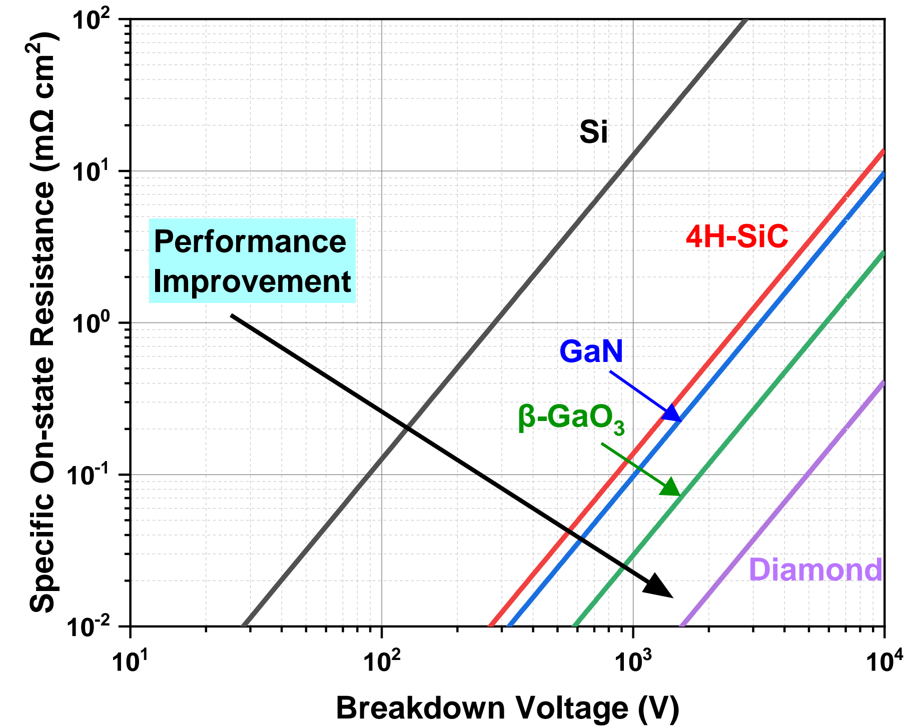
Faster **Switching time**

Reduced **Switching losses per cycle**



Thinner drift regions due to higher E_c

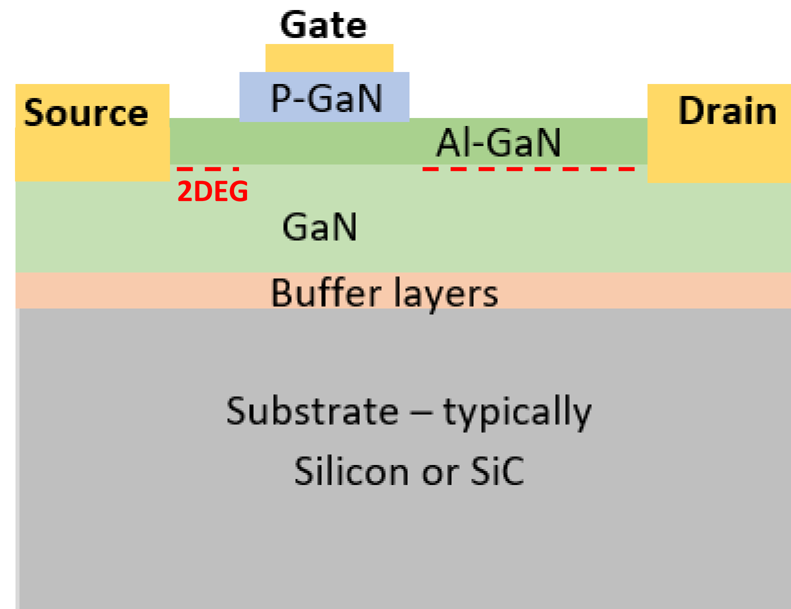
Smaller Die sizes due to lower $R_{ds,on}$



$$C = \frac{\varepsilon_S A}{d}$$

Comparing Lateral and Vertical GaN

Lateral Device: enhancement mode HEMT



Vertical Device: Trench MOSFET

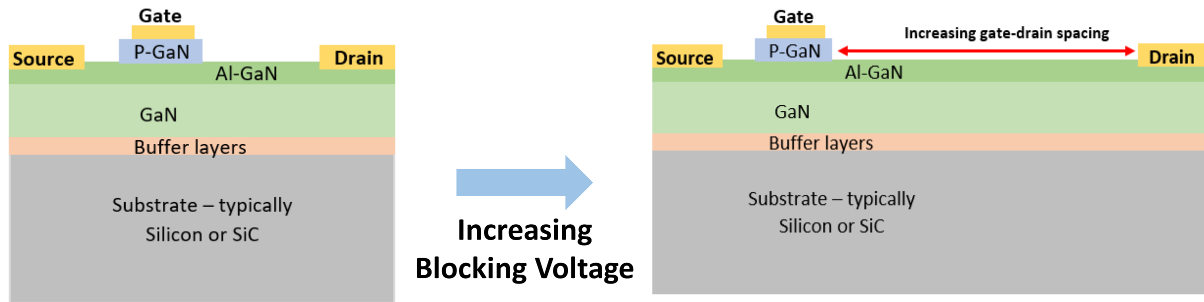
- Low R_{on} due to high electron mobility in 2DEG
- Commercially available
- Zero Q_{RR} - no reverse recovery losses (no PN junction)
- Fast switching performance (low Q_G, C_{GD})

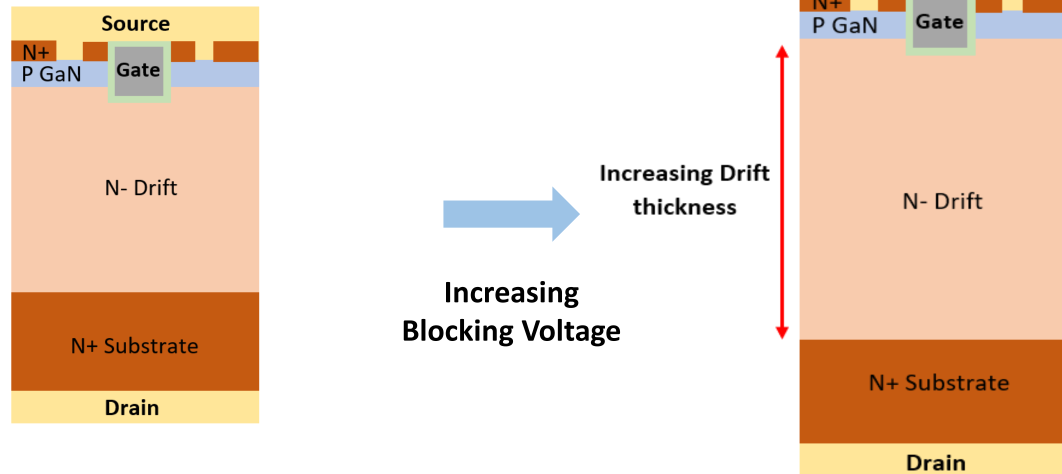
- Blocking voltage dependant on contact spacing
- No avalanche capability

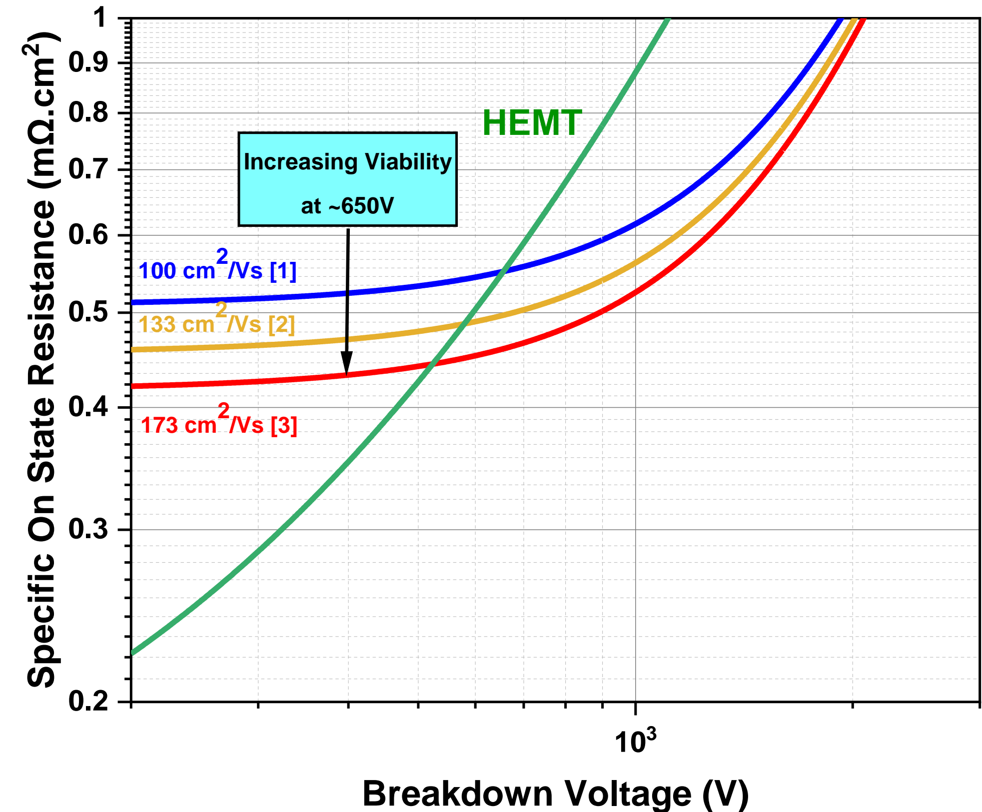
- Standard MOS gate
- Blocking voltage independent of area – ideal for voltage scaling
- Avalanche Capability

- Mobility limited by channel
- Requires P-type doping

Scaling for Blocking Voltage

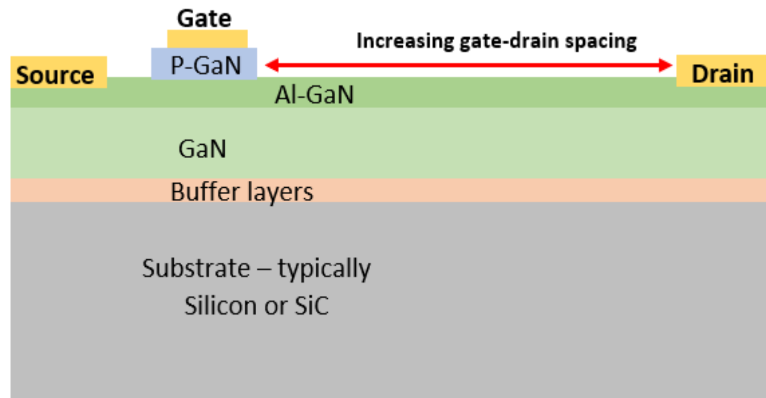


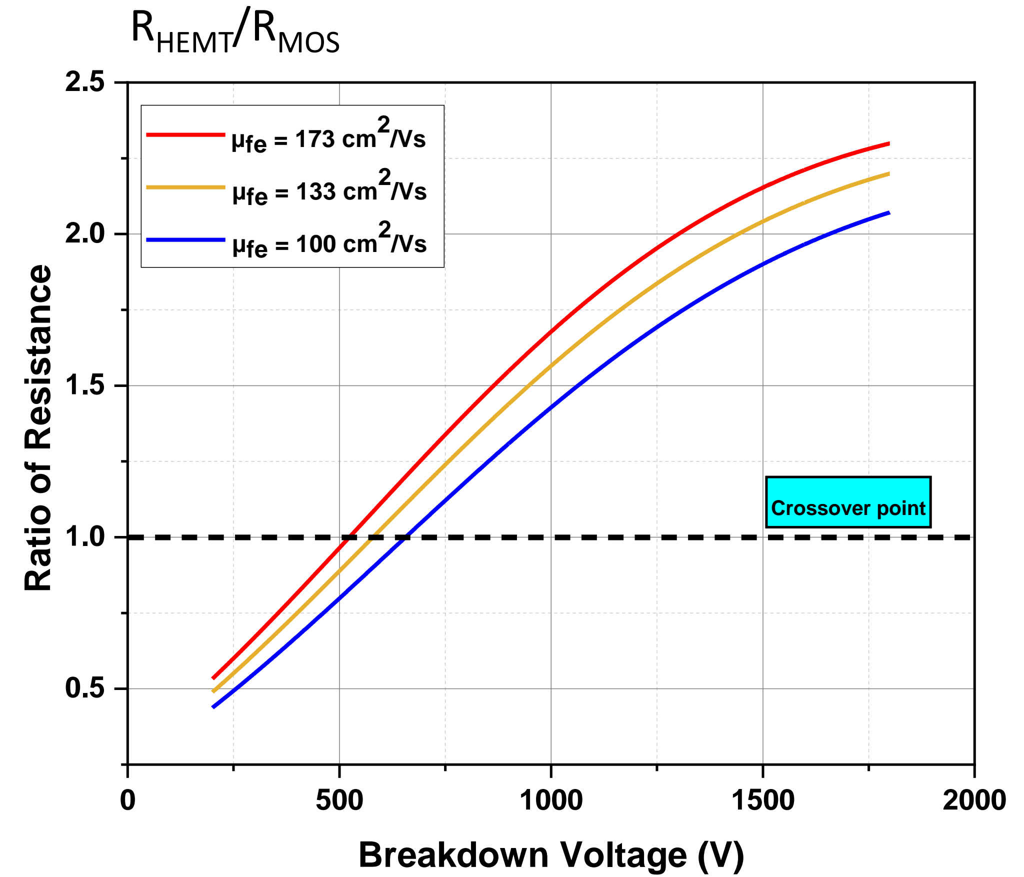




1. M. Kuraguchi *et al*., "Improvement of channel mobility and reliability in GaN-MOSFETs," *2019 CSW,* pp. 1-2, doi: 10.1109/ICIPRM.2019.8819114.
2. Hirotaka Otake *et al* ,"GaN-Based trench gate MOSFETs with over 100 cm²/Vs channel mobility", 2007 *Jpn. J. Appl. Phys.* 46 L599
3. Ryo Tanaka *et al* ," Mg implantation dose dependence of MOS channel characteristics in GaN double-implanted MOSFETs " , 2019 *Appl. Phys. Express* 12 054001

Scaling for Blocking Voltage





- ✓ HEMTs have superior $R_{ds,on(sp)}$ as μ_{2DEG} is far higher than μ_{fe}
- ✗ Scaling laterally for breakdown voltage results in larger die sizes than vertical GaN above 650V

HEMTs: Derating Issues

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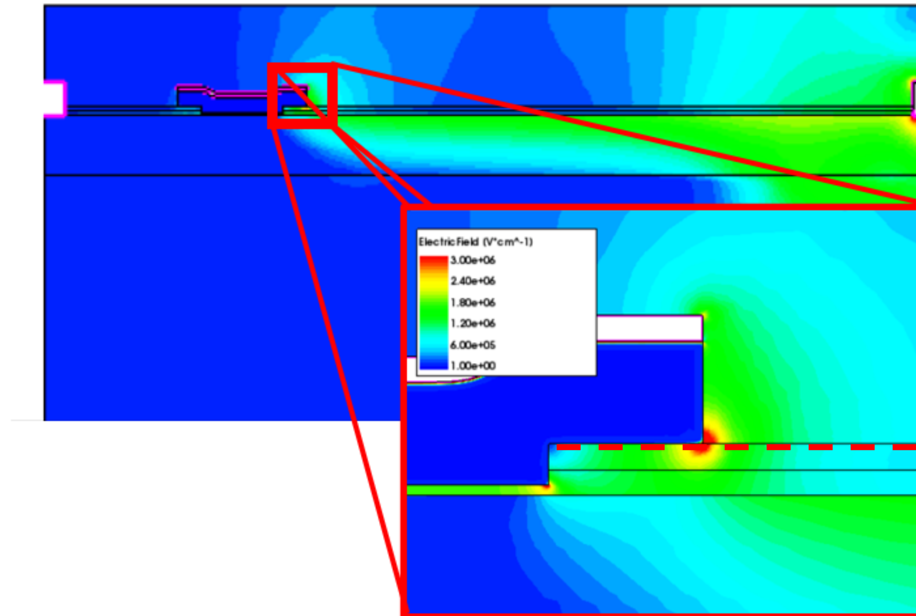
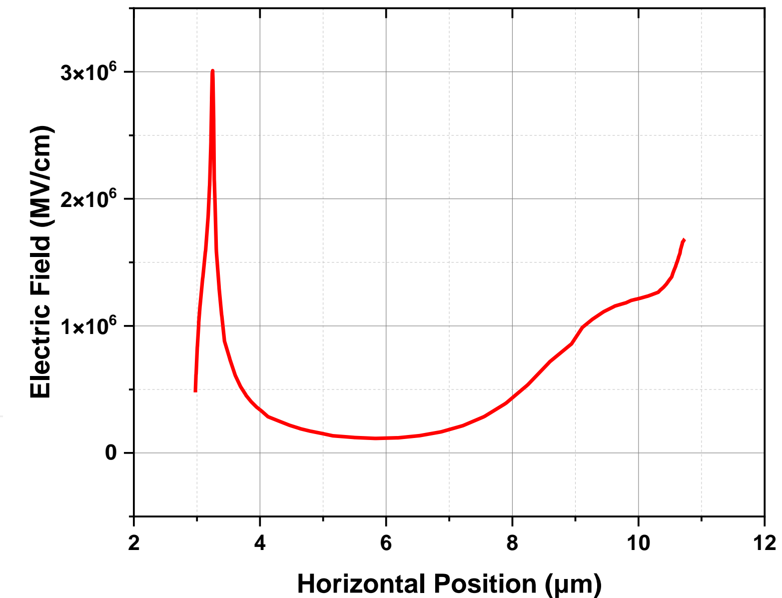
- Due to the structure of HEMTs, consistent high fields can be experienced in passivation layers between the gate and drain electrodes
- Breakdown in dielectric is destructive, unlike impact ionization in a semiconductor
- Time dependant dielectric breakdown (TDDB) is also a concern -> further derating



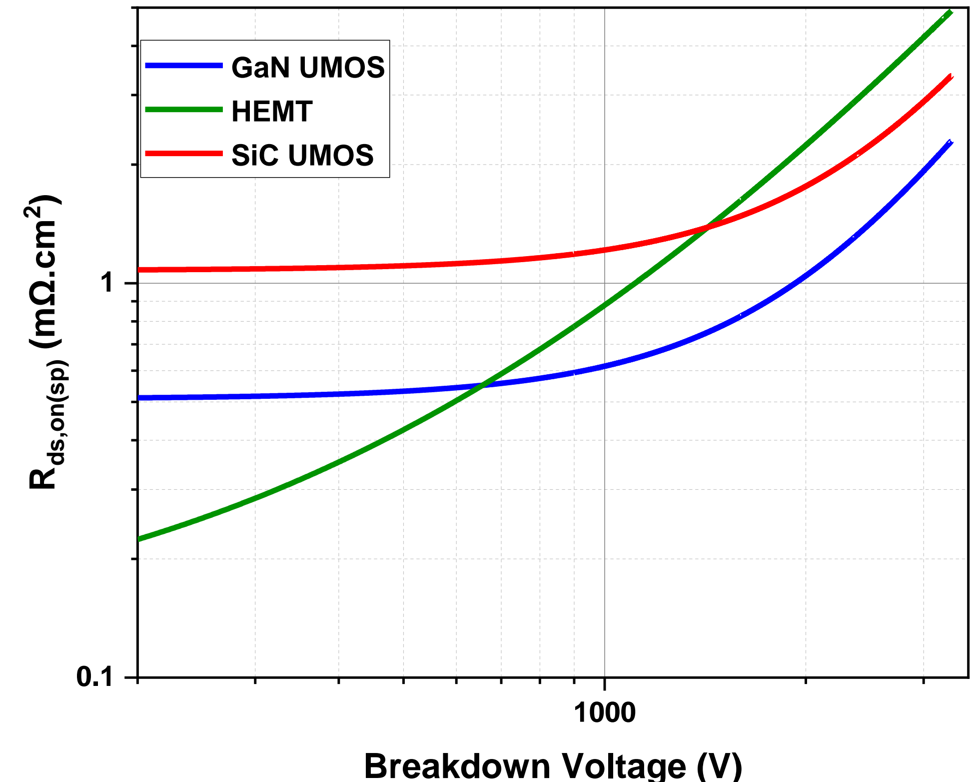


Simulated Electric field profile in a HEMT at V_{ds} = 400V, V_{gs} = 0V.

Comparing to SiC Trench MOSFETs

- SiC Trench MOSFETs mature technology nodes which compete with HEMTs today at 650V
- However lower $E_{c,}$ μ_{FE} and μ_d result in GaN trench MOSFETs having better ideal performance
- Are these values realistic?

Parameter	4H-SiC	GaN
E_c (MV/cm)	2.49	3.19
μ_d (cm^2/Vs)	720	1000
μ_{FE} (cm^2/Vs)	40	100-173 [1-3]



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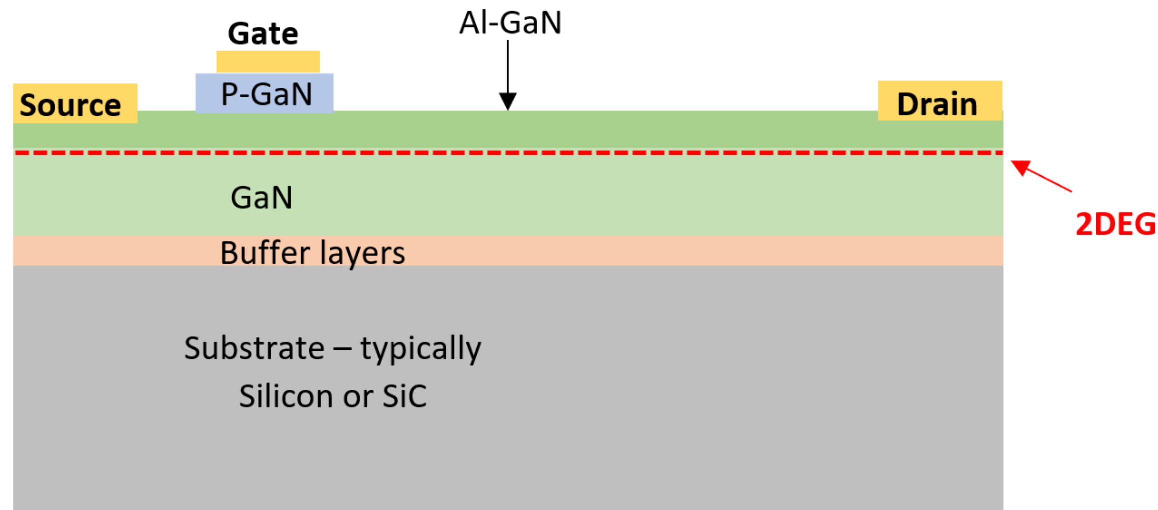
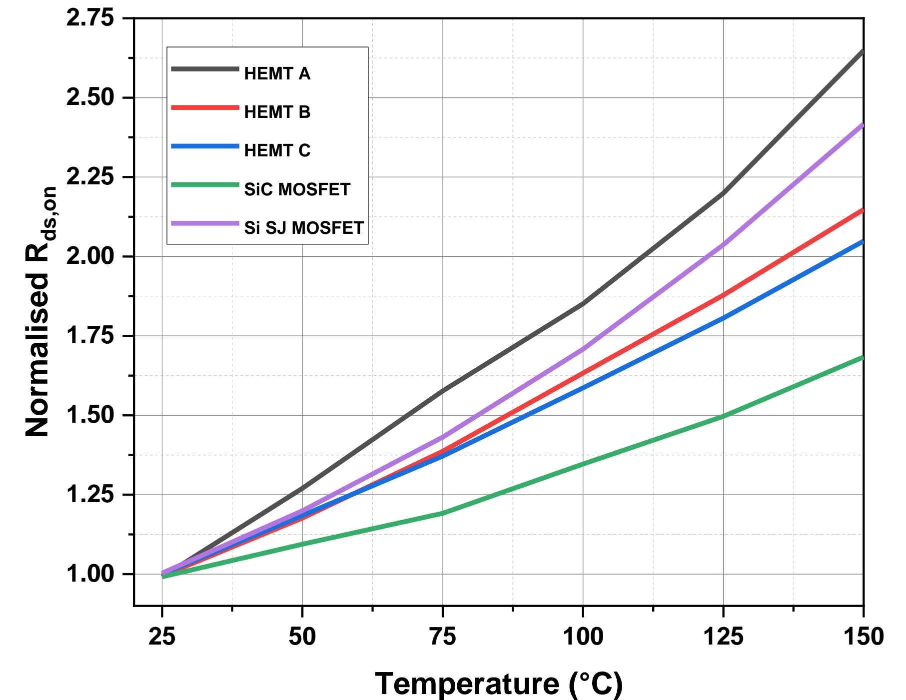
High Temperature Operation





- Due to the nature of the 2DEG channel in HEMTs, elevated temperature significantly increases $R_{ds,on}$

Derating

High R_{on} temperature coefficient Higher Current Device needed to achieve target current at temperature Larger Die Area Higher Capacitance Increase **Switching losses per cycle**

Choosing a Substrate for Vertical GaN

Property	GaN on Si	Gan on SiC	GaN on GaN
Defect Density (cm^{-2})	10^9	10^8	10^3 to 10^6
Lattice Mismatch (%)	17	3.5	0
CTE Mismatch (%)	54	25	0
Layer Thickness (µm)	<5	<10	>50
Breakdown Voltage (V)	<1000	<2000	>5000
Off-state Leakage	High	High	Low
Device Types	Lateral	Lateral, vertical possible	Vertical
Available Size	8”	6”, 8” on horizon	4”, 6” on horizon
Cost	$	$$	$$$

P-type GaN Issues

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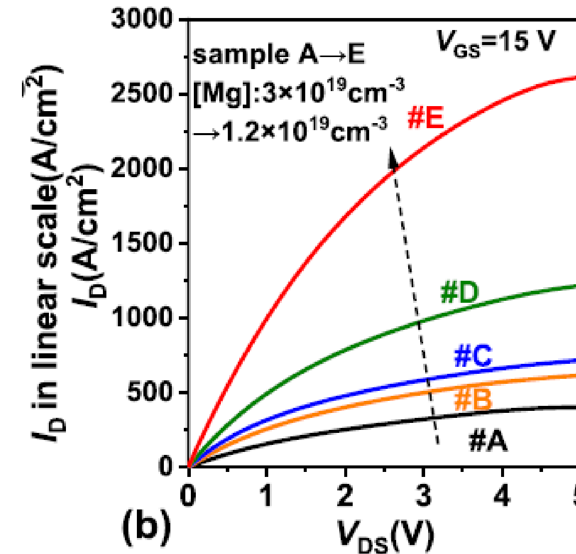
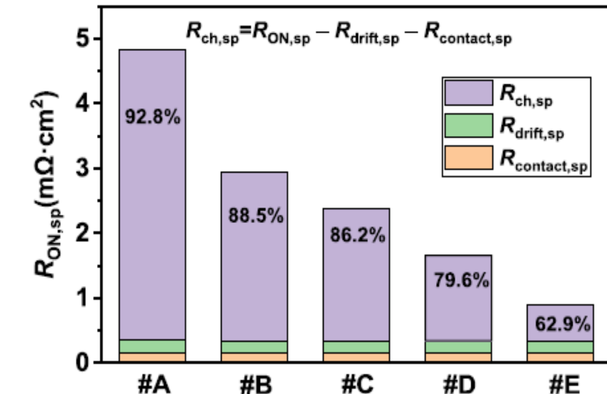
P-type GaN is required to form the P-base region of the MOSFET

- P-type GaN is grown using Mg as an acceptor
- Activation typically lies around **1-3%** due to:
  - Decomposition of GaN above 1473K [1]
  - 150-200meV activation energy of Mg [2]



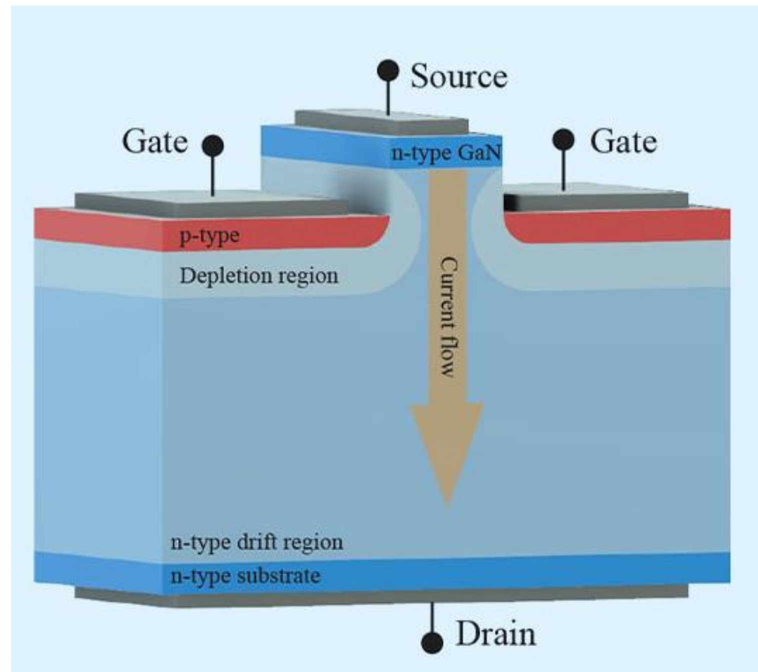


Sample	A	B	C	D	E
Mg target Conc. (10^{19} cm^{-3})	3	2.6	2.3	1.8	1.2
V_{th} (V)	7.75	7.53	7.05	5.21	4.7
$I_{ds,MAX}$ (A/cm^2)	400	635	713	1261	2605
$R_{ds,on(sp)}$ ($m\Omega.cm^2$)	4.83	2.95	2.39	1.66	0.89

Results from a study on the effect of Mg Conc. on on-state performance. [3]

1. Sakurai, H et al, "Highly effective activation of Mg-implanted p-type GaN by ultra-high-pressure annealing", 2019, *Applied Physics Letters*, *115*(14), p.142104.
2. Pu, T et al, "Review of recent progress on vertical GaN-based PN diodes", 2021 *Nanoscale Research Letters*, *16*(1), pp.1-14
3. R. Zhu et al, "Effects of p-GaN Body Doping Concentration on the ON-State Performance of Vertical GaN Trench MOSFETs" 2021, *IEEE Electron Device Letters*, 42(7), pp. 970-973.

Commercial Vertical GaN Today



Example vertical GaN JFET design

There are two companies currently manufacturing vertical GaN power devices:

Parameter	NexGen	Odyssey
Technology	Vertical GaN JFET	Vertical GaN JFET
Blocking Voltage (V)	1200	650,1200
Current Rating (A)	35	10
$R_{ds,on}$ at 25°C (mΩ)	60	-
Method of achieving P-type	Epitaxial	Implant
Package	8x8 DFN	8x8 DFN
Development Stage	-	Delivered first samples to customers Q1 2023

Quasi-Vertical GaN-on-SiC MOSFETs

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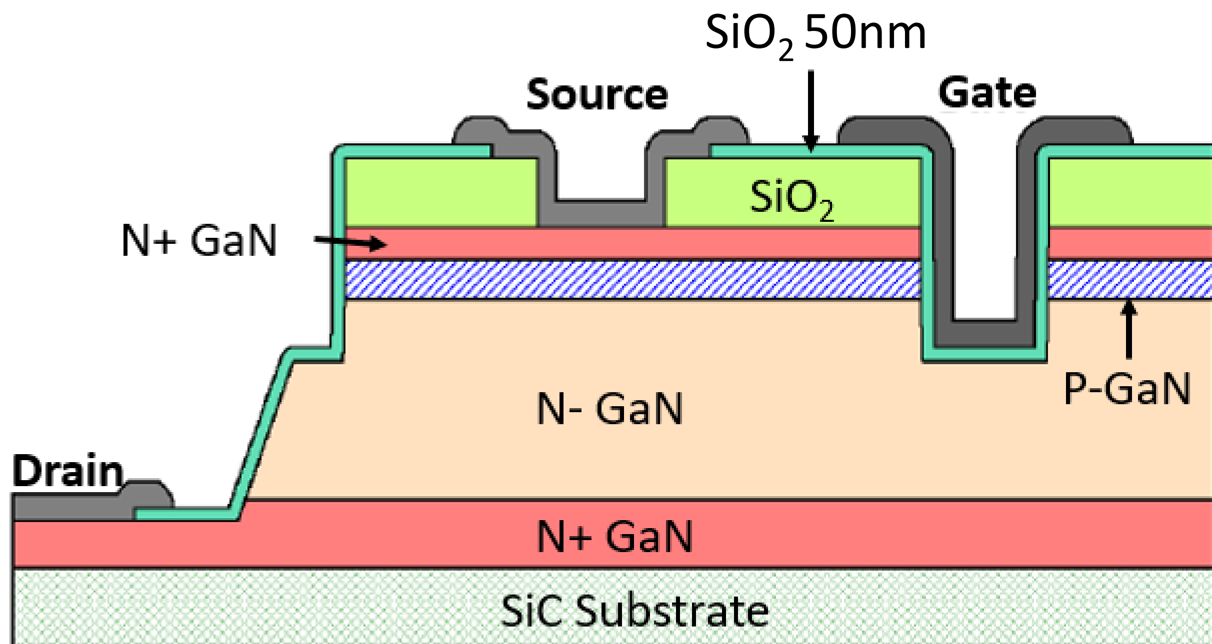
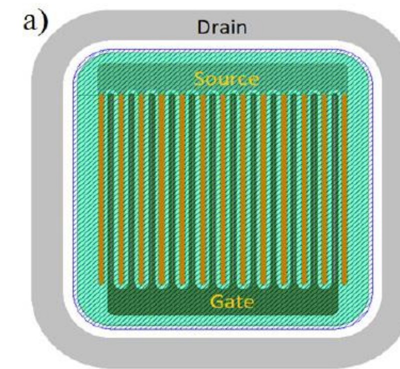
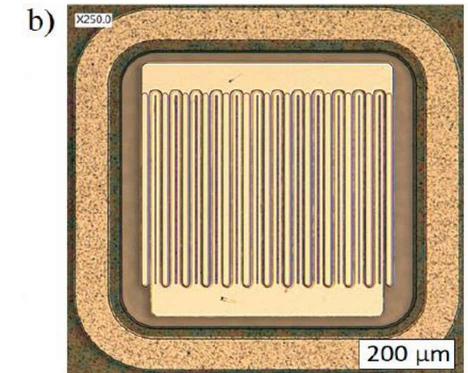
- Initially aiming for **200V** for 48V mild HEV DC-DC converter applications
- 2.5um drift layer

Region	Thickness (µm)	Doping (cm^{-3})
N+ Source	0.02	$5x10^{18}$
N Source	0.2	$5x10^{18}$
P Body	0.4	$3x10^{19}$
N- Drift	2.5	$1x10^{17}$
N+ Drain	0.5	$1x10^{19}$
SiC Substrate	350	Semi-Insulating



Q-Vert GaN MOSFET cross-section

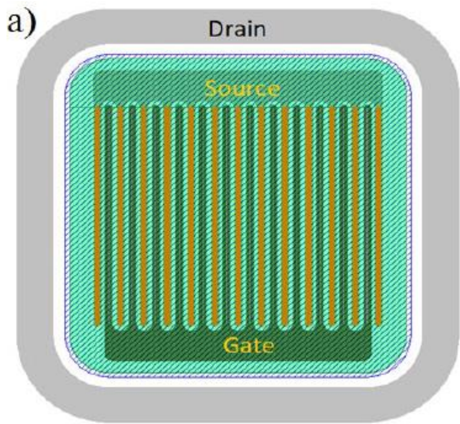


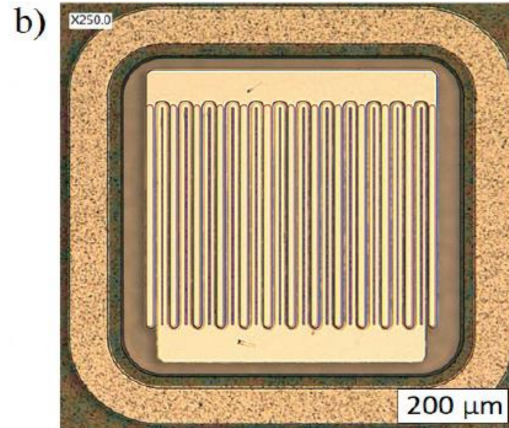


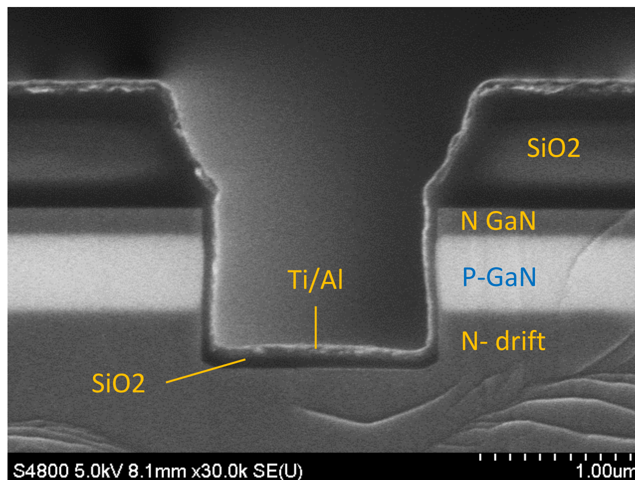
(a) Top down mask layout of q-vert MOSFET (b) Image of fabricated device

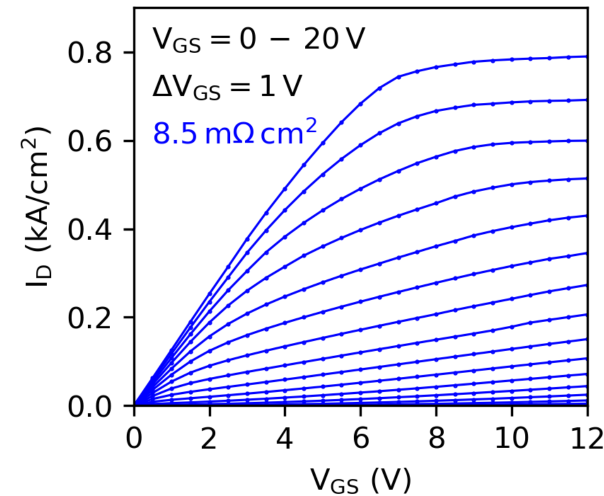
1. Evans, J. et al, 2023. Fabrication of Quasi-Vertical GaN-On-SiC Trench MOSFETs. *Key Engineering Materials*, *945*, pp.61-66.

Quasi-vertical GaN MOSFET – DC Characteristics



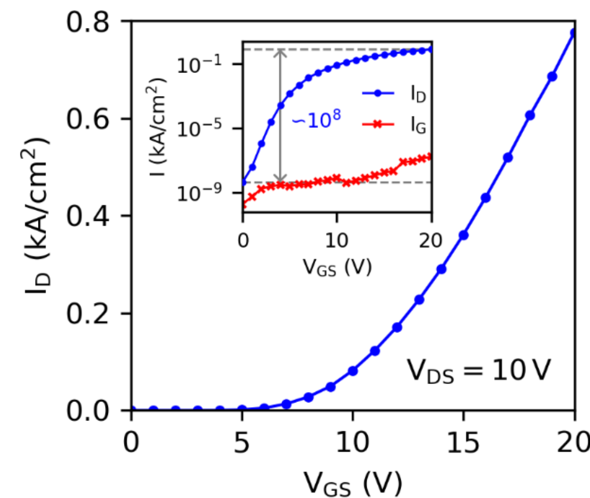


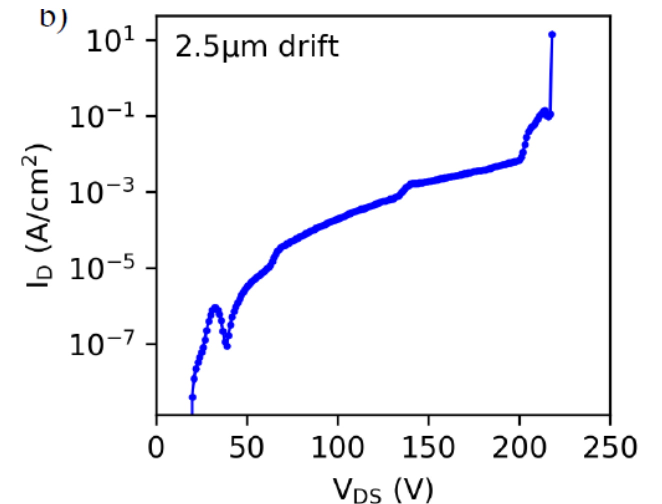




12 finger devices (1x1mm)

- **V_{th} ≈ 9 V**
- **I_{max} ≈ 250 mA**
- **$R_{ds,on(sp)}$ ≈ 8 mΩ.cm^2**
- **V_{br} ≈ 220V (90V/μm)**





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2D TCAD Model of Q-Vert Device

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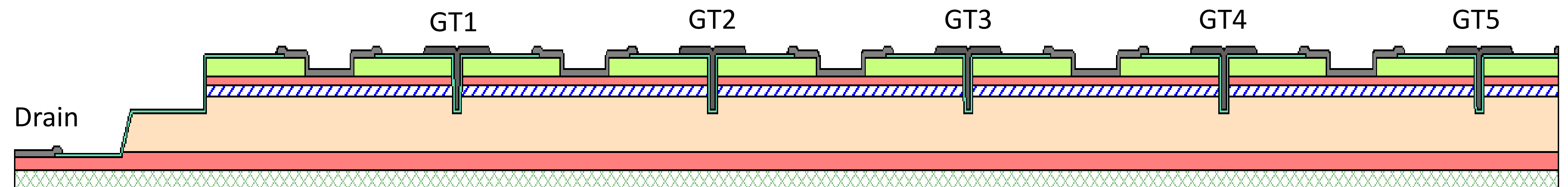
- Simulation of current density in on-state looking at different gate trenches
- Asymmetric current distribution correlating with distance from drain contact
- Significant lateral current spreading through drift layer in more active gate trenches
- Does not take into account 3D effects – shows worst case scenario

Gate Trench 1

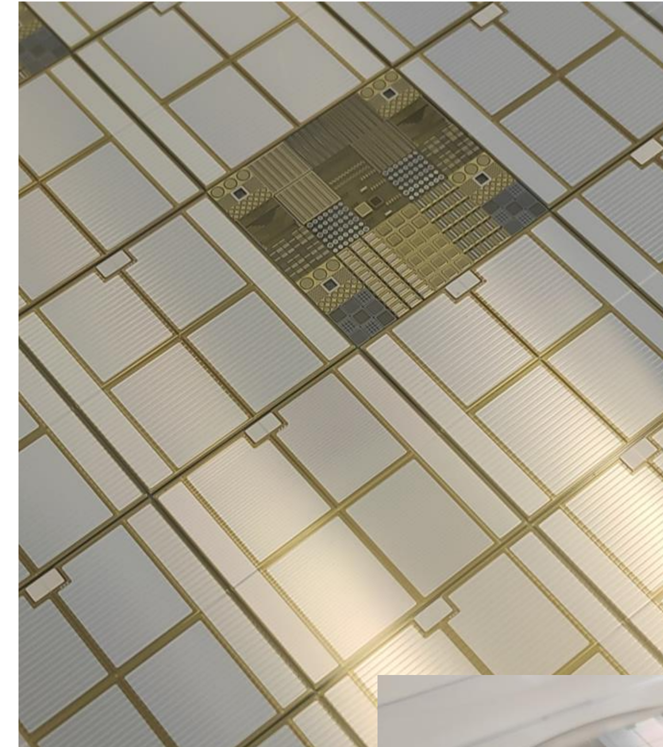
Source
Gate
Source
SiO_2
n-layer
p-body
Drift (5E16 cm^{-3})
Drain layer (1E19 cm^{-3})
X
Y

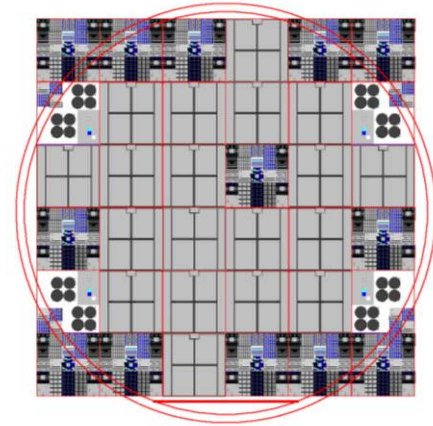
Gate Trench 5

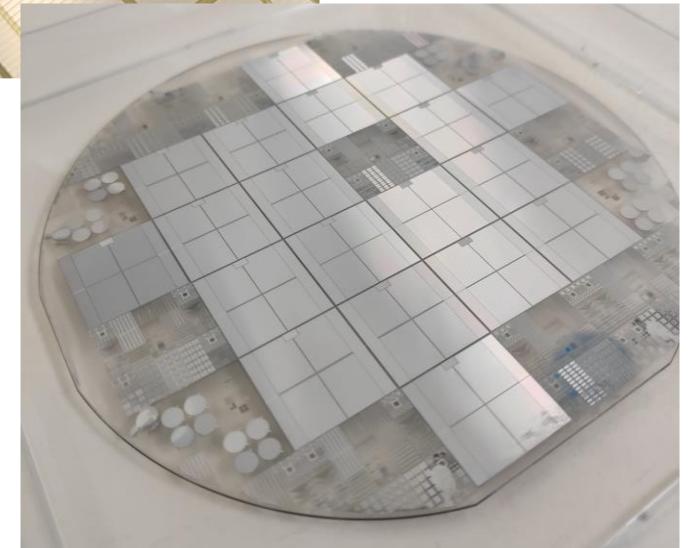
TotalCurrentDensity (A*cm^-2)
1.200e+04
1.000e+04
8.000e+03
6.000e+03
4.000e+03
2.000e+03
5.000e-01
X
Y



Conclusions







- **Key challenges for vertical GaN to overcome:**
  - Material quality - superior E_C compared with e.g. SiC?
    - Substrate dependant – availability of GaN substrates…
  - Are inversion layer mobilities of >100 $cm^2/V.s$ achievable?

- **HEMTs are not going anywhere!**
  - Advanced device structures to address challenges:
    - Polarised super junction
    - Parallel channel
    - GaN Ics
  - Can these be used to scale to voltages of 1.2kV?

Acknowledgements

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- Pegasus Chemicals
- SPTS (KLA Company)

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Thank you for your time, any questions?

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