EPSRC Centre for Power Electronics: Switch optimisation Theme

Ultra High Voltage Power Electronics:

Realising the Full Potential of SiC Devices Rated at 10 kV+

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Coventry University, UK: Samuel Perkins

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EPSRC CPE Switch Optimisation Theme: Contents

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EPSRC CPE Switch Optimisation Theme: Introduction & Background

Silicon Carbide: A maturing Industry

SiC is one of the revolutionary “wide-bandgap” semiconductors.

Like GaN, it has a high critical electric field allowing it to support high voltages, in very thin drift regions.

This means that a 1200V SiC MOSFET has a set of device characteristics (R_{DSON}, switching) similar to a 150 V Si MOSFET!

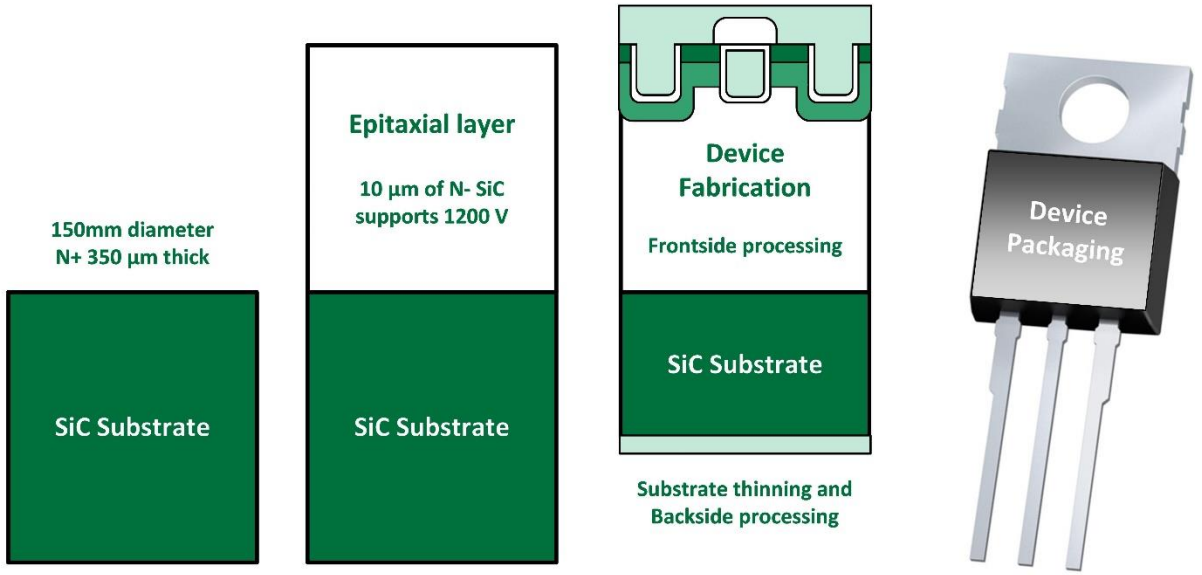
Chip Manufacturers are now getting to grips with SiC and the industry – from substrates, epitaxy, fabrication to packaging – is becoming established.

3x
Bandgap Energy

9x
Critical Electric Field

2.5x
Thermal Conductivity

Fundamental SiC Properties compared to Silicon



The SiC development processes

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Silicon Carbide: Fundamentals

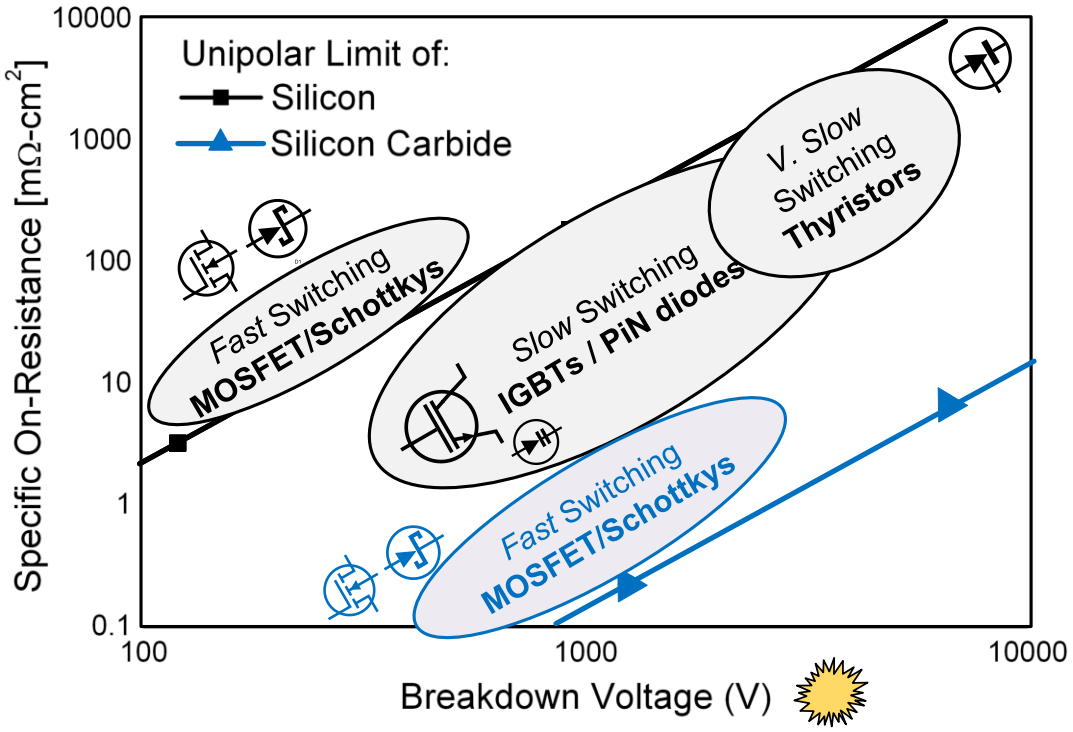
The high critical field of SiC can be exploited in one of two ways, by maximising breakdown voltage, or by minimising device resistance

3x
Bandgap Energy

9x
Critical Electric Field

2.5x
Thermal Conductivity

Fundamental SiC Properties compared to Silicon



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Silicon Carbide: Enabling EV

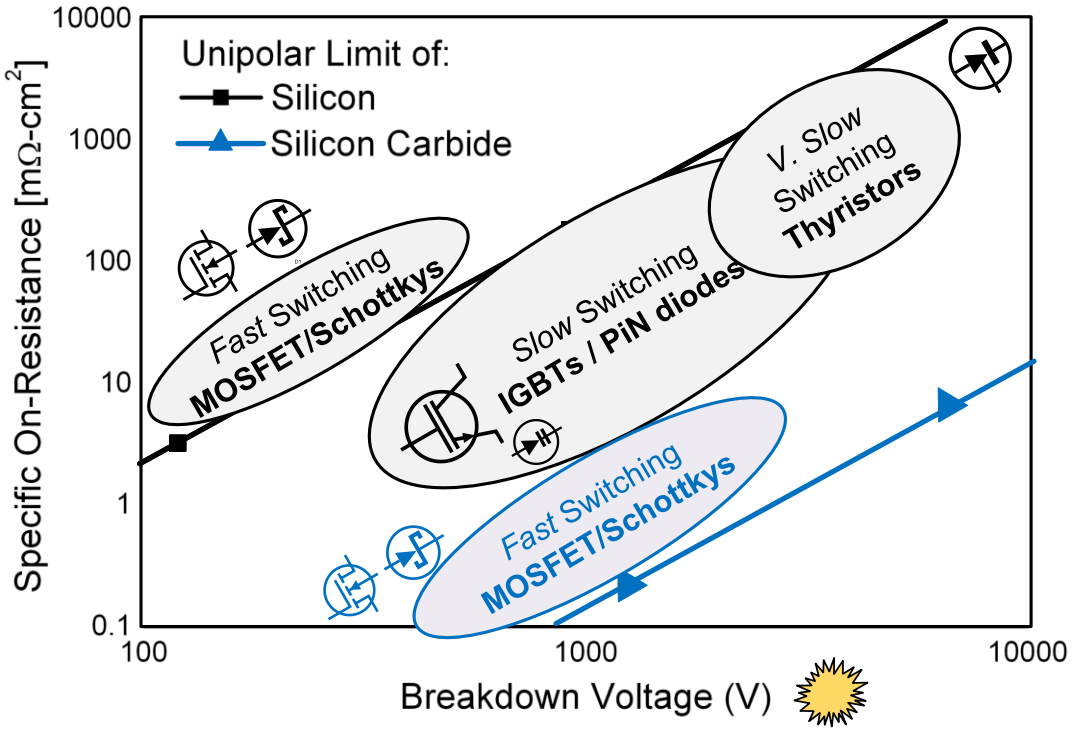
The properties of SiC MOSFETs are being utilised by EV manufacturers to produce small, light and highly efficient inverters, reducing battery weight and extending range.

3x
Bandgap Energy

9x
Critical Electric Field

2.5x
Thermal Conductivity

Fundamental SiC Properties compared to Silicon



ROHM supplies Full SiC Power Modules to Formula E racing team Venturi

http://www.rohm.com/web/global/news-detail?news-title=rohm-supplies-full-sic-power-modules-to-formula-e-racing-team-venturi&defaultGroupId=false

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Silicon Carbide: Maximising Potential

Today's SiC market barely scratches the surface of its potential market. HV MOSFETs, IGBTs and thyristors, all open up other applications from solar and traction, to HVDC and the grid.

3x
Bandgap Energy

9x
Critical Electric Field

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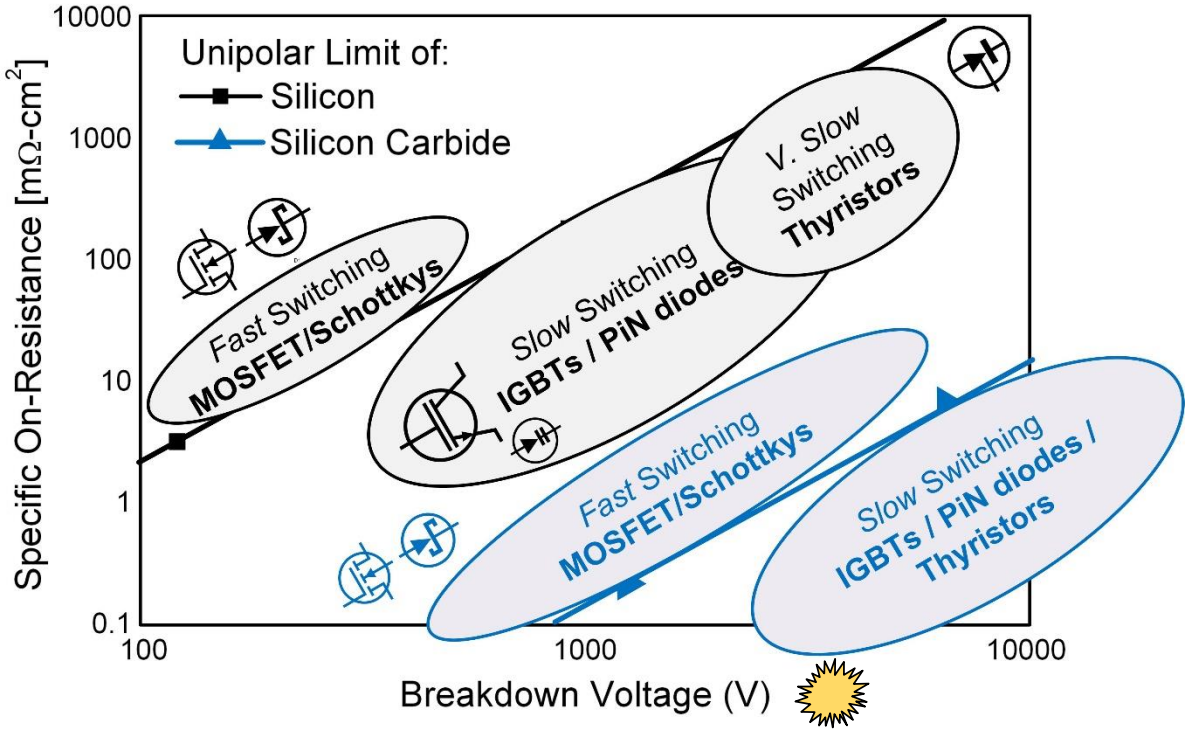
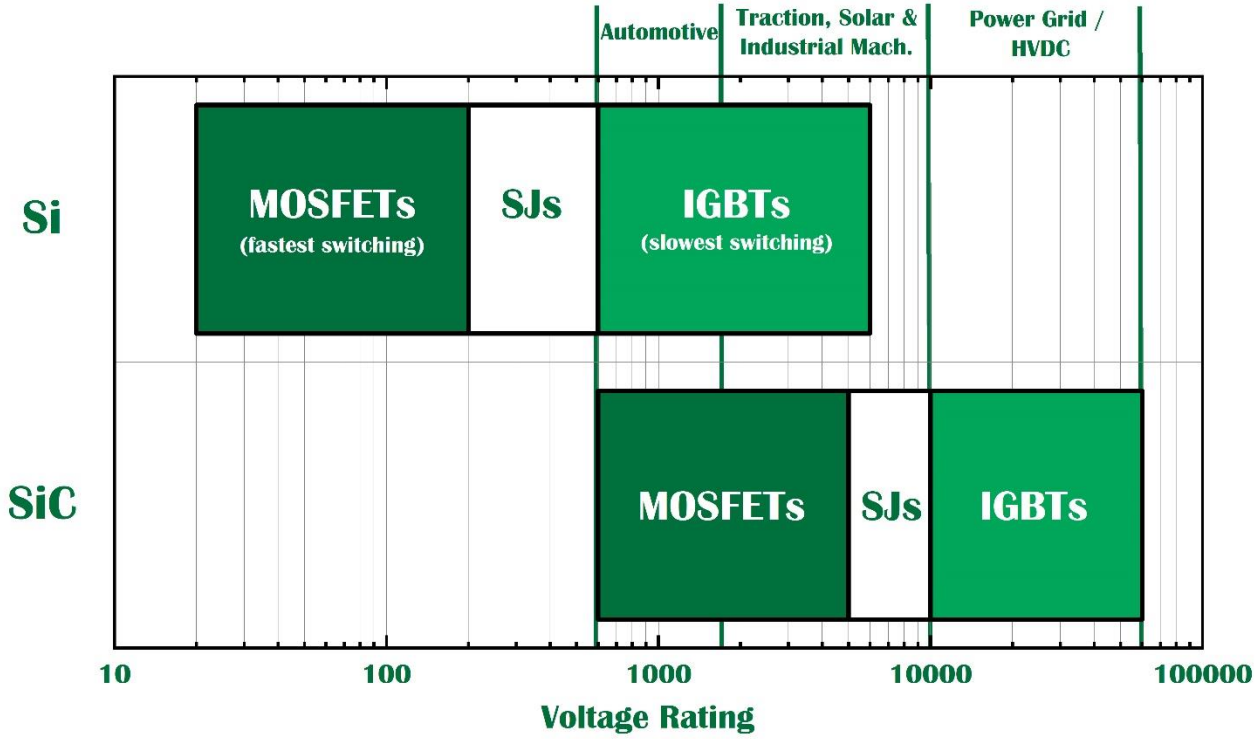
Fundamental SiC Properties compared to Silicon





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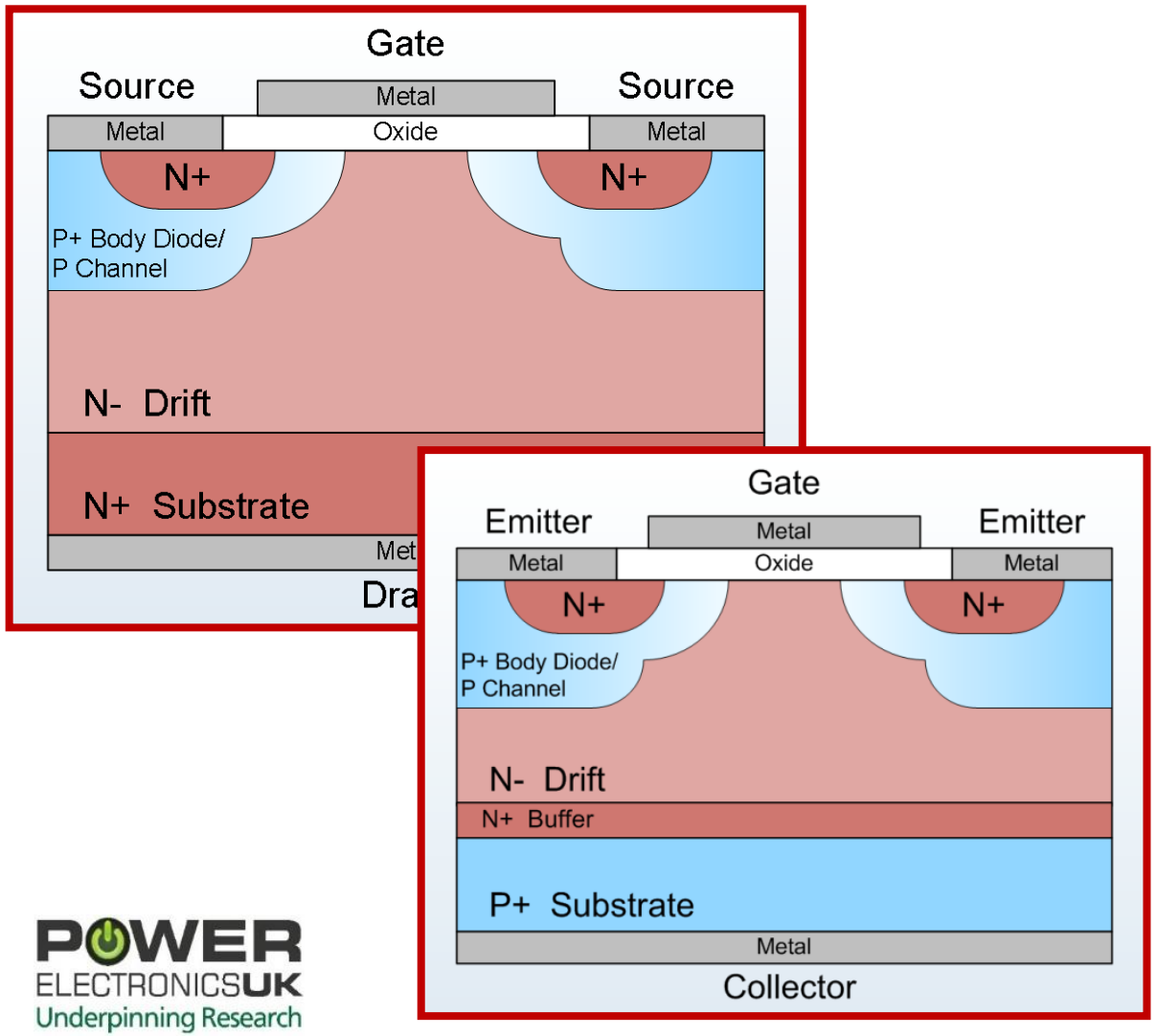
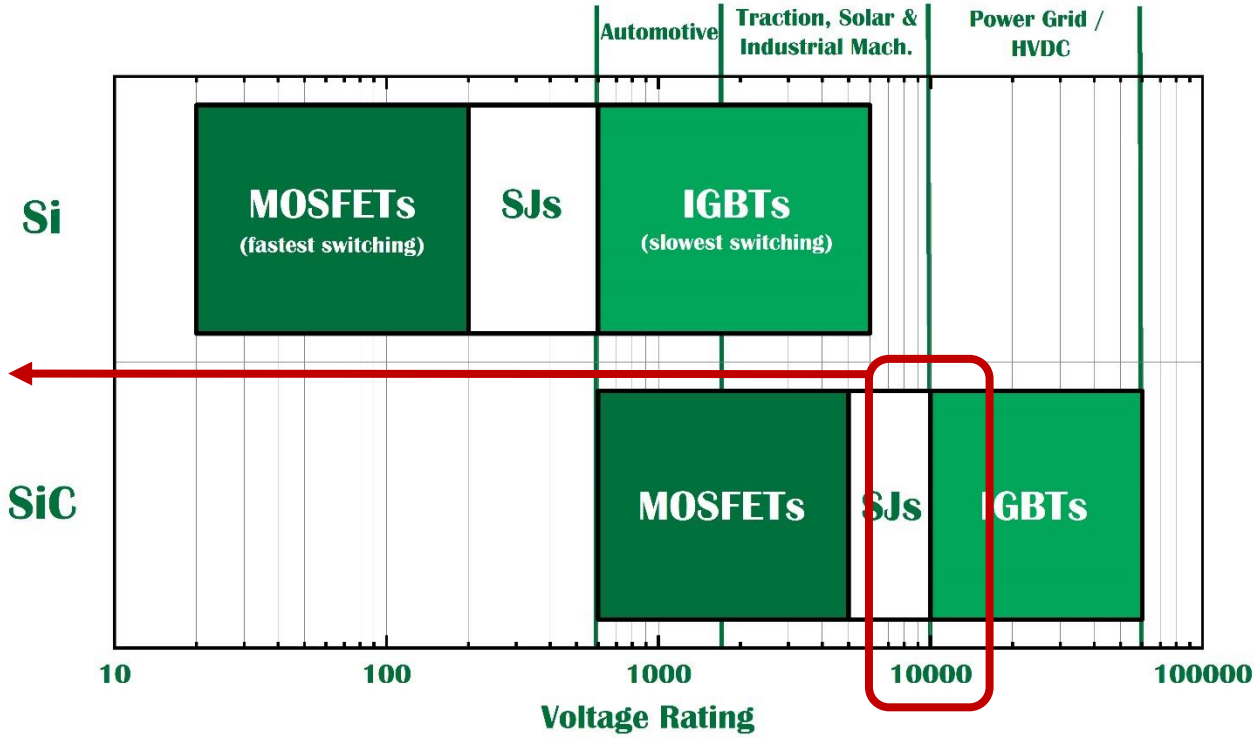
10 kV SiC MOSFETs and IGBTs



SO Theme: Maximising the potential of SiC

Begun in 2018, the goal of the Switch Optimisation Theme was to develop the SiC devices of tomorrow, IGBTs and MOSFETs rated to 10 kV.



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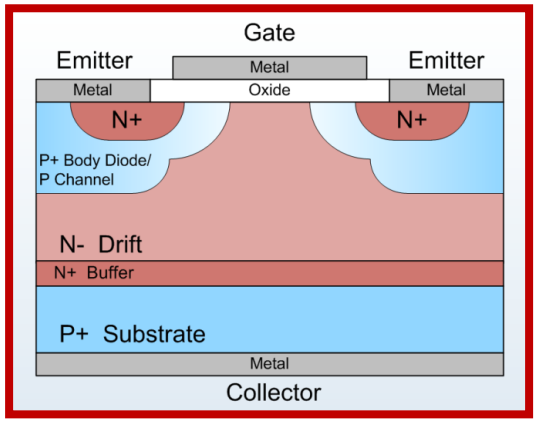
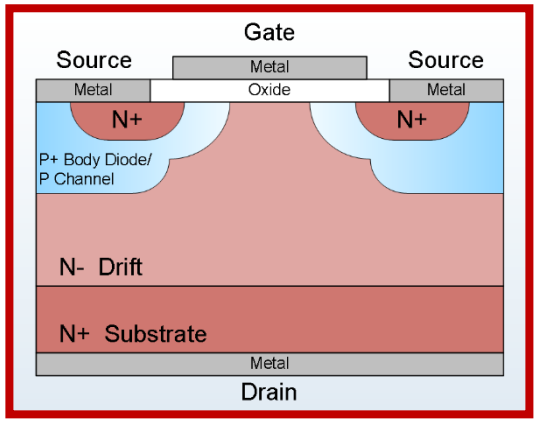
EPSRC CPE Switch Optimisation Theme: Introduction & Background

10 kV SiC MOSFETs and IGBTs

10 kV was selected as a transition voltage between unipolar and bipolar SiC devices with prospective applications in a number of high voltage applications including the grid, solid state transformers and HVDC.

The project was to involve two full development cycles from simulation, fabrication and testing.





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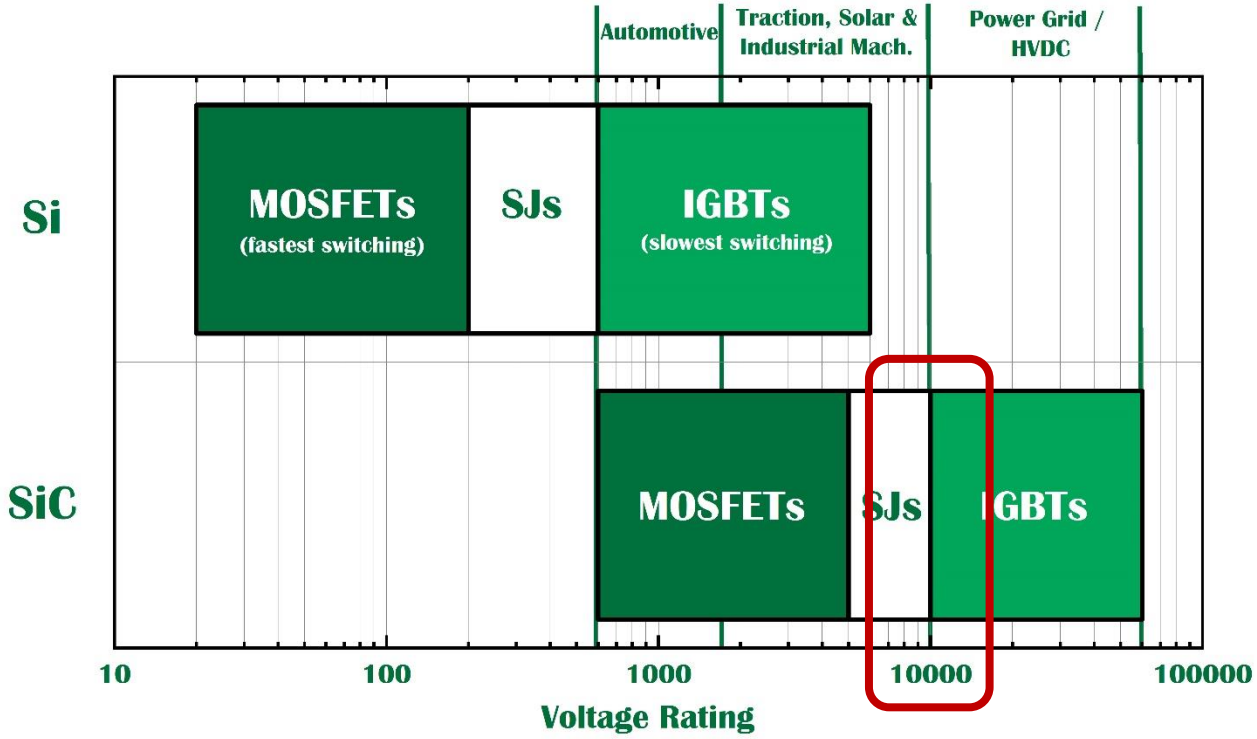

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EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

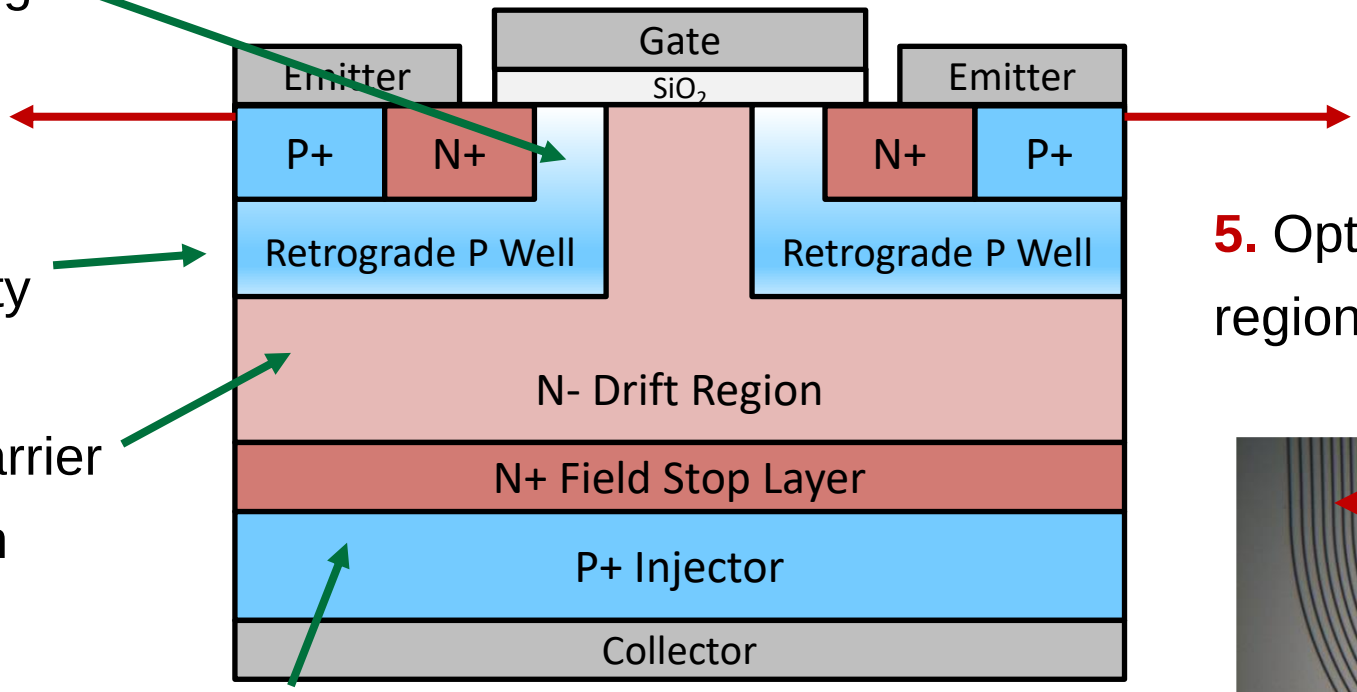
The UPE2: SO Theme IGBT

A challenging device to fabricate…

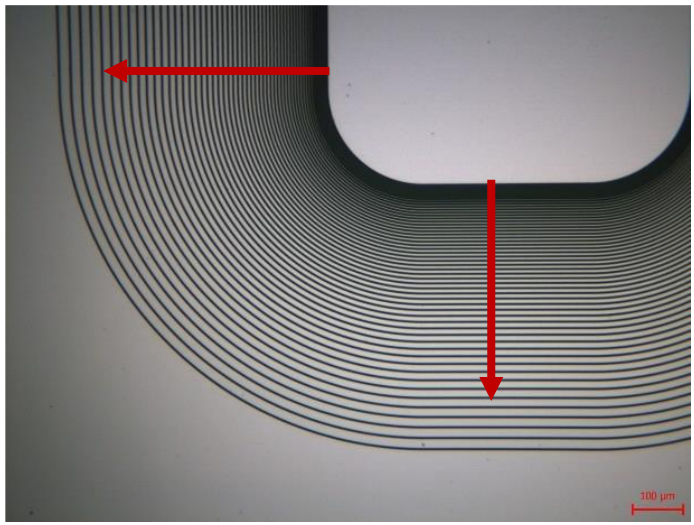
4. Optimising the frontside gate design

3. Maximising device robustness and reliability

2. High quality, high carrier lifetime SiC drift region



5. Optimising the termination regions for 10 kV



1. Forming a P+ injector with only N+ Substrates available

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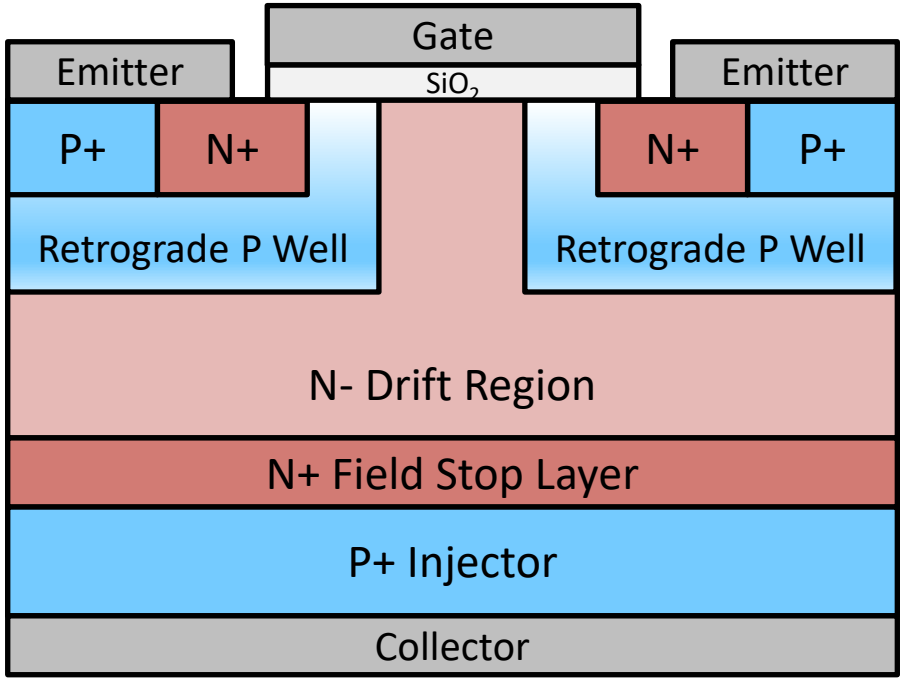
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

The innovation of the SO theme will be discussed as we go through the IGBT fabrication process!

The UPE2: SO Theme IGBT



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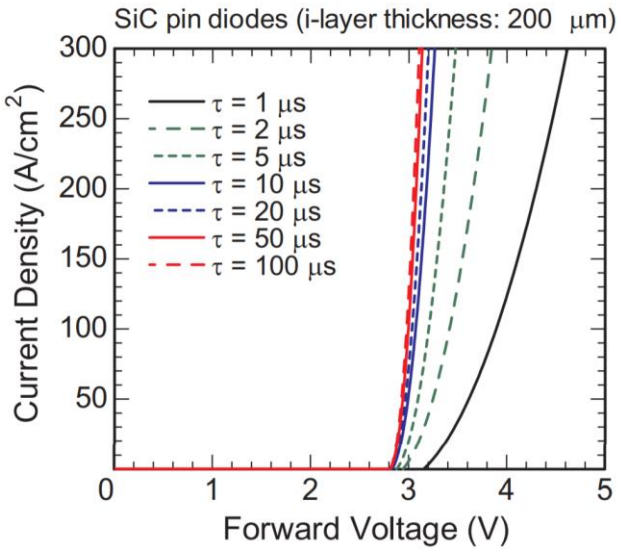
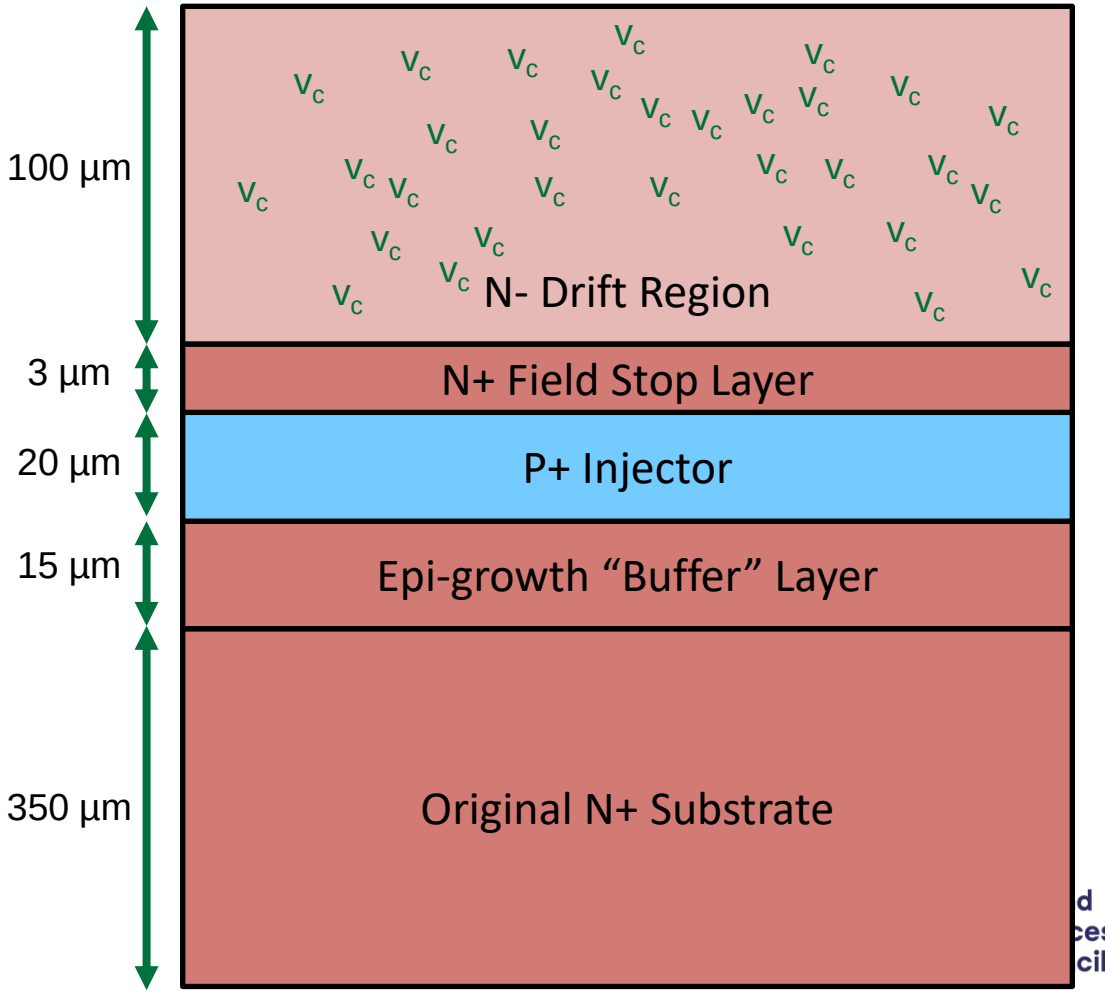
1. *Forming a P+ injector with only N+ Substrates available*

2. ***High quality, high carrier lifetime SiC drift region***

- Starting point is a 350 µm N+ 4H-SiC substrate.
- All the device layers are grown - epitaxially in a CVD reactor – on the substrate surface.
- However, all SiC has a large number of crystal defects – carbon vacancies
- These lower the carrier lifetime, reducing conductivity modulation.



The UPE2: SO Theme IGBT



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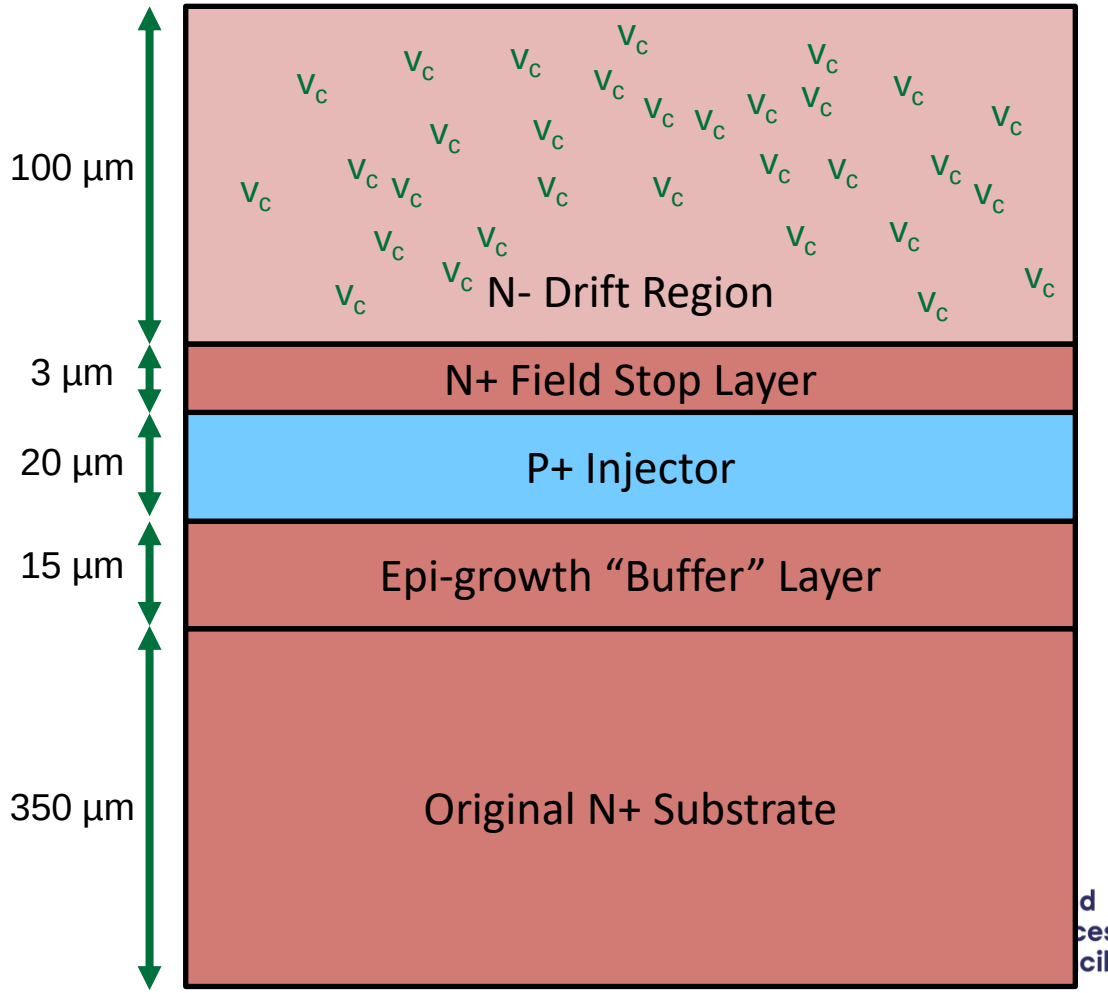
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*
2. ***High quality, high carrier lifetime SiC drift region***

- We therefore developed our own “Lifetime enhancement technique”.

The UPE2: SO Theme IGBT



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EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*
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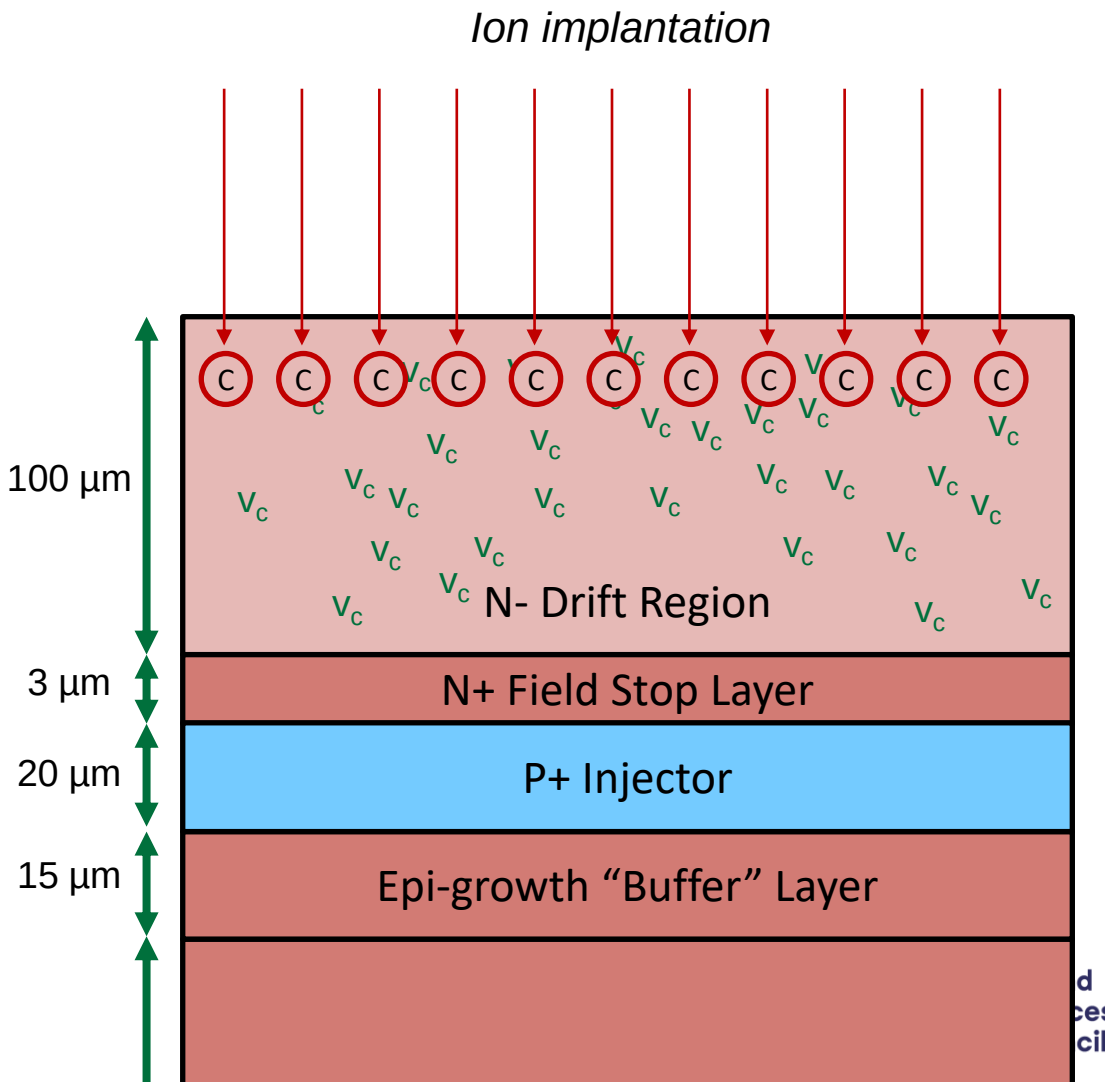
- We therefore developed our own “Lifetime enhancement technique”.
- First, carbon was implanted into the surface
- Then driven through the drift region with a 4 hour anneal.

The UPE2: SO Theme IGBT



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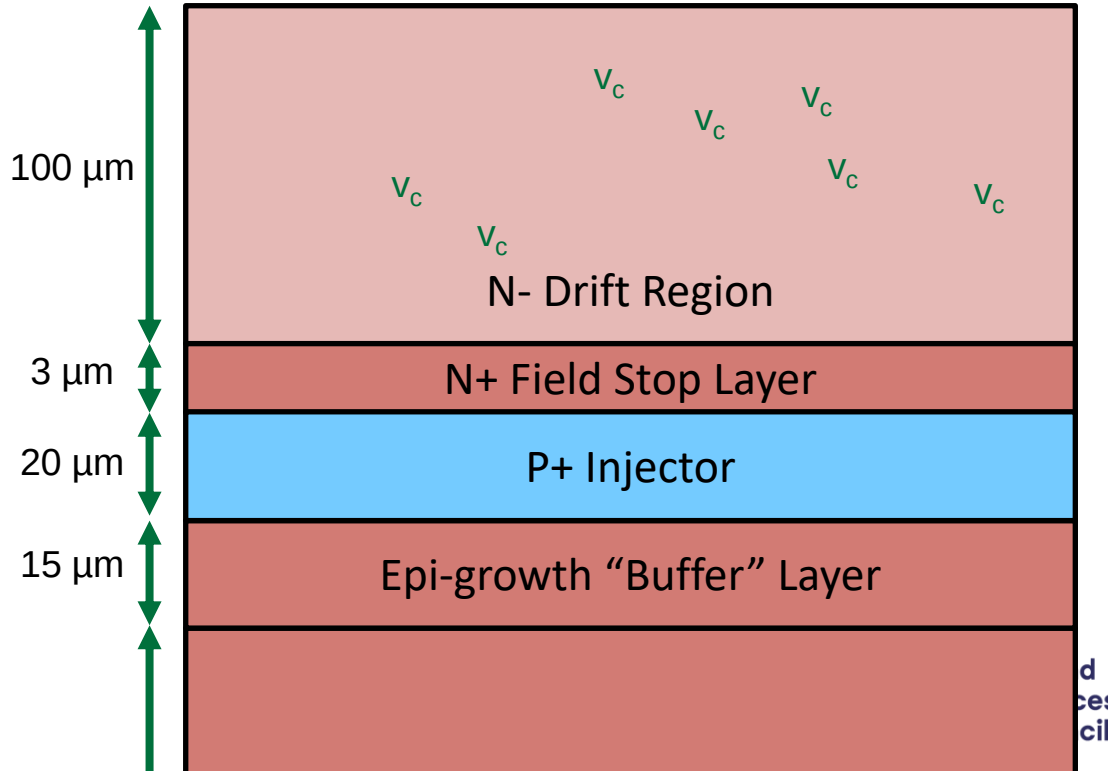
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*
2. ***High quality, high carrier lifetime SiC drift region***

The UPE2: SO Theme IGBT

- We therefore developed our own “Lifetime enhancement technique”.
- First, carbon was implanted into the surface
- Then driven through the drift region with a 4 hour anneal.

- Carrier lifetime is expected to improve from 1 µs to 3-4 µs, maximising the conductivity modulation of the 100 µm drift region.
- Wafers with and without the lifetime enhancement are being produced for benchmarking.



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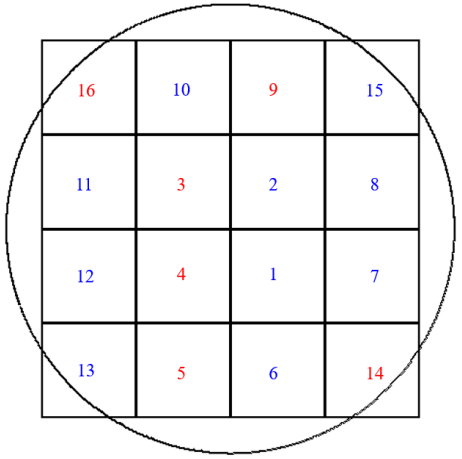
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

3. *Maximising device robustness and reliability*

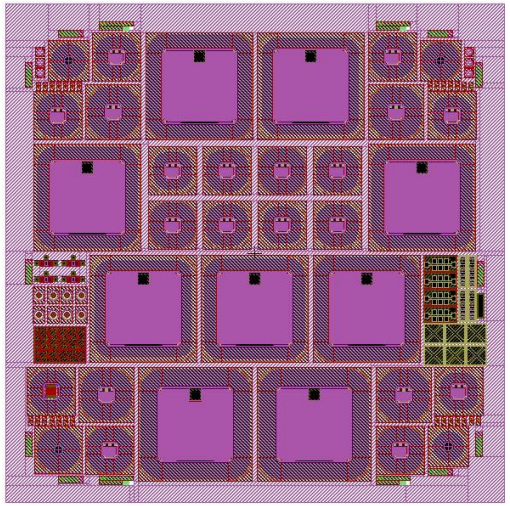
4. ***Optimising the frontside gate design***

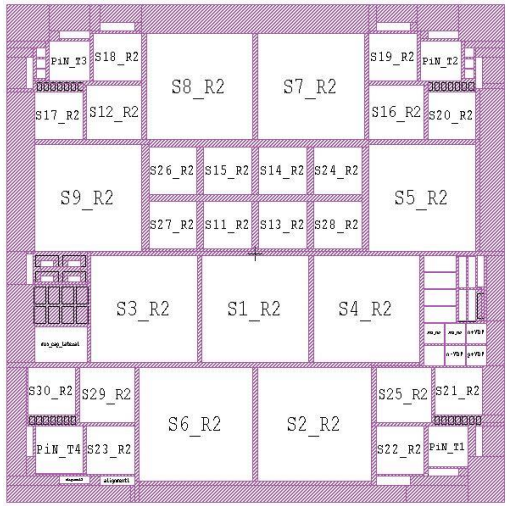
- Several iterations of device simulation led to a large matrix of design splits. These looked at various channel lengths, JFET widths, source contacts and termination designs.



"JTE" Termination samples
Novel Trench p-ring chips

- These were all embedded into a full 4" wafer process to develop over 1500 IGBTs (or MOSFETs) per wafer.





Size	Label	Channel Length	JFET Lj	P++/N++	Trench P ring	JTE
		1.5,2,3,5µm	0,3,4,5,6µm	Option 1,2,3		
Large	S1	2	4	1	T3	JTE6
	S2	2	4	1	T4	JTE5
	S3	2	4	1*	T1	JTE4
	S4	2	4	3	T2	JTE3
	S5	3	4	1	T3	JTE2
	S6	4	4	2	T4	JTE1
	S7	2	3	1*	T1	JTE4
	S8	2	5	1*	T2	JTE5
	S9	2	0	1	T3	JTE6
Small	S11	2	4	1	T3	JTE6
	S12	2	4	1	T4	JTE5
	S13	2	4	1	T1	JTE4
	S14	2	4	3	T2	JTE3
	S15	2	4	1	T3	JTE2
	S16	2	4	1*	T4	JTE1
	S17	5	6	1*	T3	JTE6
	S18	2	3	1*	T3	JTE6
	S19	2	5	1*	T3	JTE6
	S20	4	6	1*	T1	JTE5
	S21	3	4	1	T1	JTE1
	S22	3	4	1	T2	JTE2
	S23	3	4	1	T2	JTE3
	S24	2	4	2	T3	JTE6
	S25	2	4	2	T4	JTE5
	S26	1	4	3	T1	JTE4
	S27	1	4	3*	T2	JTE5
	S28	2	0	1	T3	JTE6
	S29	2	0	1	T4	JTE5
	S30 Thy	n/a	0	1	T3	JTE4

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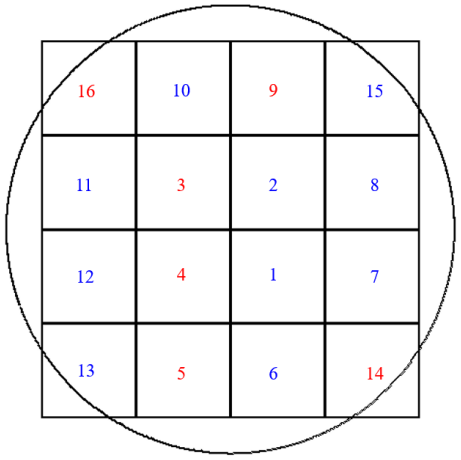
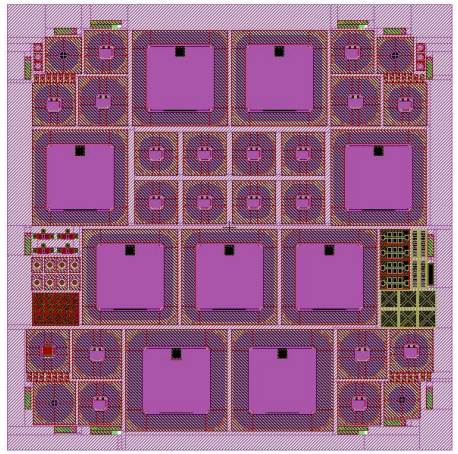
3. *Maximising device robustness and reliability*

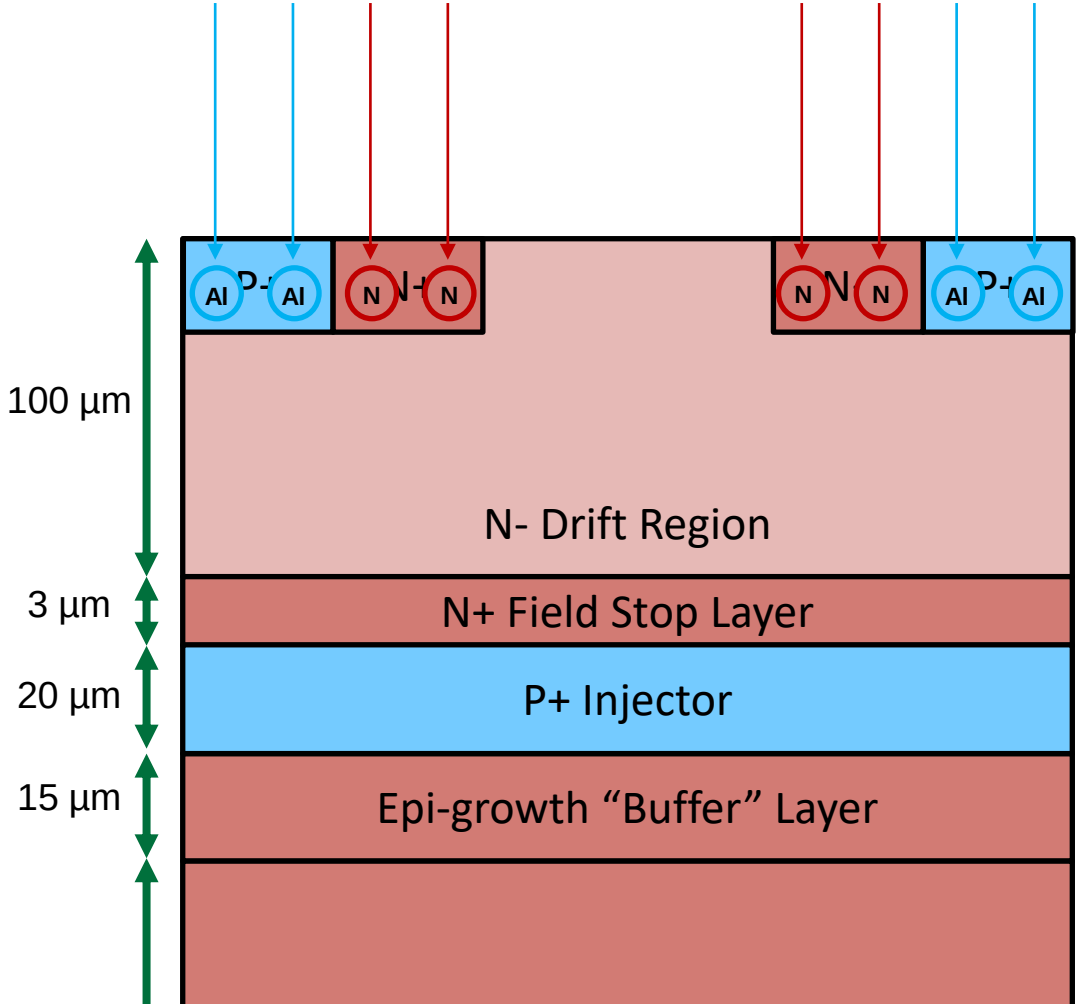
4. ***Optimising the frontside gate design***

- The first “front-side” fabrication step was to implant the P type and N type regions, across the full 4” wafer.
- This included the source contacts…





The UPE2: SO Theme IGBT



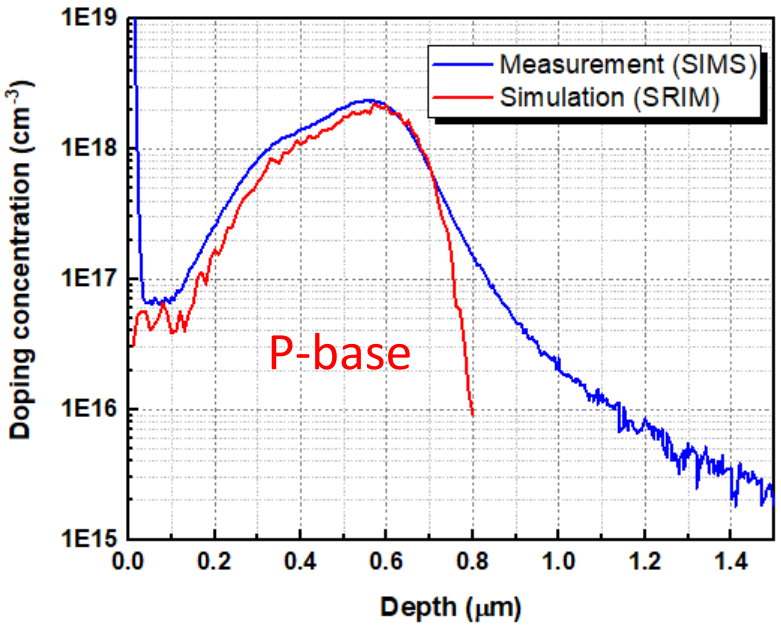
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

3. *Maximising device robustness and reliability*

4. *Optimising the frontside gate design*

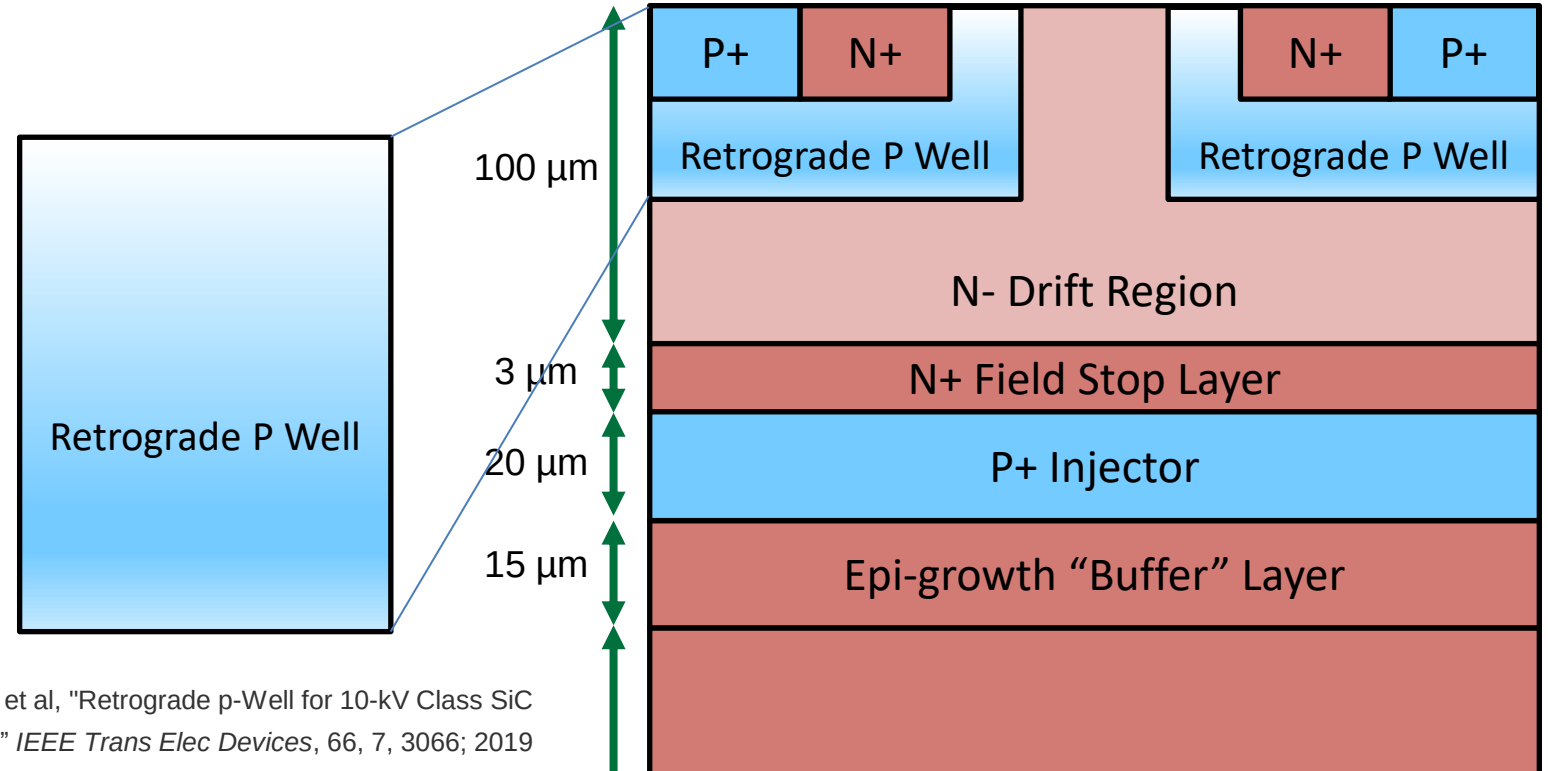
- The first “front-side” fabrication step was to implant the P type and N type regions, across the full 4” wafer.
- This included the source contacts…

  …and the P-well contacts.



The UPE2: SO Theme IGBT

The novel p-well was simulated to minimise switching losses and maximise the robustness of the IGBT to short circuit faults



Tiwari, et al, "Retrograde p-Well for 10-kV Class SiC IGBTs” *IEEE Trans Elec Devices*, 66, 7, 3066; 2019

EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

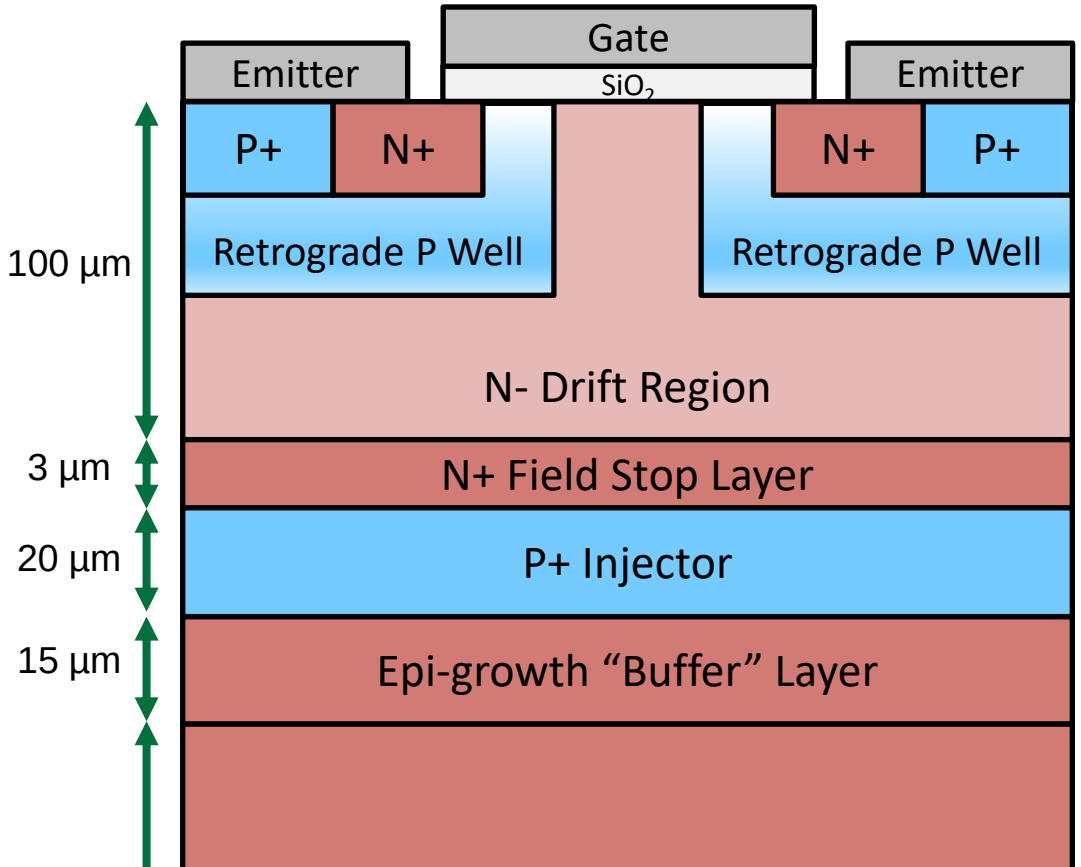
3. *Maximising device robustness and reliability*

4. ***Optimising the frontside gate design***

The UPE2: SO Theme IGBT

- The first “front-side” fabrication step was to implant the P type and N type regions, across the full 4” wafer.
- This included the source contacts…

  …and the P-well contacts.
- “Conventional” SiC MOS Gate processing follows to form the SiO_2 and metal region on the IGBT (or MOSFET) top surface.



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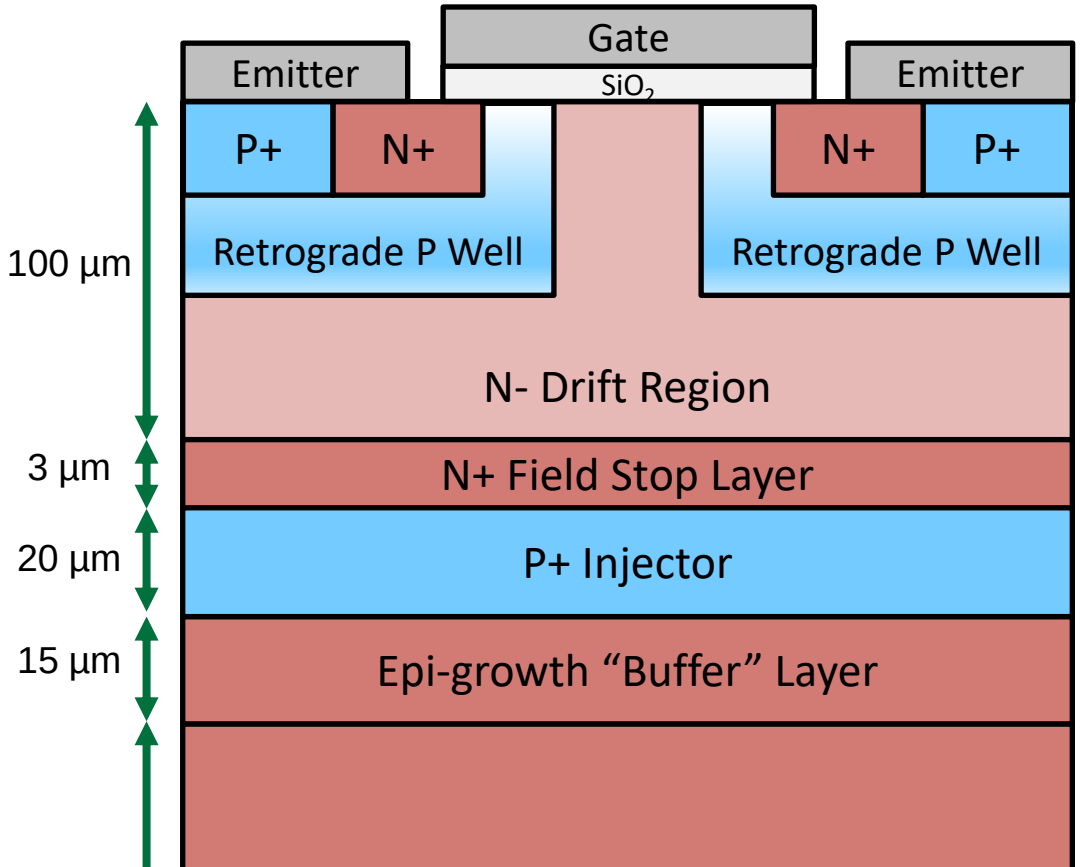
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*

- Until now, the processing has continued with the original 350 µm N+ substrate still remaining on the backside of the wafer.
- This retained the rigidity of the wafer during processing.

The UPE2: SO Theme IGBT



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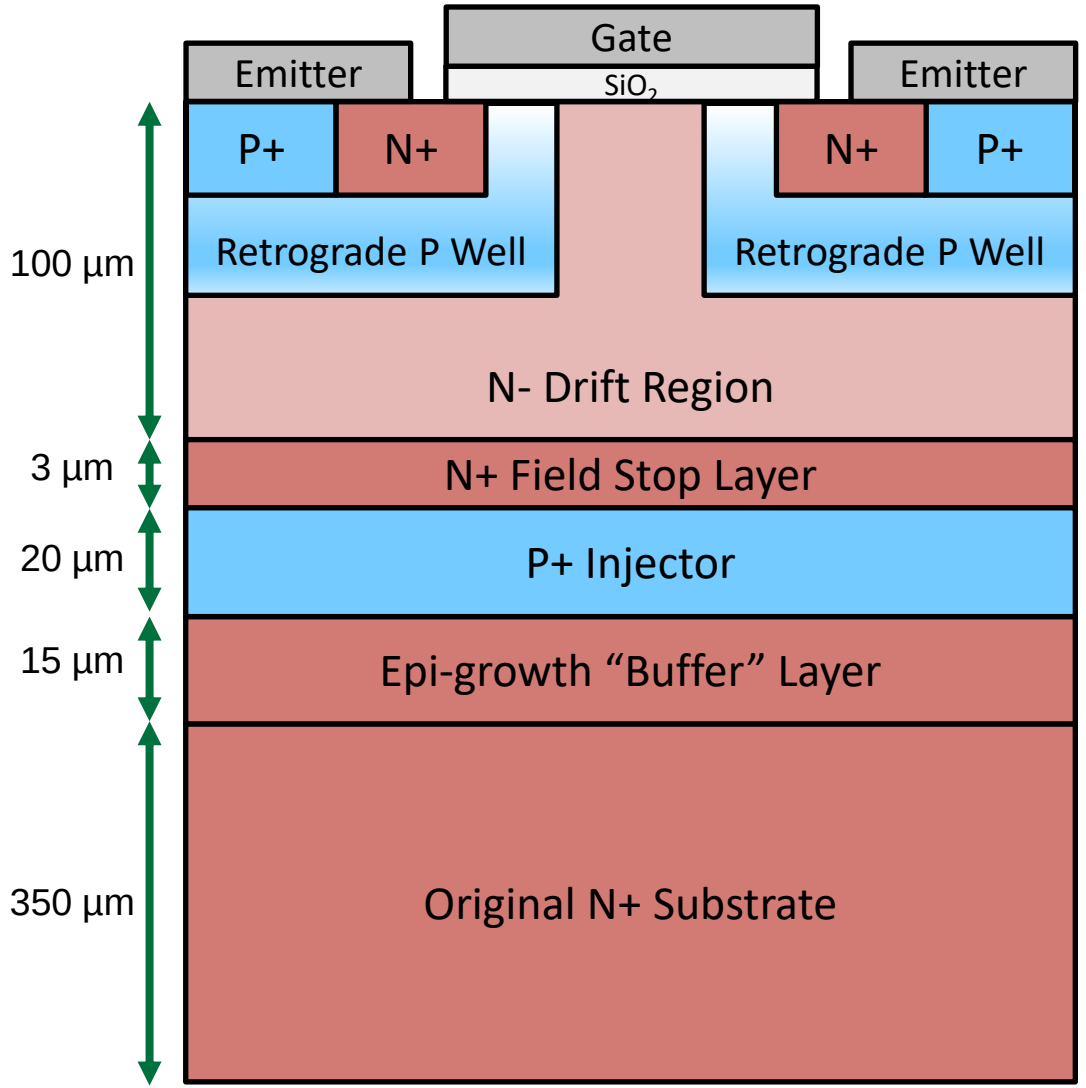
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*

- Until now, the processing has continued with the original 350 µm N+ substrate still remaining on the backside of the wafer.
- This retained the rigidity of the wafer during processing.
- Now, the substrate can be removed.

The UPE2: SO Theme IGBT



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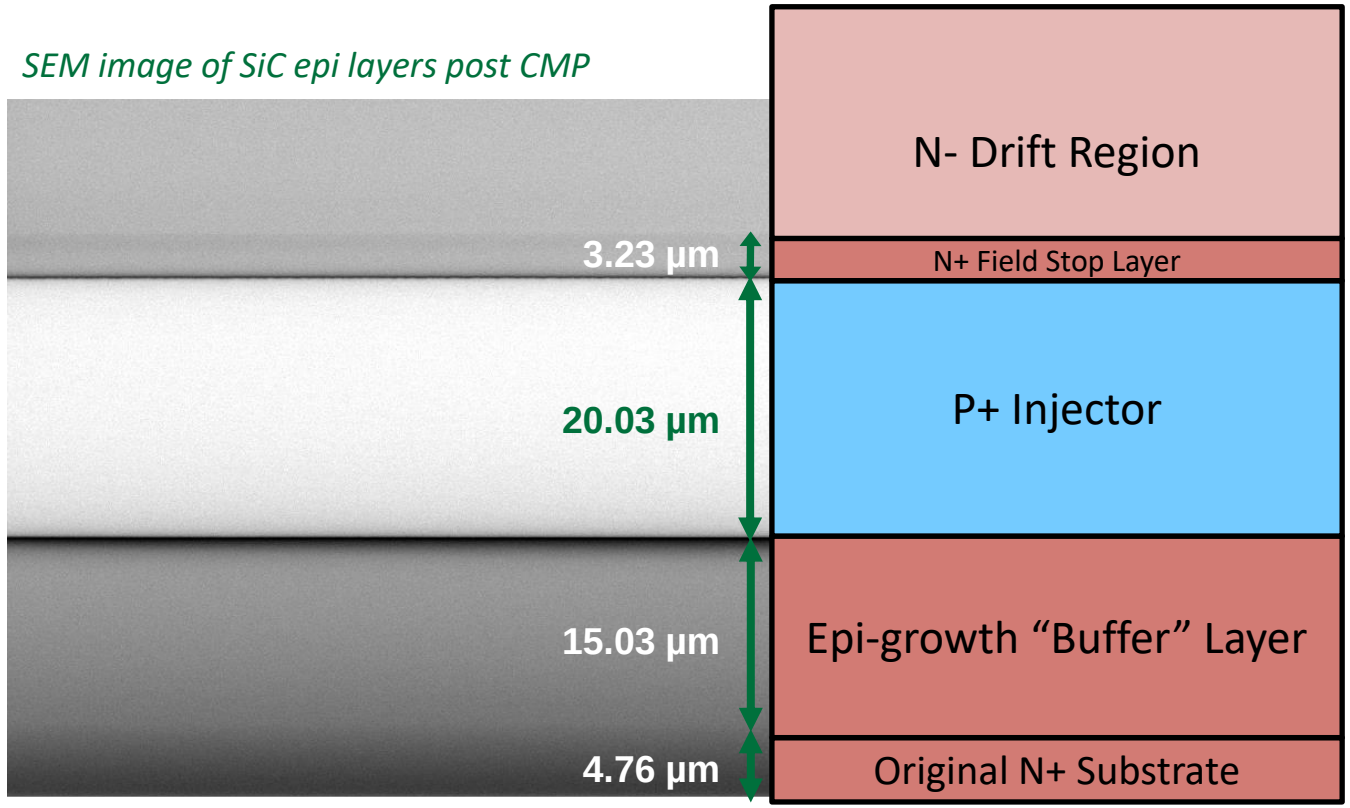
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

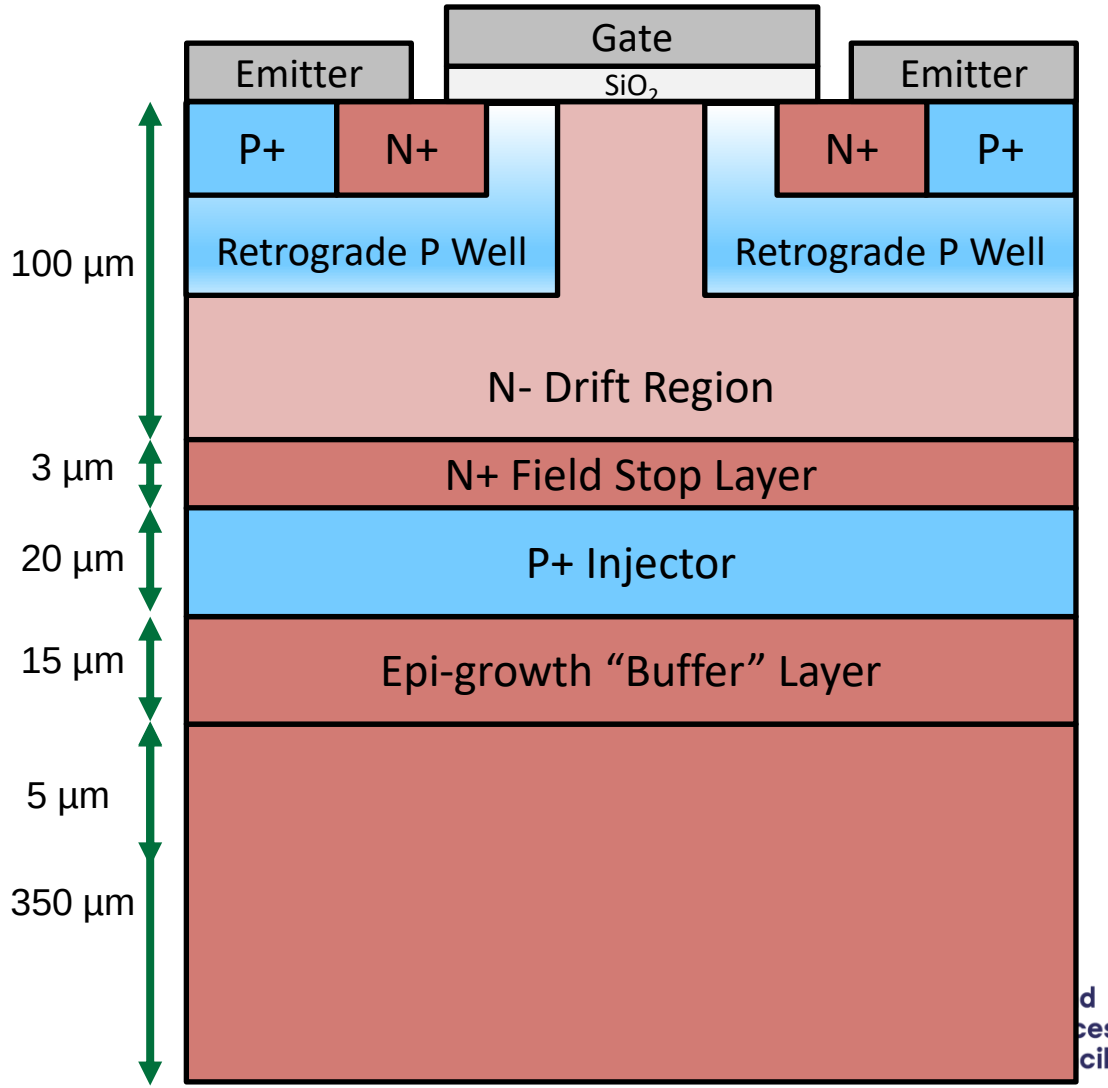
1. *Forming a P+ injector with only N+ Substrates available*

- The majority of the substrate can be removed via CMP polishing on the full wafer.
- This leaves a few microns of the substrate and epi buffer.

SEM image of SiC epi layers post CMP



The UPE2: SO Theme IGBT

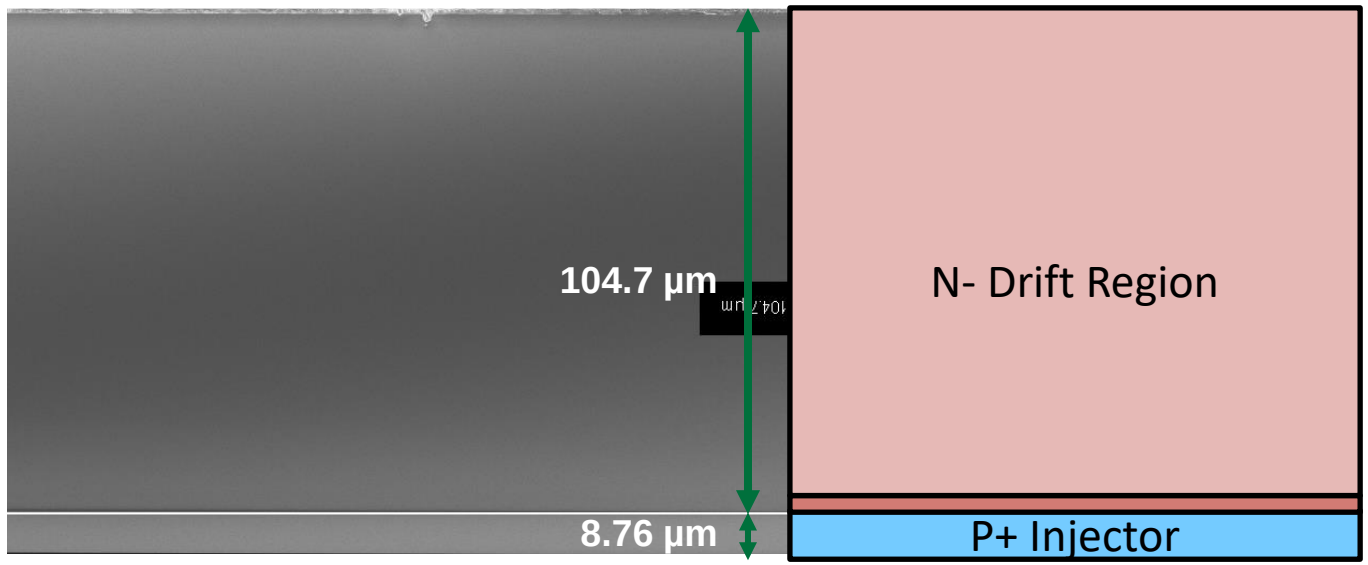


EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

1. *Forming a P+ injector with only N+ Substrates available*

- The rest of the substrate and the epi buffer layer can be removed in-house on individual chips using RIE/ICP etching
- The P+ injector is reduced to 9 µm

SEM image of SiC epi layers post RIE/ICP Etching



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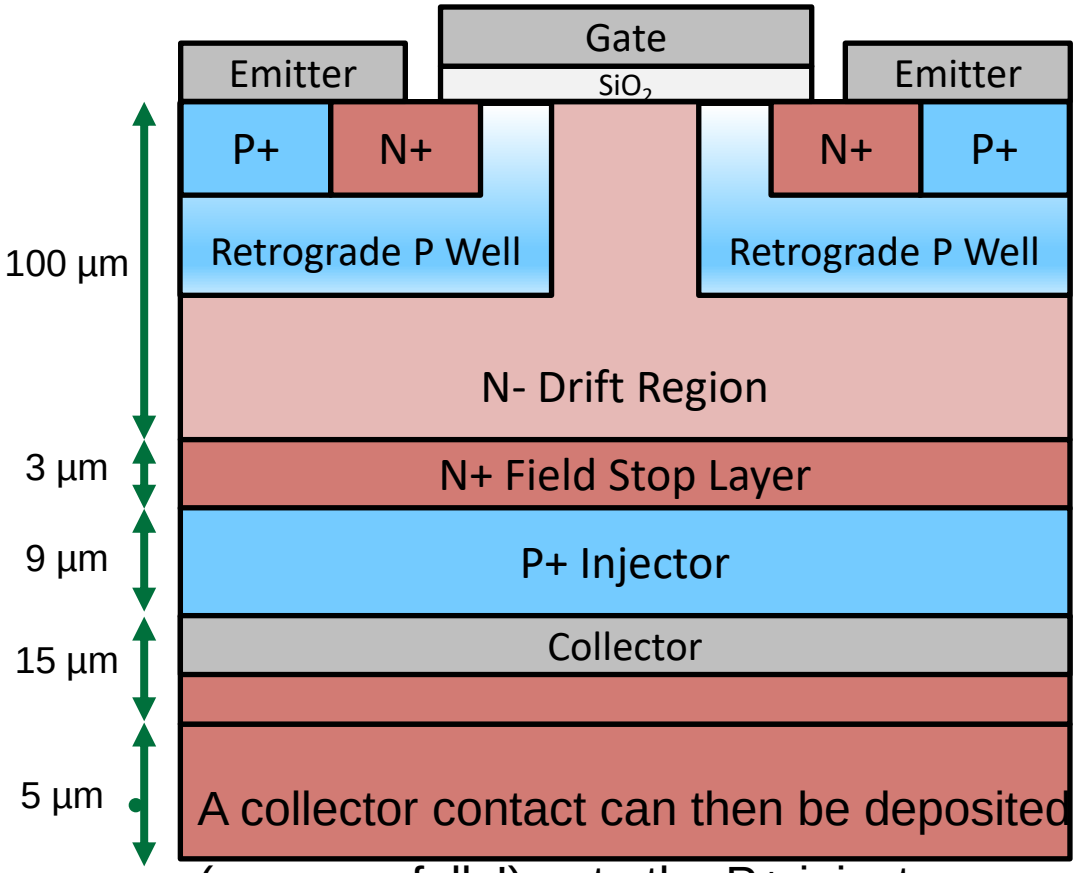

(very carefully!) onto the P+ injector.

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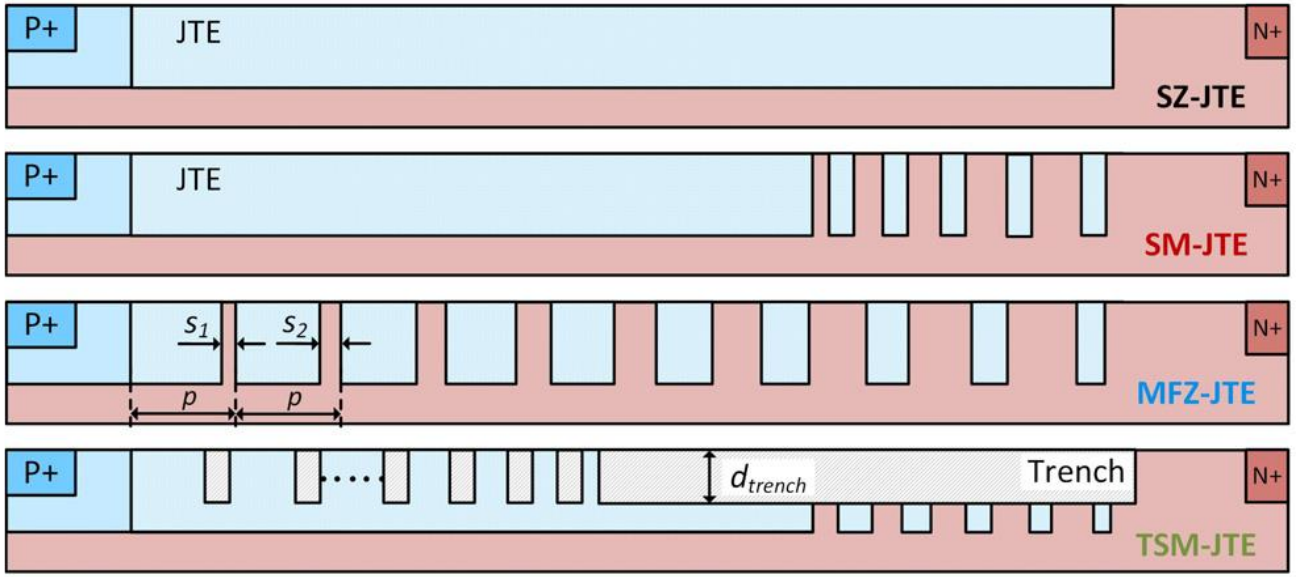
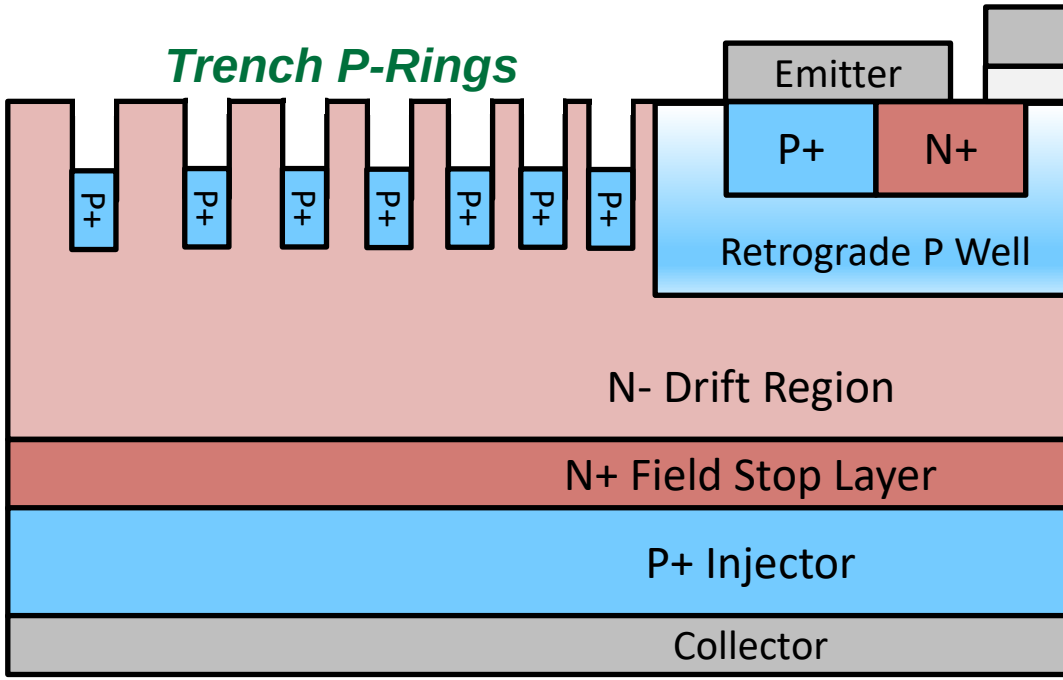
EPSRC CPE Switch Optimisation Theme: Innovation & Achievements

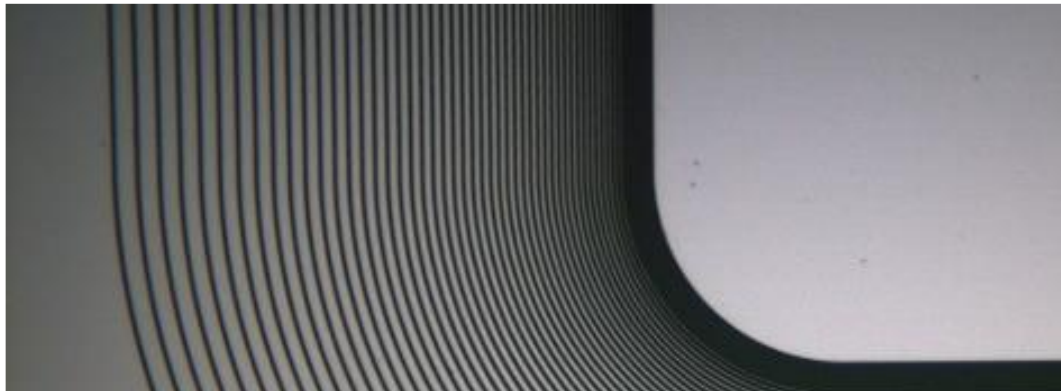
5. *Optimising the termination regions for 10 kV*

- Novel termination designs are required to achieve V_{BD}>10 kV
- Over 27 different designs are being trialled including:
  - P-rings and **Trench P-rings**, two-zone hybrid JTEs[1],
  - Our novel **Trench-Assisted Space-Modulated JTE**[2].



The UPE2: SO Theme IGBT





[1]S. Perkins *et al.*, "Optimal edge termination for high oxide reliability aiming 10kV SiC n-IGBTs," *2019 IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, 2019, pp. 358-363

[2]T. Dai et al, "A Compact Trench-Assisted Space-Modulated JTE Design for High-Voltage 4H-SiC Devices," IEEE Trans. Elec. Dev., 68, 3, 1162, 2021.

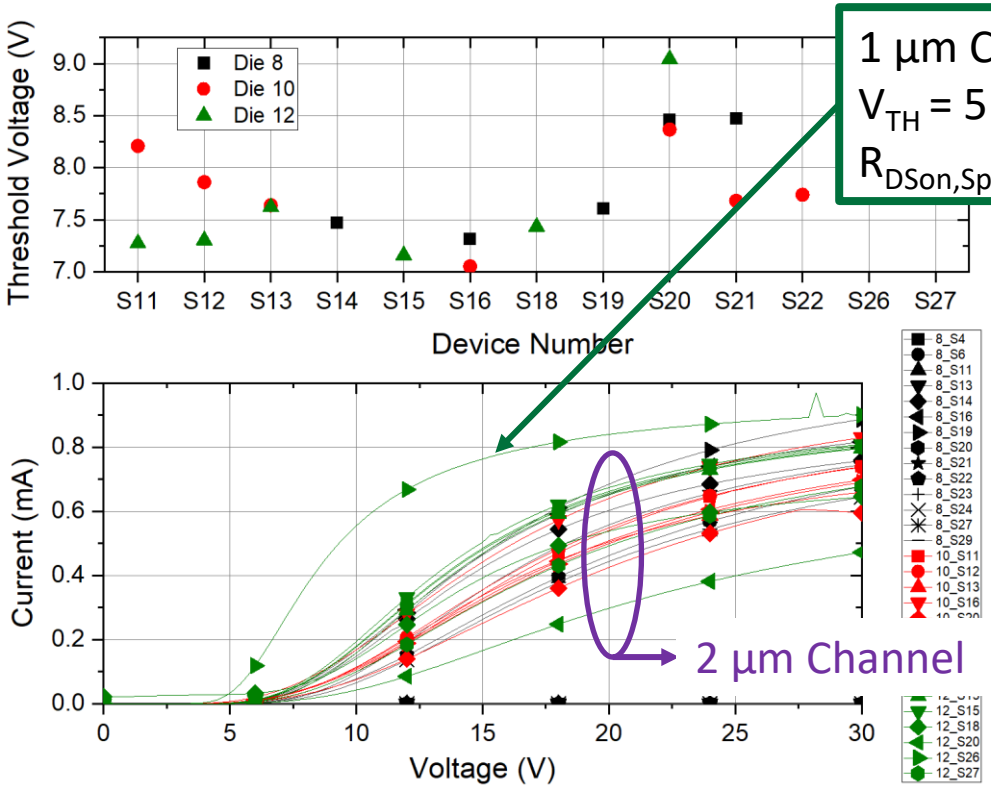
EPSRC CPE Switch Optimisation Theme: Contents

EPSRC CPE Switch Optimisation Theme: Results

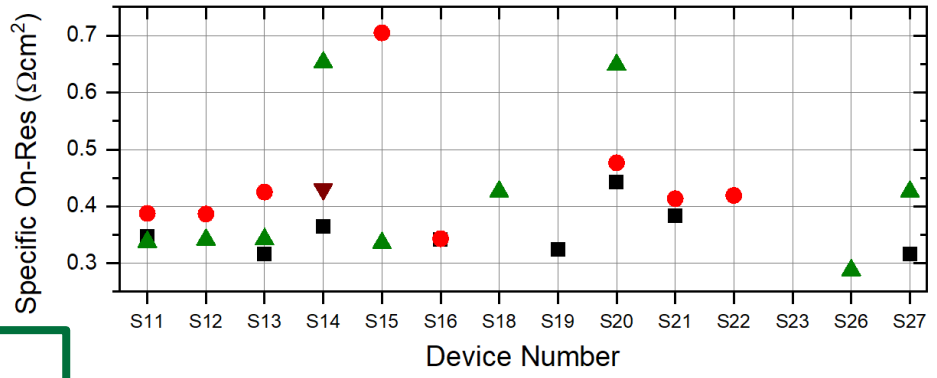
Do they work?!

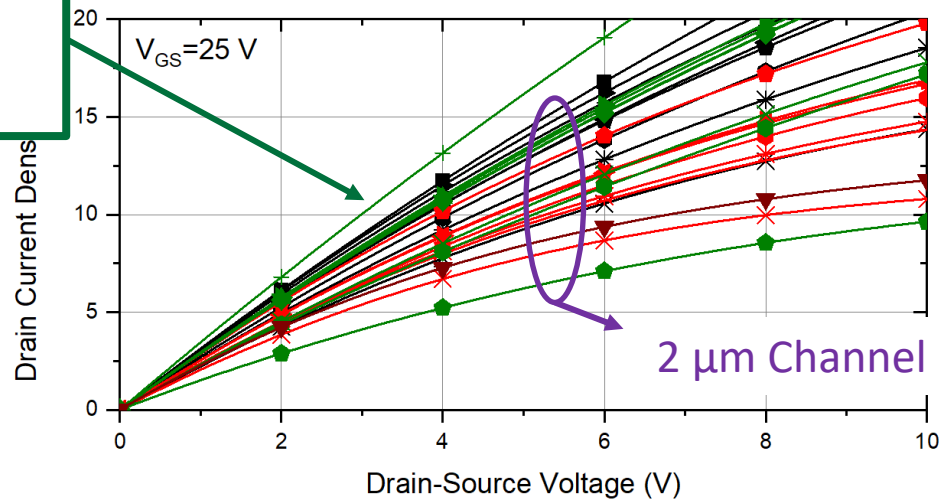
Yes! The early signs are good. The final IGBTs will be finished in Sept 2021, but we can reveal some early test results from Gen2. First the MOSFETS!

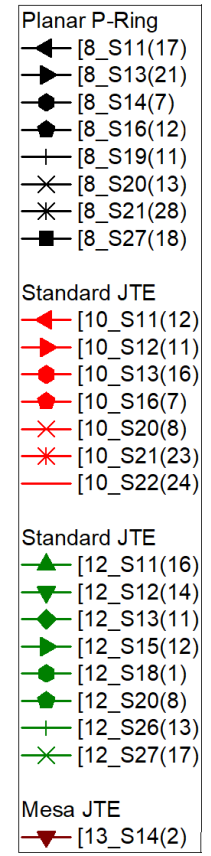
10 kV MOSFETs: Initial Transfer and Output Characteristics



1 µm Channel MOSFET:
V_{TH} = 5 V
$R_{DSon,Sp}$ = 288 mΩ-cm²







Transfer Characteristics show a **threshold voltage** of 5 – 8 V, depending on gate design.

Output Characteristics show an **On-resistance** of 0.3-0.45 Ω-cm² depending on gate design.

EPSRC CPE Switch Optimisation Theme: Results

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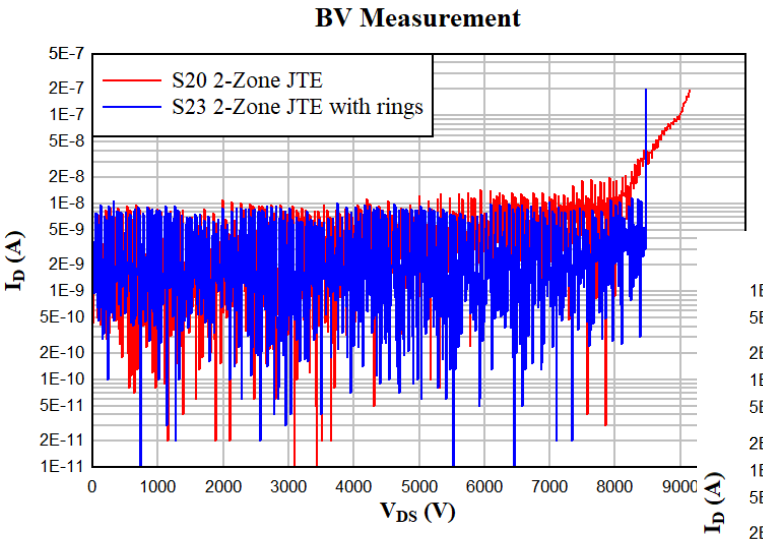
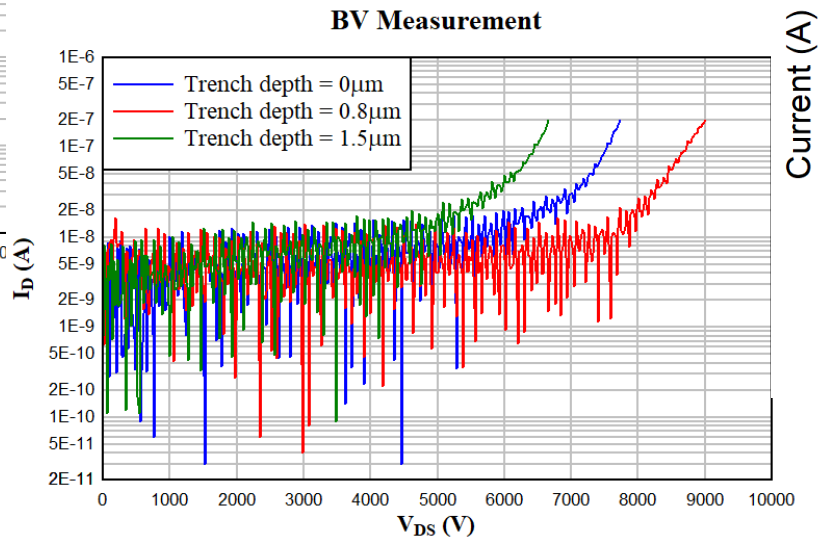
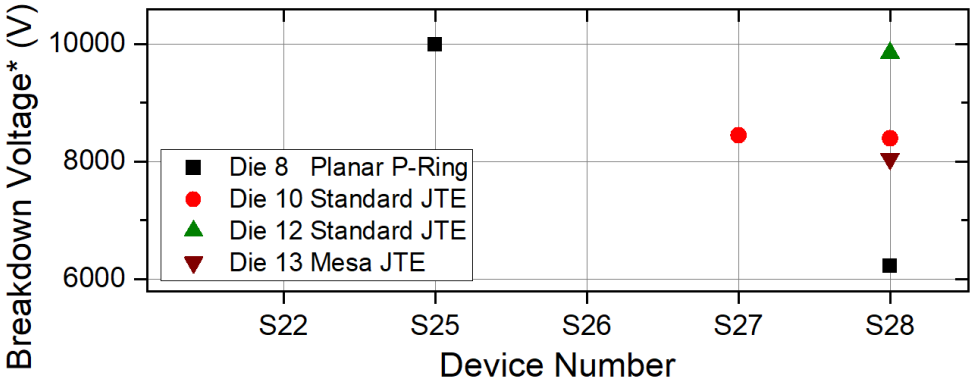


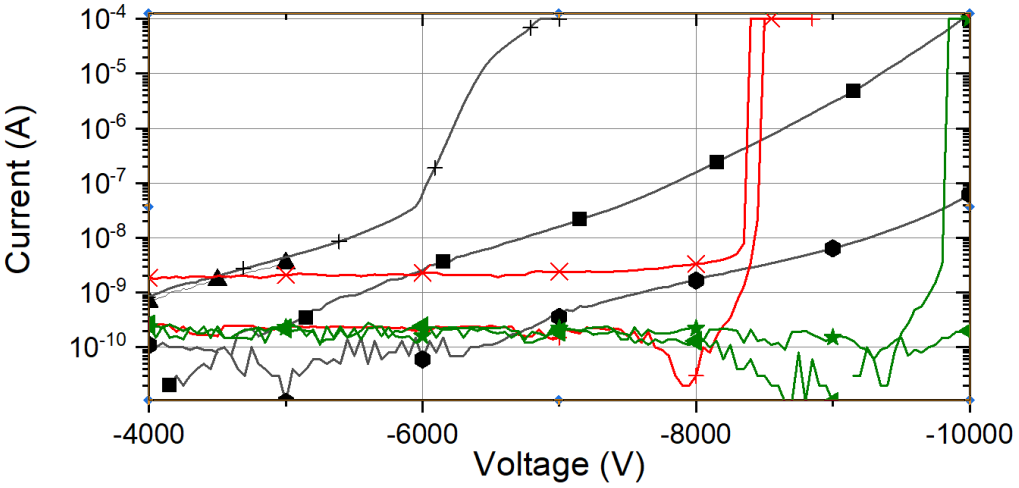
2-Zone JTE Proof of Concept



Trench P-ring Proof of Concept

10 kV MOSFETs: Reverse Characteristics





Reverse Characteristics show that the same devices can reach a **breakdown voltage** of 10 kV depending on gate design.

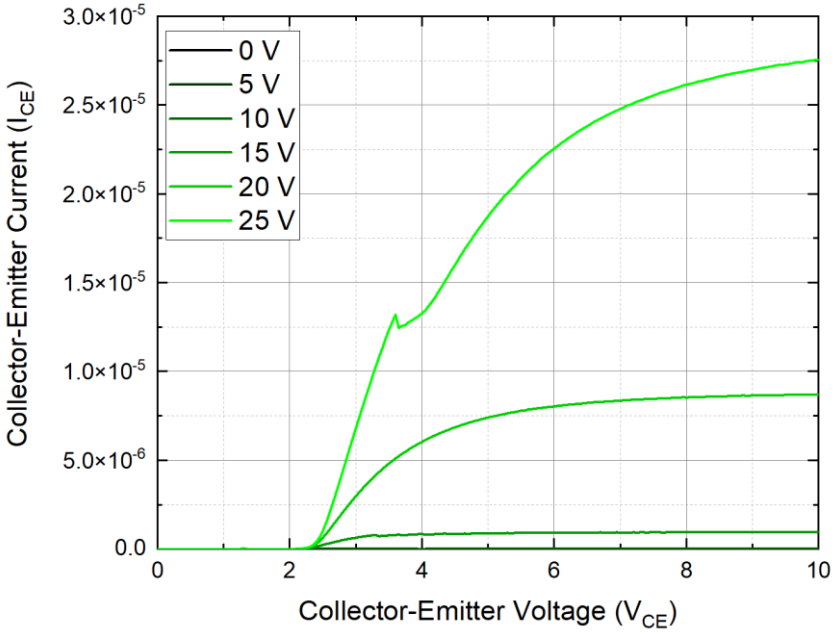
POWER ELECTRONICSUK Underpinning Research

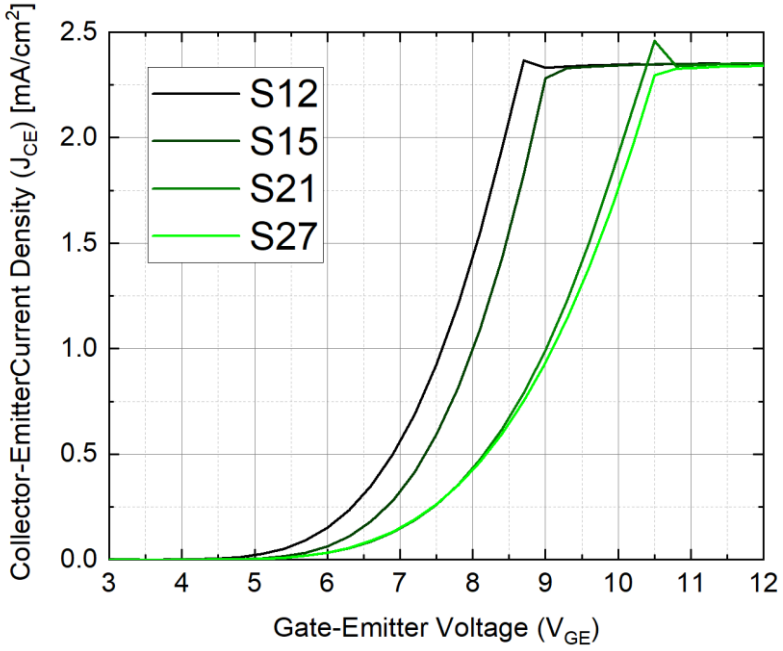
EPSRC CPE Switch Optimisation Theme: Results

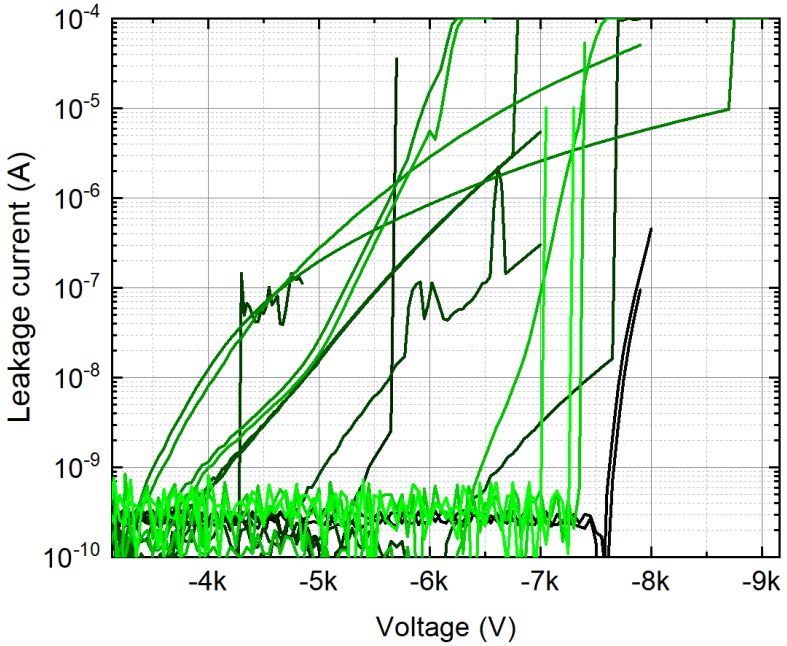
Do they work?!

Some early IGBT results…

10 kV IGBTs: Initial Transfer and Output Characteristics







Output Characteristics from small area test cells show the typical **2.5 V built in potential**

Transfer Characteristics show a **threshold voltage of 6-8 V.**

Reverse Characteristics show potential, but are a work in progress!

EPSRC CPE Switch Optimisation Theme: Summary

Switch Optimisation Theme: Maximising the potential of SiC

- Begun in 2018, the goal of the Switch Optimisation Theme was to develop the SiC devices of tomorrow, IGBTs and MOSFETs rated to 10 kV.
- Over two design and development processes, a number of novel processes have been achieved:
  - A design process to produce and compare 1500 MOSFETs and IGBTs
  - A lifetime enhancement technique
  - A new retrograde IGBT gate design aimed at maximising short circuit robustness
  - A number of innovative termination structures.
- SiC MOSFET results already show we have developed a 10kV device capable of 288 mΩ-cm^2.
- Work continues to finish the IGBT devices in Q3 2021, including maximising their V_{BD}