Reliability and Health Management Research Activity

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Power Semiconductor Devices			**Reliability of Power Modules**		
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High Frequency Power Electronics			**Condition and Health Monitoring**		

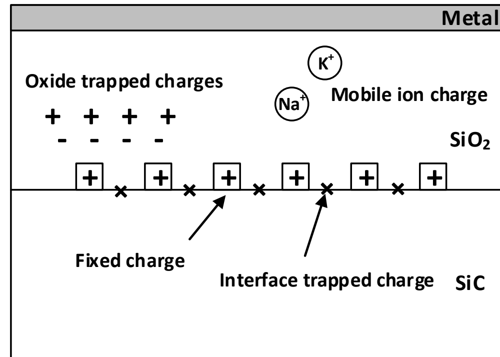
CONTENTS/OUTLINE

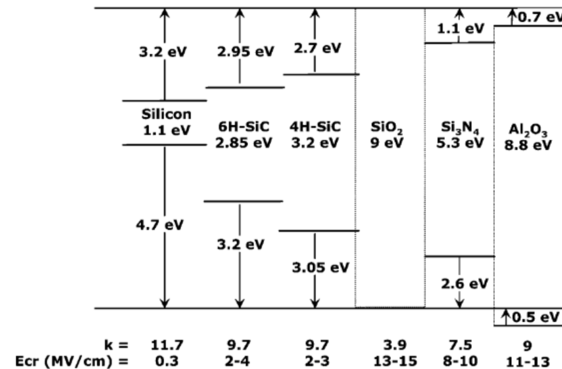
- Reliability/Protection of Gate Oxides in SiC MOSFETs
  - Introduction to oxide reliability
  - Bias Temperature Instability
  - 3rd Quadrant Technique for BTI Characterization
  - Current source/Voltage source gate driving
  - V_{GS} de-rating in SiC MOSFETs

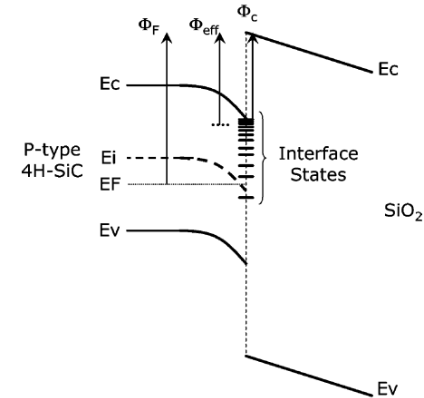
Introduction to Oxide Reliability

- Gate oxide has been/was a reliability concern in SiC MOSFETs
- Semiconductor-oxide interface
  - SiC/SiO_2 is not Si/SiO_2 (more complex)
  - Wider bandgap of SiC (3.3 eV) and narrower band offsets to the dielectric
  - Existence of carbon
  - Interface and near oxide trap density D_{it} in SiC/SiO_2 is 100x D_{it} in Si/SiO_2

T. Aichinger, et al. "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability,* vol. 80, pp. 68-78, 2018.





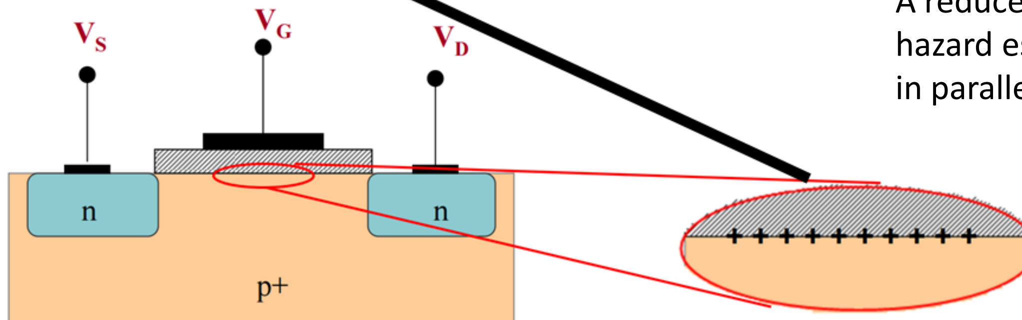


Introduction to Oxide Reliability

- The oxide interface between SiC and SiO_2 is not as reliable as that between Si and SiO_2.

- Fixed oxide and interface traps capture electrons during positive bias and holes during negative bias. This causes a shift in V_{TH} which is detrimental to device reliability.

$$V_{TH} = \left(\emptyset_{MS} - \frac{Q_f}{C_{OX}}\right) + 2\frac{kT}{q}ln\left(\frac{N_A}{n_i}\right) + \frac{qN_A}{C_{OX}}\sqrt{\frac{4\varepsilon}{qN_A}\frac{kT}{q}ln\left(\frac{N_A}{n_i}\right)}$$



A reduced threshold voltage is a circuit hazard especially if it occurs unevenly in parallel connected devices.

Simplified MOSFET diagram showing MOS interface

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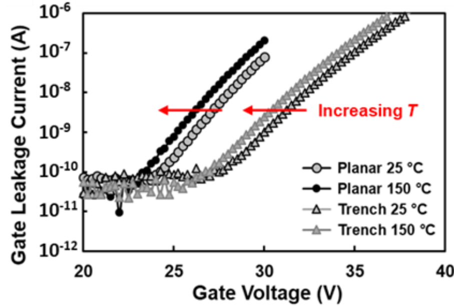
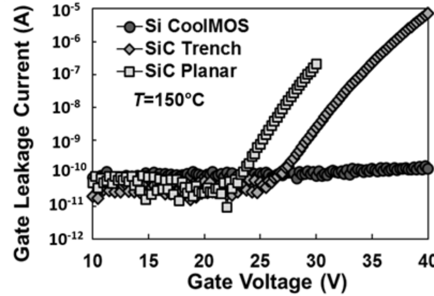
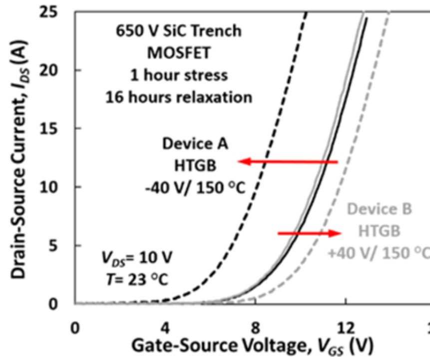
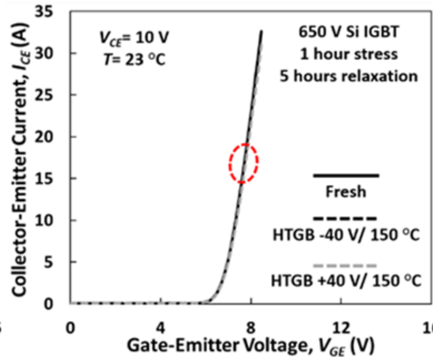
Introduction to Oxide Reliability





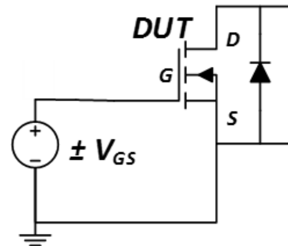
Gate Oxide Breakdown characteristics for Si/SiC MOSFETs

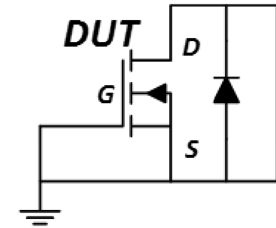




SiC and IGBT Gate Transfer characteristics before and after BTI Stressing

- Accelerated stress tests are performed to investigate the extent of BTI in power MOSFETs/IGBTs
- Stress tests can be with positive or negative gate voltages





J. O. Gonzalez and O. Alatise, 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 837-844.

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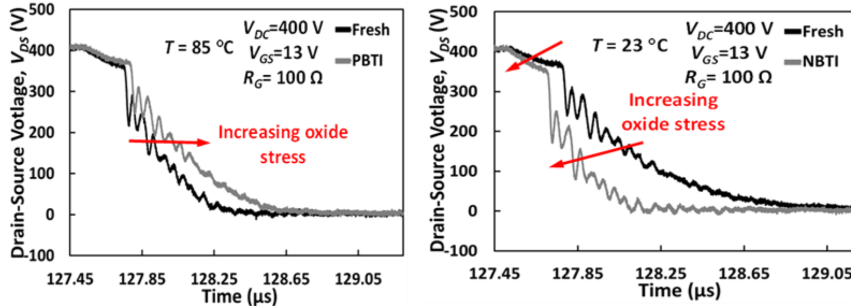
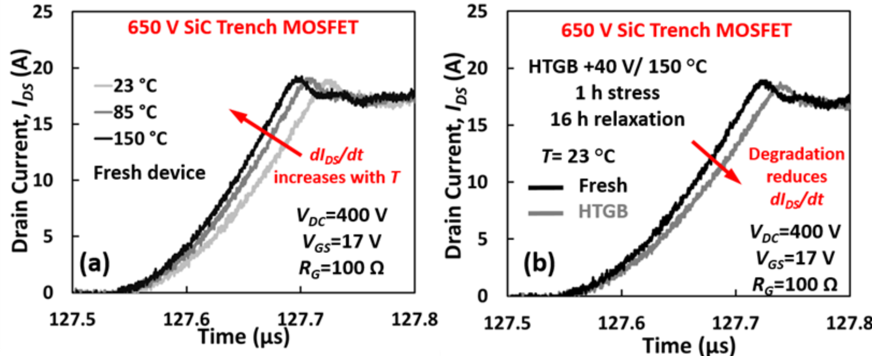
Impact of BTI on Switching Transients



Impact of NBTI and PBTI on drain voltage transients in SiC MOSFETs



Impact of NBTI and PBTI on drain current transients in SiC MOSFETs

- The change in V_{TH} affects the turn-ON and turn-OFF V_{DS} and I_{DS} transients.
- PBTI causes delayed transients during turn-ON due to increase in V_{TH}.
- NBTI causes accelerated transients during turn-ON due to reduction in V_{TH}.

$$\frac{dI_{DS}}{dt} = \frac{\beta V_{GG}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS} + C_{GD})}$$

$$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{GP}}{R_G C_{GD}}$$

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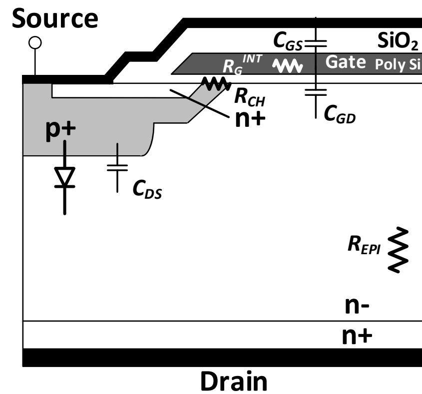
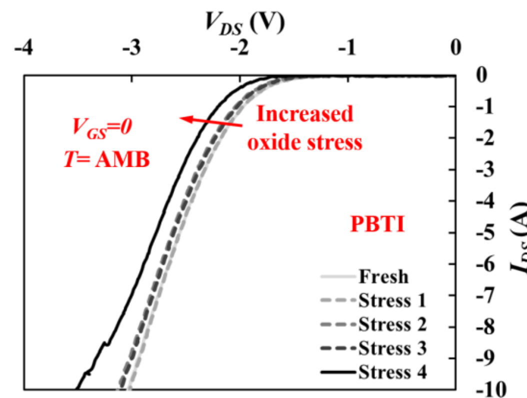
Using 3rd Quadrant Characteristics for BTI Characterisation

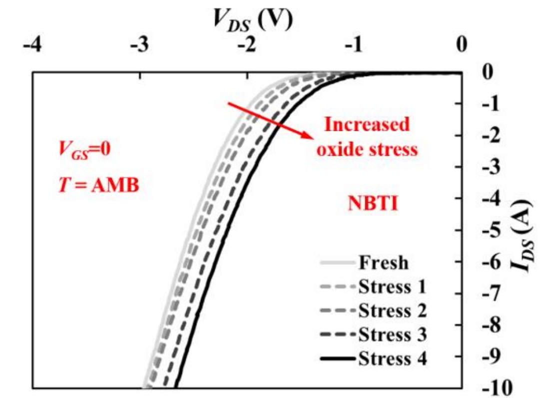
J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

- Body diode voltage – 3rd quadrant characteristics
  - Current flowing through the channel due to partial turn-ON during reverse conduction when V_{GS}=0



MOSFET with Body diode





Impact of NBTI and PBTI on 3RD Quadrant characteristics in SiC MOSFETs

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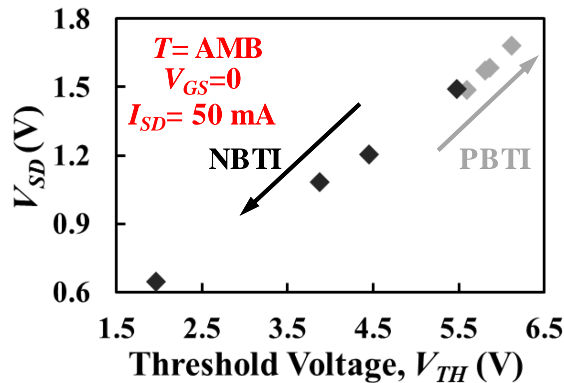
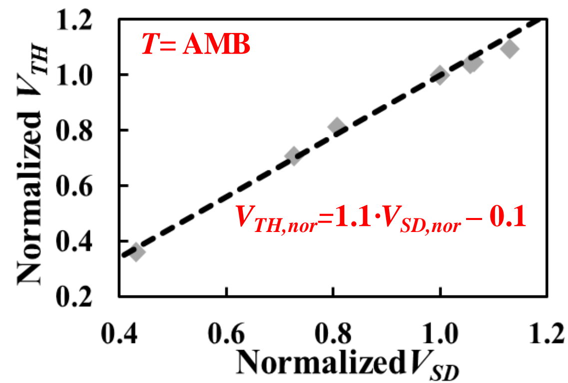
Using 3rd Quadrant Characteristics for BTI Characterisation

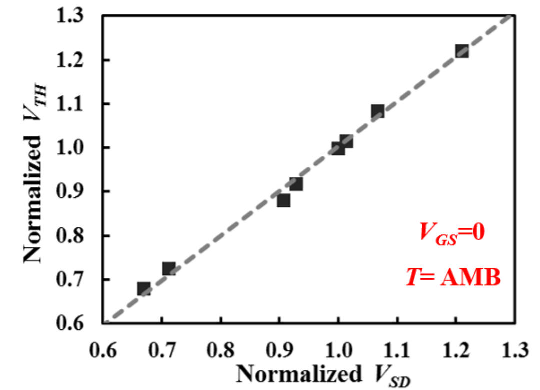
- Novel methodology for BTI characterization
  - Using the body diode voltage when V_{GS}=0
  - Similar to the use of V_{SD} as temperature sensor, but for detecting oxide degradation/V_{TH} shifts.
  - Calibration required. Using accelerated stress tests.

J. O. Gonzalez, O. Alatise and P. Mawby, "Non-Intrusive Methodologies for Characterization of Bias Temperature Instability in SiC Power MOSFETs," IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-10

J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,







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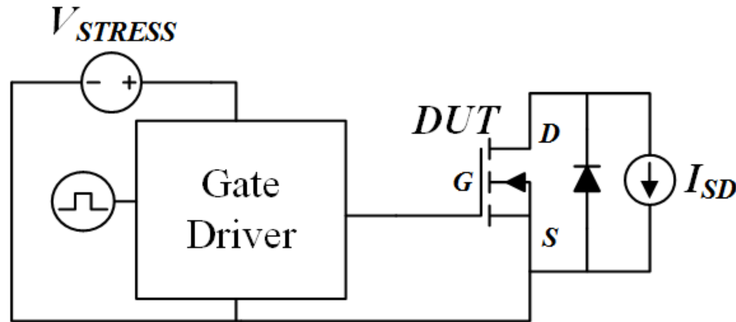
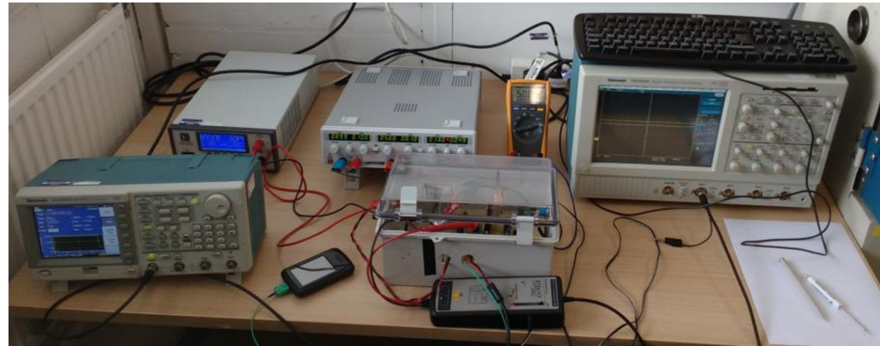
Using 3rd Quadrant Characteristics for BTI Characterisation

J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

- Circuit
  - Gate driver is used to apply stress voltage to the gate
  - Constant current source: low sensing current I_{SD} flowing in the source-drain direction





Experimental set-up for characterising BTI using 3rd quadrant characteristics

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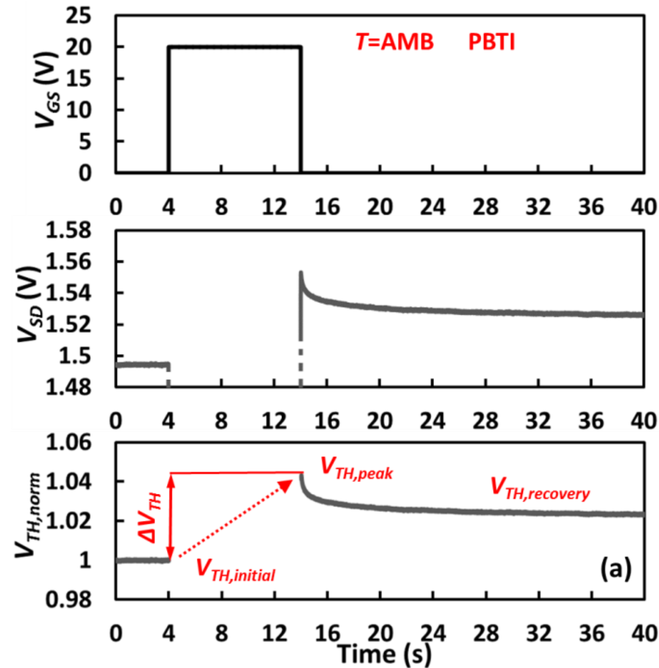
Using 3rd Quadrant Characteristics for BTI Characterisation

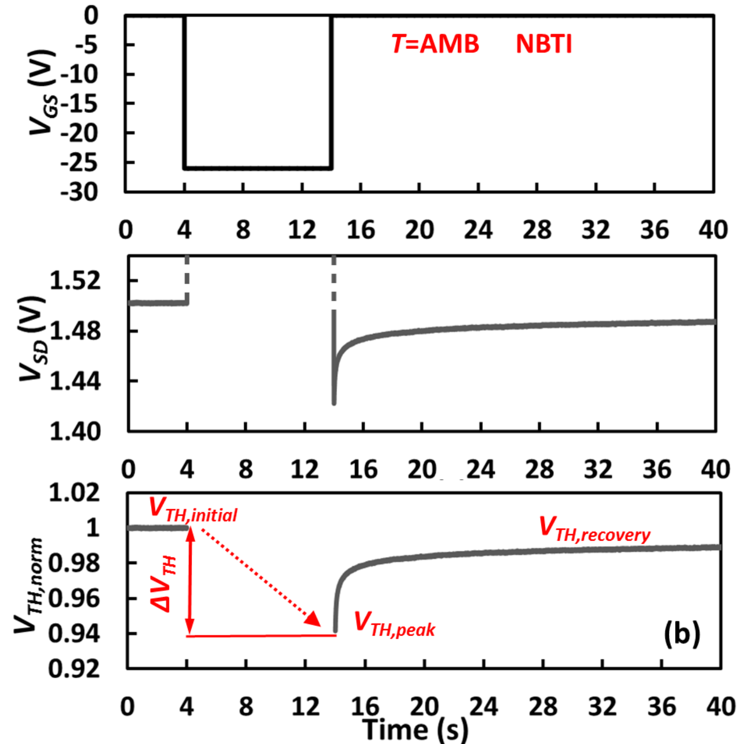


V_{GS}, V_{SD} and V_{TH} during stress and recovery for PBTI

- PBTI evaluation
  - Pre-stress phase (V_{GS}=0 V): The current flows through the body diode and channel. I_{SD}= 50 mA , $V_{TH,initial}$
  - Stress phase (V_{GS}=20 V): The current flows through channel. Device is ON.
  - Recovery phase (V_{GS}=0 V): The current flows through the body diode and channel. $V_{TH,peak}$ and $V_{TH,recovery}$

J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018.

Using 3rd Quadrant Characteristics for BTI Characterisation



V_{GS}, V_{SD} and V_{TH} during stress and recovery for NBTI

- NBTI evaluation
  - Pre-stress phase (V_{GS}=0 V): The current flows through the body diode and channel. I_{SD}= 50 mA , $V_{TH,initial}$
  - Stress phase (V_{GS}=-26 V): The current flows through body diode only. SiC PN junction voltage
  - Recovery phase (V_{GS}=0 V): The current flows through the body diode and channel. $V_{TH,peak}$ and $V_{TH,recovery}$

J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018.

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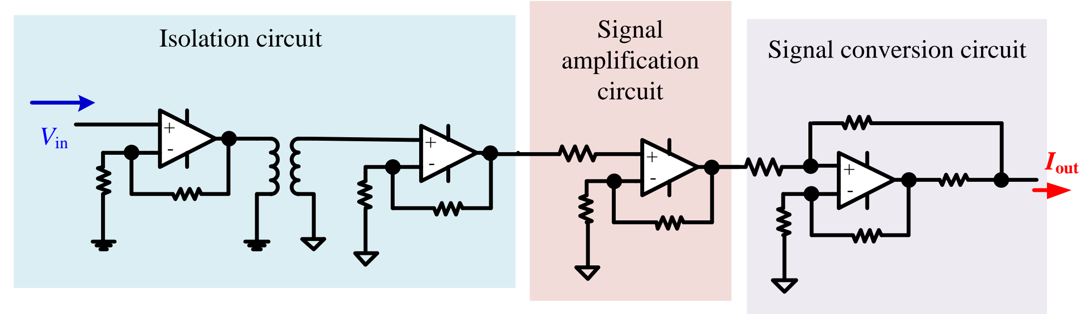
A Controllable Current Source Gate Driver for SiC MOSFETs

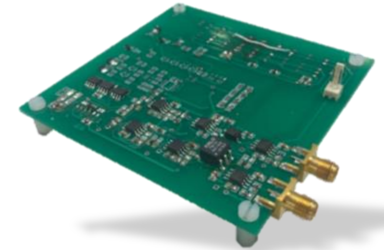
- The gate driver consists of 3 parts: signal isolation, signal amplification and signal conversion.
- The output current follows the shape of the input voltage signal.
- The input voltage signal can be programmed and generated by the DSP control system.



Schematic of the proposed gate driver

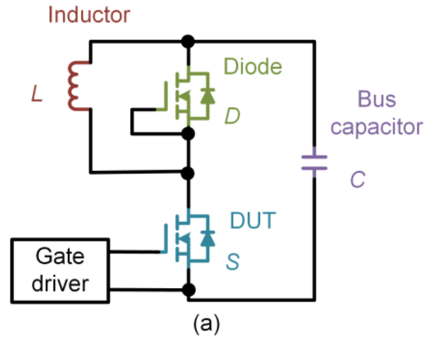
Parameters	Value
Output voltage range	-5V~15V
Output current range	0~200mA
Time step	13.3ns ~ 10us

Performance of the prototype

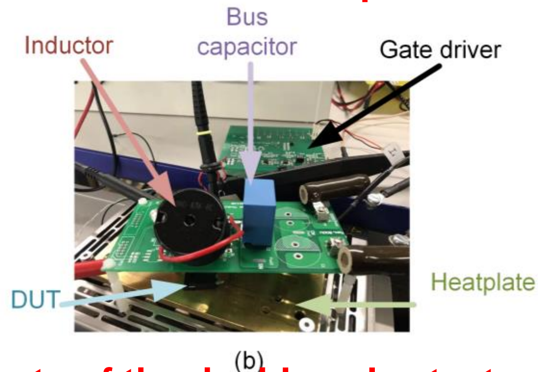


Picture of the prototype

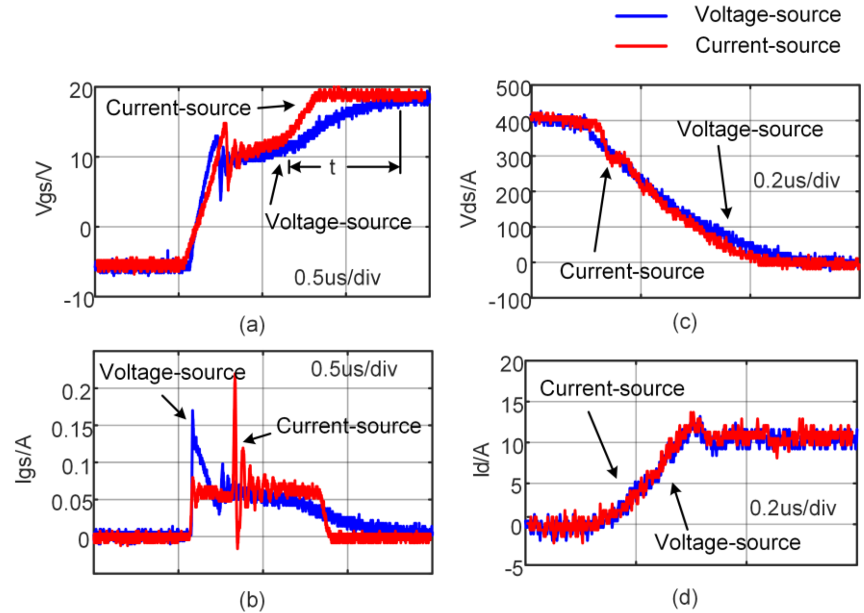
A Controllable Current Source Gate Driver for SiC MOSFETs



(a) schematic of the double pulse test set up



(b) photo of the double pulse test set up



A comparison of current source and voltage source gate driver. Test condition: V_{DS} = 400V, I_{DS} = 10A, Temperature = 25°C, I_{gs} = 60mA (for current source gate driver), R_g = 160Ω (for voltage source gate driver). (a) gate voltage comparison; (b) gate current comparison; (c) dV/dt comparison; (d) dI/dt comparison.

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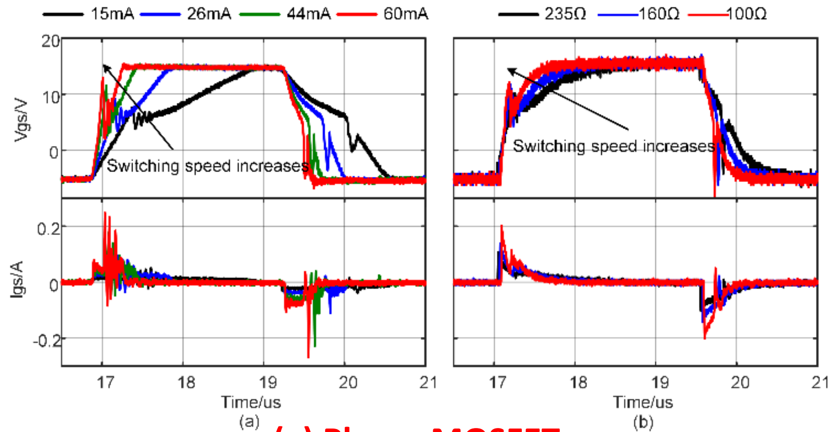
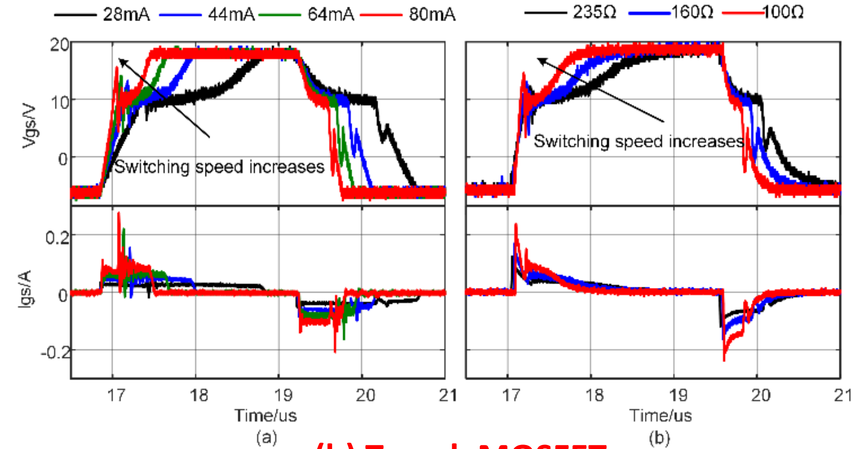
Current Source vs Voltage Source Gate Drivers

- Higher gate current increases the switching speed of the device but introduces higher oscillation on both the gate voltage and gate current.
- Planar SiC MOSFETs have faster turn-on and turn off transients compared to trench counterparts, due to the smaller gate-source capacitance.
- CSG introduces lower switching time compared to VSG.



(a) Planar MOSFETs



(b) Trench MOSFETs

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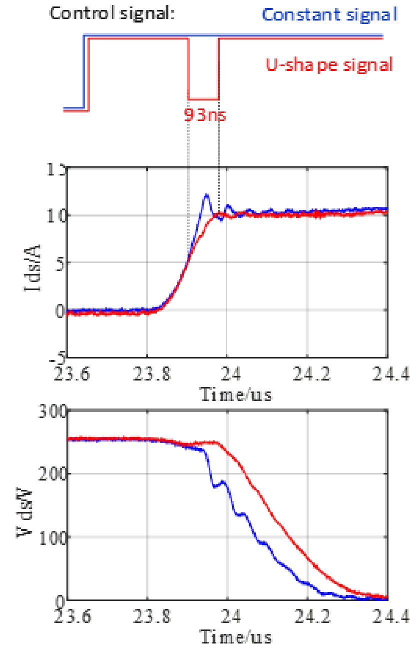
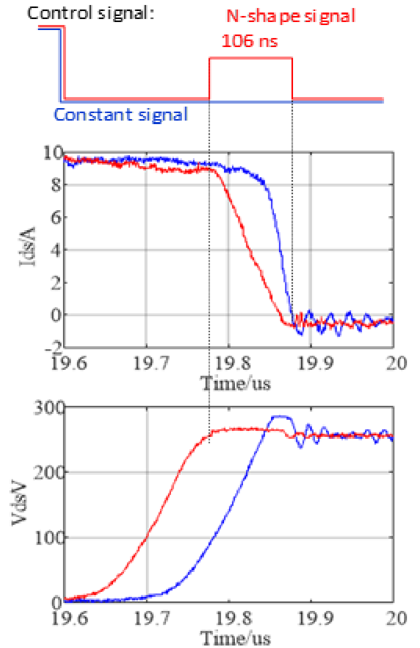
Current Source vs Voltage Source Gate Drivers

- U-shape and N-shape gate driving signals are proposed for the optimization of turn-on and turn-off transient.
- Conventional method reduces overshoots by increasing gate resistor, resulting in higher losses.
- Compared with conventional method, the proposed active gate driving signals have better performance in suppressing the overshoots without jeopardizing switching losses.

Switching performance	Turn-on loss	Turn-off loss	Current overshoot	Voltage overshoot
No suppression	0.36mJ	0.24mJ	1.92A	28V
Convention suppression method	0.86mJ	0.40mJ	1.12A	19V
Proposed suppression method	0.62mJ	0.30mJ	0.40A	11V



(a) Turn-on



(b) Turn-off

Prof Volker Pickert, Newcastle University

A Novel Method for Measuring V_{TH} using CSG Drivers

- The proposed method consists of 2 working modes: operating mode and measuring mode.
- In operating mode, S is turned-off. DUT works normally.
- In measuring mode, S is turned-on. The gate and drain of DUT are shorted. CSG generates constant current. The gate voltage is clamped at threshold voltage.
- The benefit of the proposed method is the low requirement for a sampling circuit.

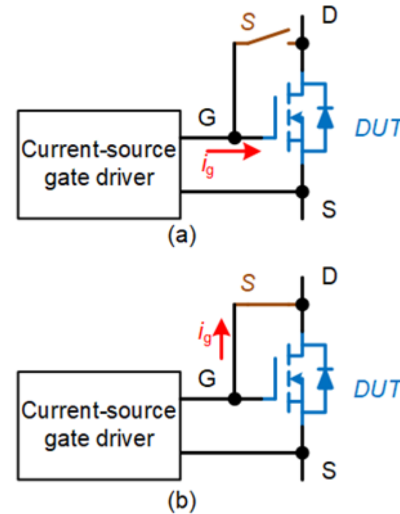
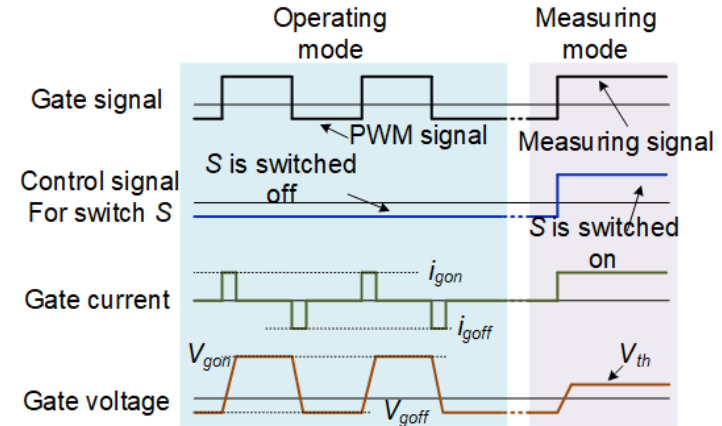


Diagram of the proposed method



Signal sequence of the proposed method

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Phenomenon of Short-Time Vth Shift

- Drain and gate terminals are shorted in the experiment.
- Step current is injected into the gate of the MOSFET.
- Linear increase of Vgs is the result of gate capacitor charging process.
- Vgs stays constant after it reaches Vth.
- Different from the simulation, there is a slow increase period in Vgs waveform.
- The slow increase period is introduced by Vth shift, the period ends after 1us.

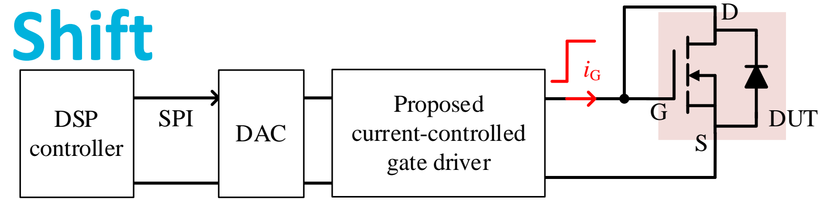
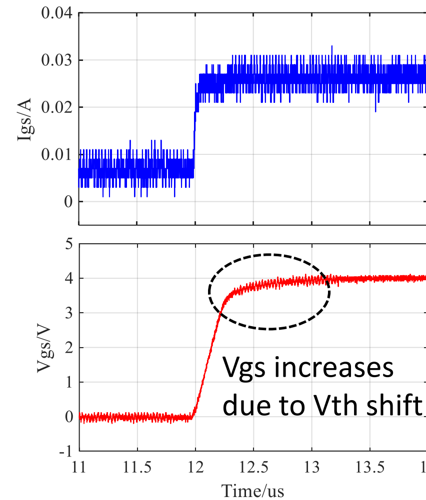
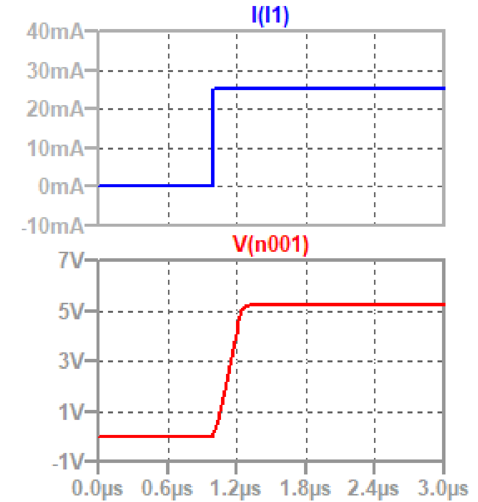


Diagram of the experimental circuit



(a) Experiment



(b) Simulation

Comparison between experiment and simulation

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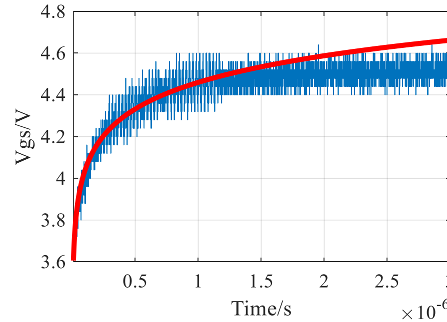
Short-Time Vth Shift as TSEP

In the short-time Vth shift period:

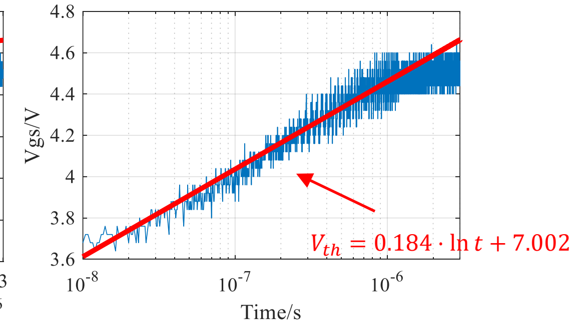
- There is a linear relationship between Vgs and the logarithm of time.
- The Vth shift period is fitted using math equation:

$$V_{th} = \mathrm{K} \cdot \ln t + \mathrm{b}$$

- The equation can not fit the experiment waveform after 1us, which means the short-time Vth shift period ends within 1us.
- The slope rate K can be regarded as a TSEP

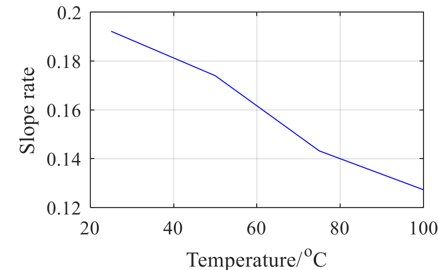


(a) Linear time axis



(b) Logarithm time axis

Curve fitting results of the short-time Vth shift

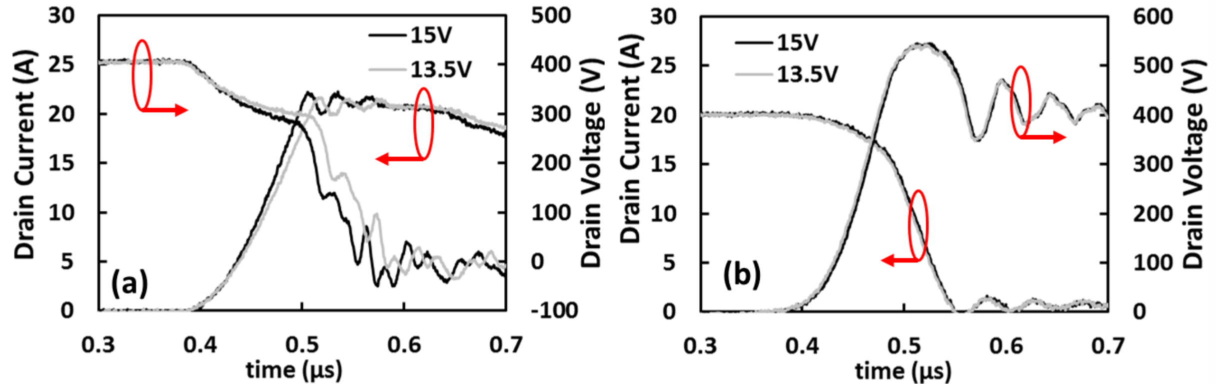


Experiment result of K vs Tj

V_{GS} De-rating for Improved Oxide Reliability

- The rate of BTI is proportional to the electric field in the gate oxide
- De-rating the V_{GS} can reduce the electric field thereby reducing the rate of charge trapping and V_{TH} shift.
- However, there are penalties to pay in terms of conduction and switching losses

MOSFET Turn ON	MOSFET Turn-OFF
$\frac{dI_{DS}}{dt} = \frac{\beta V_{GG}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS} + C_{GD})}$	$\frac{dI_{DS}}{dt} = \frac{-\beta V_{GP}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS} + C_{GD})}$
$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{GP}}{R_G C_{GD}}$	$\frac{dV_{DS}}{dt} = \frac{V_{GP}}{R_G C_{GD}}$



(a) Turn-ON transients at V_{GS} and 90% V_{GS}. (b) Turn-OFF transients at V_{GS} and 90% V_{GS}

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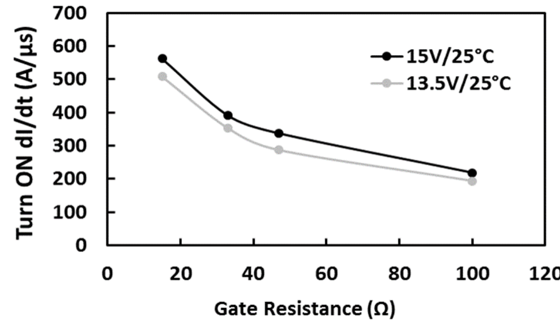
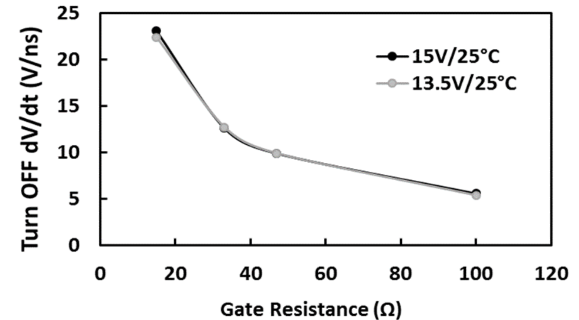
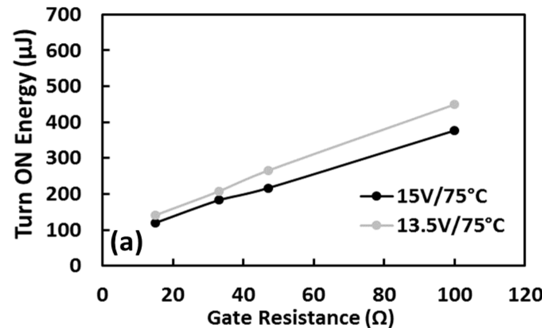
V_{GS} De-rating for Improved Oxide Reliability

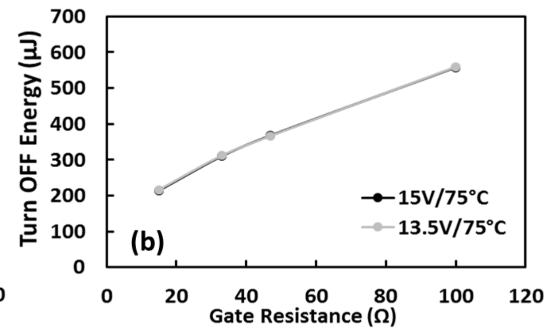
- De-rating VGS by 10% reduces the turn-ON di/dt.
- Turn-OFF dV/dt remains unchanged
- There is a less than 10% increase in turn-ON switching energy as V_{GS} is derated by 10%
- Turn-OFF switching energy is unaffected





(a) Turn-ON dI/dt and (b) Turn-OFF dV/dt as a function of R_G for different V_{GS}





(a) Turn-ON Energy and (b) Turn-OFF Energy as a function of R_G for different V_{GS} at 75°C. Load current:20 A

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Outputs/dissemination/knowledge transfer

Invited talks

IMAPS "Latest Advancements in WBG Reliability and Gate Driving", 2021

Research Projects

Royal Society industry Fellowship, 2020 to 2024, £174k

Journals & conferences

1. R Wu, JO Gonzalez, Z Davletzhanova, PA Mawby, O Alatise The Potential of SiC Cascode JFETs in Electric Vehicle Traction Inverters IEEE Transactions on Transportation Electrification 5 (4), 1349-1359
2. JO Gonzalez, R Wu, S Jahdi, O Alatise Performance and reliability review of 650 V and 900 V silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs, IEEE Transactions on Industrial Electronics 67 (9), 7375-7385
3. JO Gonzalez, O Alatise, Crosstalk in SiC power MOSFETs for evaluation of threshold voltage shift caused by bias temperature instability 2019 21st European Conference on Power Electronics and Applications (EPE'19)
4. JO Gonzalez, M Hedayati, S Jahdi, BH Stark, O Alatise, Dynamic characterization of SiC and GaN devices with BTI stresses Microelectronics Reliability 100, 113389.
5. JO Gonzalez, R Wu, SN Agbo, O Alatise Robustness and reliability review of Si and SiC FET devices for more-electric-aircraft applications Microelectronics Reliability 100, 113324
6. E Bashar, Q Han, R Wu, L Ran, O Alatise, S Jupe, Analysis of DC offset in fault current caused by machines in a medium voltage distribution network, The Journal of Engineering 2019 (17), 3494-3499
7. B Hu, S Konaklieva, S Xu, J Ortiz-Gonzalez, L Ran, C Ng, P McKeever and O Alatise, Condition monitoring for solder layer degradation in multi-device system based on neural network The Journal of Engineering 2019 (17), 3582-3586
8. JO Gonzalez, O Alatise, Challenges of junction temperature sensing in SiC power MOSFETs, 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE)
9. JO Gonzalez, O Alatise, P Mawby, Characterization of BTI in SiC MOSFETs Using Third Quadrant Characteristics, 2019 31st International Symposium on Power Semiconductor Devices and ICs …
10. JO Gonzalez, O Alatise, PA Mawby, Novel Method for Evaluation of Negative Bias Temperature Instability of SiC MOSFETs, Materials Science Forum 963, 749-752

Journals & conferences

1. Wang X, Wu H, Pickert V. "Gate Threshold Voltage Measurement Method for SiC MOSFET with Current-Source Gate Driver, " *2020 IET International Conference on Power Electronics, Machines and Drives (PEMD)*, In press.

2. Wu H, Wang X, et al. "Investigation into the Switching Transient of SiC MOSFET Using Voltage/Current Source Gate Driver, " *2020 IET International Conference on Power Electronics, Machines and Drives (PEMD)*, In press.

3. Wang, X., Wu, H., and Pickert, V. (2020, January). A cost-efficient Current-Source Gate Driver for SiC MOSFET Module and its Comparison with Voltage-Source Gate Driver. In *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)* (pp. 979-984). IEEE.

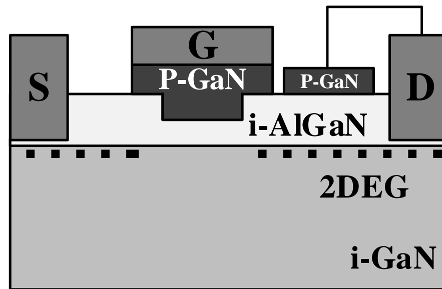
4. Wang, X., Wu, H., and Pickert, V. (2019, March). Design of an advanced programmable current-source gate driver for dynamic control of SiC device. In *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 1370-1374). IEEE.

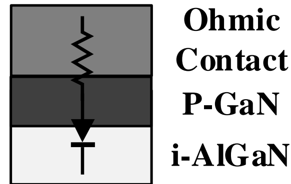
CONTENTS/OUTLINE

- Gate Dielectrics and Temperature Sensing in GaN HEMTs
  - Introduction to GaN HEMTs
  - 3rd Quadrant Technique in GaN HEMTs
  - Advanced Gate Driving in GaN HEMTs
  - Junction Temperature Sensing in GaN HEMTs

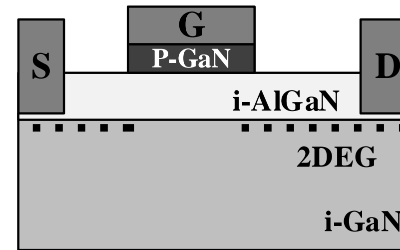
Introduction to GaN HEMTs

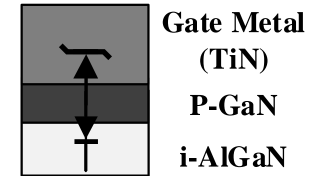
- (i) p-GaN gate on AlGaN with an ohmic contact
- (ii) p-GaN gate on AlGaN with a Schottky contact





Ohmic contact





Schottky contact

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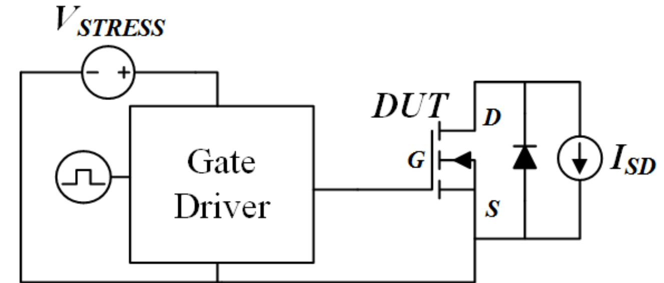
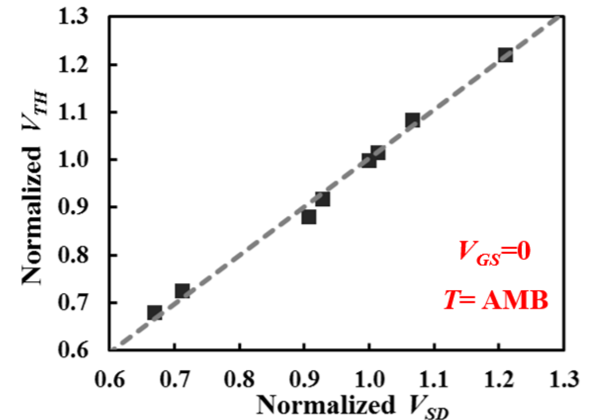
Third Quadrant Characteristics in GaN HEMTs

- Method for characterizing V_{TH} shifts in SiC MOSFETs using the body diode.
  - Similar to the use of V_{SD} as temperature sensor
  - It requires a calibrated relationship between V_{SD} and V_{TH}
- GaN HEMTs
  - **There is direct a relationship between V_{SD} and V_{TH}**

	V_{TH} (V) V_{GS}=V_{DS} @ I= 10 mA	V_{SD} (V), V_{GS}=0, @ I = 10 mA
Ohmic Gate GaN HEMT	**1.478**	**1.483**
Schottky Gate GaN HEMT	**1.597**	**1.576**





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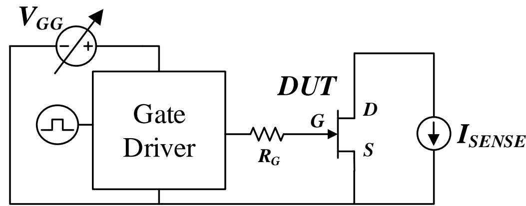
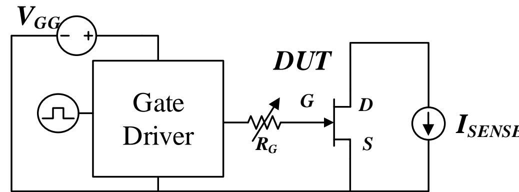
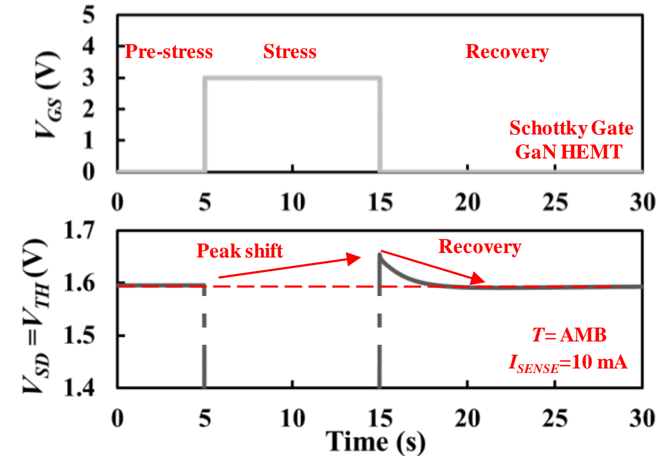
Threshold Voltage Instability in GaN HEMTs

- We evaluated the third quadrant methodology in GaN devices for characterizing V_{TH} drift after gate stress
  - Gate voltage stress for the Schottky gate HEMT
  - Gate current stress for the Ohmic gate HEMT







Example for a 3 V/10 s stress pulse

- Different stress parameters can be evaluated:
  - Stress time
  - Gate stress voltage/current
  - Temperature

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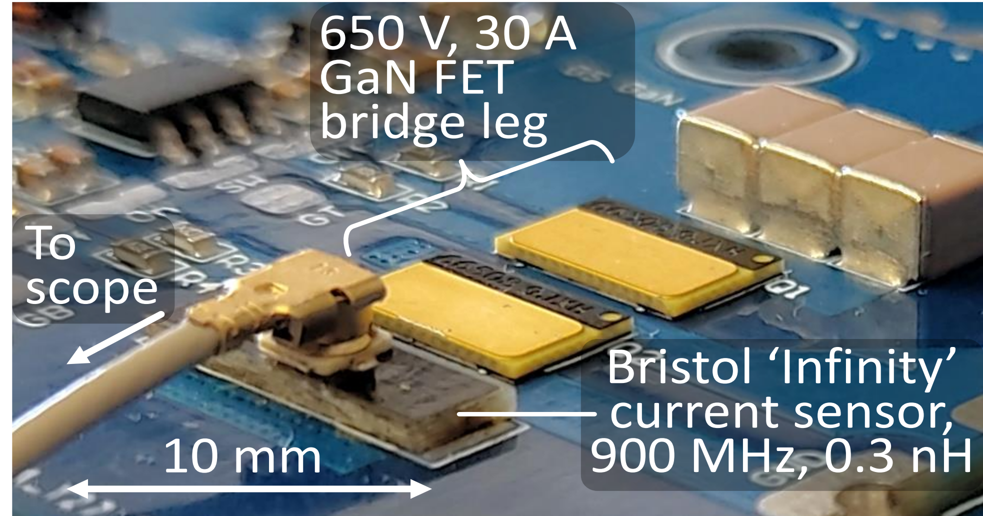
Advanced Gate Drivers and Current Sensing for GaN Devices

- We may have a working active gate driver chip for SiC devices before end of year (Output amplitude range: +/-20A, +35V to -10V. Timing flexibility: 100 steps of 1ns, each with independently adjustable drive strength). Please register your interest.

- We also still have Gen3 GaN driver chips if you'd like to try out certain gate waveforms on GaN, or create high-def pulses for other purposes.



Version 2 of Bristol Infinity Sensor will be available soon,

please register your interest via bernard.stark@bristol.ac.uk

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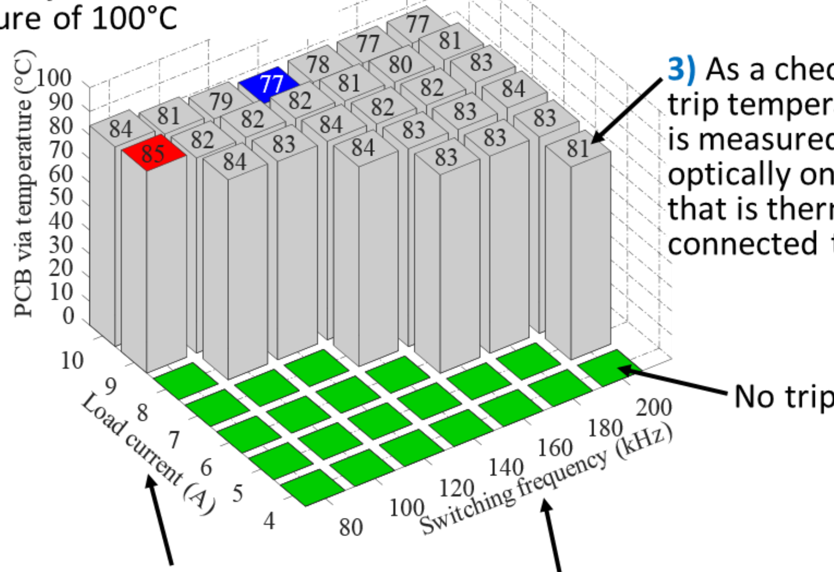
Over-Temperature Protection using di/dt as a TSEP

1) A limit on di/dt is set, that equates to a junction temperature of 100°C

2) Circuit trips when max turn-on di/dt drops below this limit.

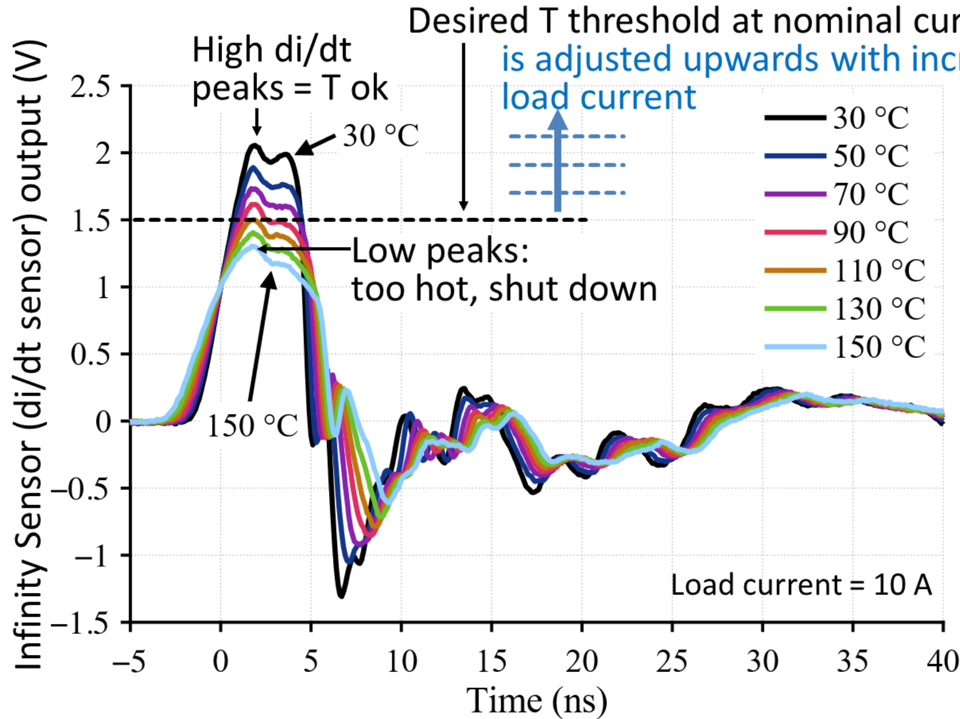
3) As a check, the trip temperature is measured optically on a via that is thermally connected to case



4) Load current and switching frequency are swept to check that the protection circuit works independently of these.

- The junction temperature of the GaN HEMT depends on the load current and the switching frequency
- When implementing junction temperature sensing, it is important to be able to distinguish between both effects

Over-Temperature Protection using di/dt as a TSEP



- Using the temperature sensitivity of di/dt in GaN HEMTs, the high speed current sensor can detect device junction temperature
- GaN has a significant temperature dependency in terms of ON-state resistance and switching rates
- Very high switching rates make temperature and di/dt sensing in GaN very difficult to implement

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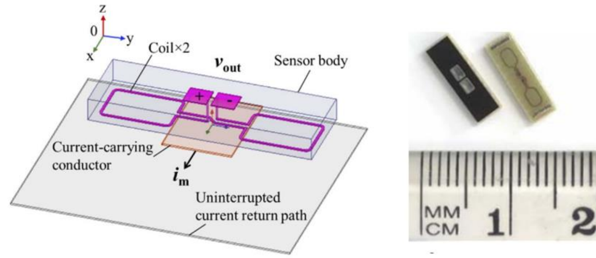
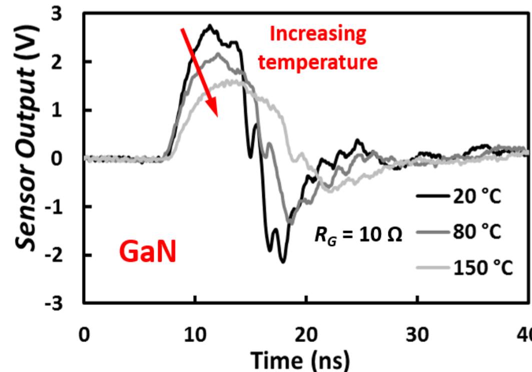
Over-Temperature Protection using di/dt as a TSEP

- Using the high speed infinity sensor, the temperature sensitivity of the GaN switching transient is measured

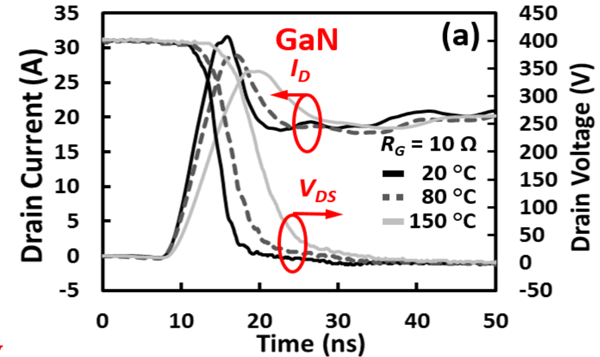
- GaN has a significant temperature dependency in terms of ON-state resistance and switching rates

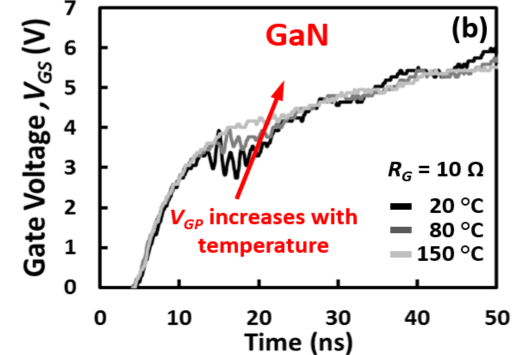


Infinity Sensor developed by Bristol University



Output voltage of the Infinity Sensor





Turn-ON transients for a GaN HEMT at different temperatures. (a) I_D and V_{DS} (b) V_{GS}

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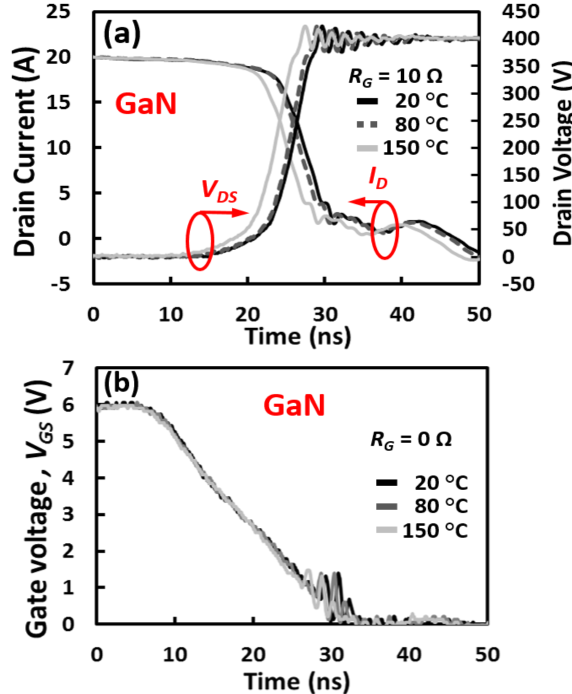
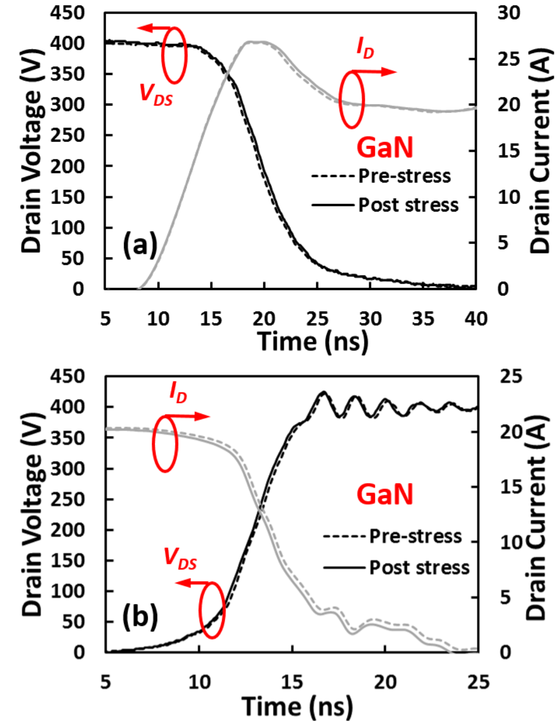
Over-Temperature Protection using di/dt as a TSEP

- Switching transient measurements have been performed on 650V GaN HEMTs
- Measurements were performed on unstressed and stressed devices to investigate the impact the impact of BTI on the transient switching characteristics of GaN HEMTs

J. O. Gonzalez, M. H. Hedayati, S Jahdi, B. H. Stark, O. Alatise, "**Dynamic characterization of SiC and GaN devices with BTI stresses**," Journal of Microelectronics Reliability, Volume 100, 2019.



Turn-OFF transients for a GaN HEMT at different temperatures. (a) I_D and V_{DS} (b) V_{GS}



(a) Pre-stress and post-stress (a) turn-ON and (b) turn-OFF characteristics in GaN device

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Outputs/dissemination/knowledge transfer

M. H. Hedayati, J. Wang, H. C. P. Dymond, D. Liu, B. H. Stark, " **Over-Temperature Protection Circuit for GaN Devices Using a di/dt Sensor**," in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 7417-7428, July 2021.

D. Liu, S. J. Hollis, H. C. P. Dymond, N. McNeill, D. Pamunuwa, B. H. Stark, “**Full custom design of an arbitrary waveform gate driver with 10 GHz waypoint rates for GaN FETs**” in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 8267-8279, July 2021.

S. Jahdi, M. Hedayati, B. H. Stark and P. H. Mellor, "**The Impact of Temperature and Switching Rate on Dynamic Transients of High-Voltage Silicon and 4H-SiC NPN BJTs: A Technology Evaluation**," IEEE Transactions on Industrial Electronics, vol. 67, no. 6, pp. 4556-4566, June 2020.

D. Liu, S. J. Hollis and B. H. Stark, "**A New Design Technique for Sub-Nanosecond Delay and 200 V/ns Power Supply Slew-Tolerant Floating Voltage Level Shifters for GaN SMPS**," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 1280-1290, March 2019.

J. O. Gonzalez, M. H. Hedayati, S Jahdi, B. H. Stark, O. Alatise, “**Dynamic characterization of SiC and GaN devices with BTI stresses**,” Journal of Microelectronics Reliability, Volume 100, 2019.

L. Middelstaedt, J. Wang, B. H. Stark and A. Lindemann, "**Direct Approach of Simultaneously Eliminating EMI-Critical Oscillations and Decreasing Switching Losses for Wide Bandgap Power Semiconductors**," in IEEE Transactions on Power Electronics, vol. 34, no. 11, pp. 10376-10380, Nov. 2019.

M. H. Hedayati, H. C. P. Dymond, and B. H. Stark, " **P-GaN gate VTH shift effects on double-pulse testing and converter continuous mode operation**," IEEE Applied Power Electronics Conference and Exposition (APEC), 2021.

M. H. Hedayati, H. C. P. Dymond, D. Liu, and B. H. Stark, "**Fast temperature sensing for GaN power devices using E-field probes**," IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, 2020.

Y. Gunaydin, S. Jahdi, O. Alatise, J. O. Gonzales, R. Wu, B. H. Stark, M. H. Hedayati, X. Yuan, and P. H. Mellor, "**Performance of Wide-Bandgap Gallium Nitride vs Silicon Carbide Cascode Transistors**," IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 239-245.

J. Wang, M. H. Hedayati, D. Liu, S. E. Adami, H. C. P. Dymond, J. J. O. Dalton, and B. H. Stark, "**Infinity Sensor: Temperature Sensing in GaN Power Devices using Peak di/dt**," IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 884-890.

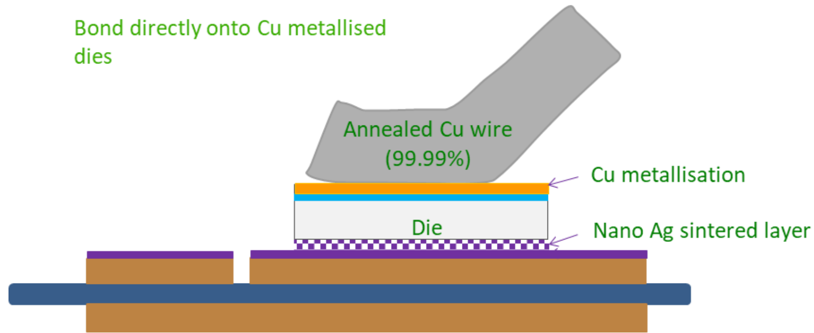
• CONTENTS/OUTLINE

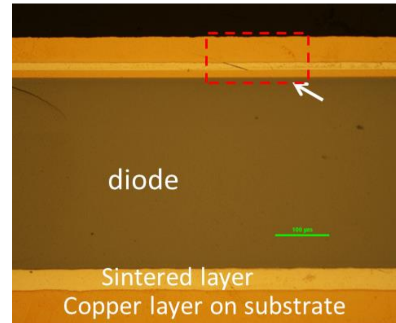
Copper Interconnects and Physics of Failure Modules

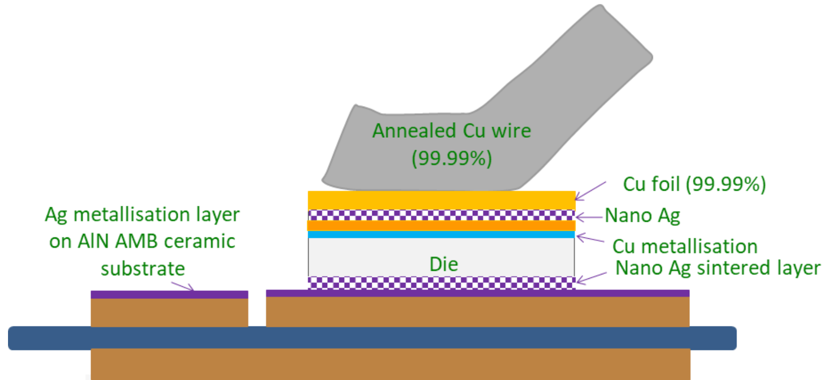
- Manufacturability & reliability of ultrasonically bonded copper wire interconnects
- Reliability studies of Ag-sintered die & large area attachments (collaboration with Loughborough)
- Physics of failure & lifetime model development (joint with Greenwhich)

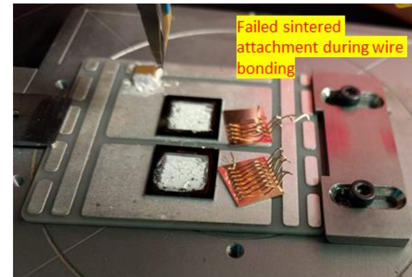
Dr Pearl Agayakwa, University of Nottingham

• WP2.1 Cu Bonding Trails and Reliability Assessment









- Annealed Cu wire bonds strongly to 25 µm thick tempered Cu foil sintered onto Ag-metallised devices. However, silver attachment fails.

- Further work to look at Cu-compatible silver pastes & other more robust composite structures

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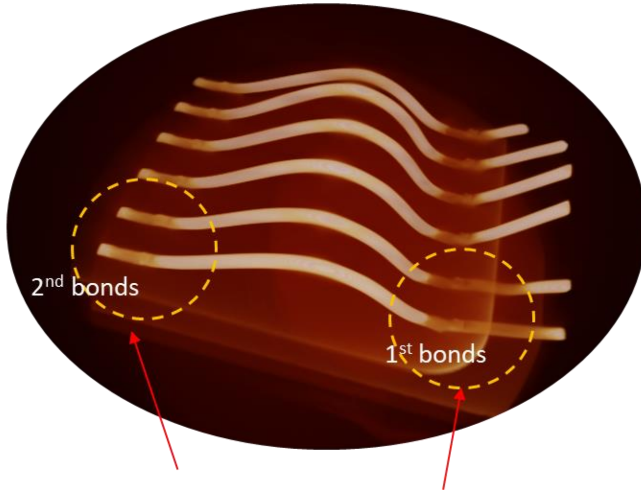
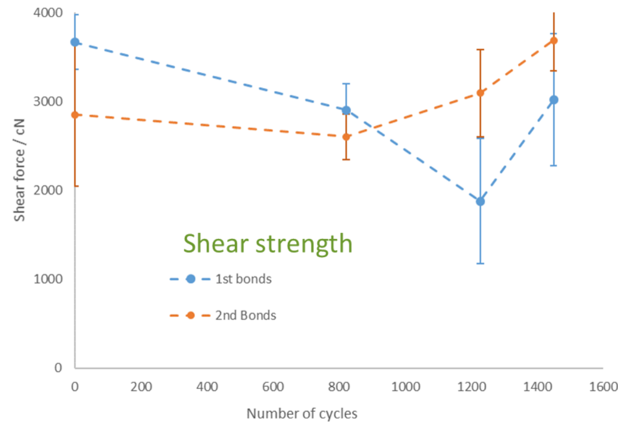
• WP2.1 Cu Bonding Trails and Reliability Assessment





- Reliability of Cu-Cu bonds assessed
- Shear strength up to 2x higher than Al wire bonds; negligible reduction in reliability after 1000 cycles from -55 to +195°C
- Possible evidence for cyclic hardening

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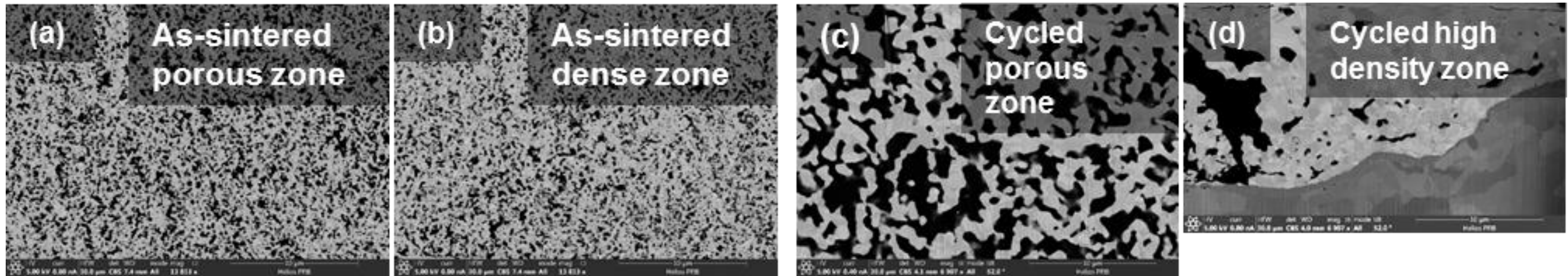
WP2.1 Detailed Microstructural Analysis of Sintered Attachment Degradation

- Joint work ongoing with HI theme (Loughborough team) to perform correlative microscale analyses of sintered attachment to support damage model development
- FIB SEM microstructures of heterogeneous pore structures and varied densities of the Ag layer & their evolution during cycling



- Grain growth, pore growth, pore number reduction, and densification observed under power cycling
- Cracks initiate within silver and propagate through copper beneath after several cycles

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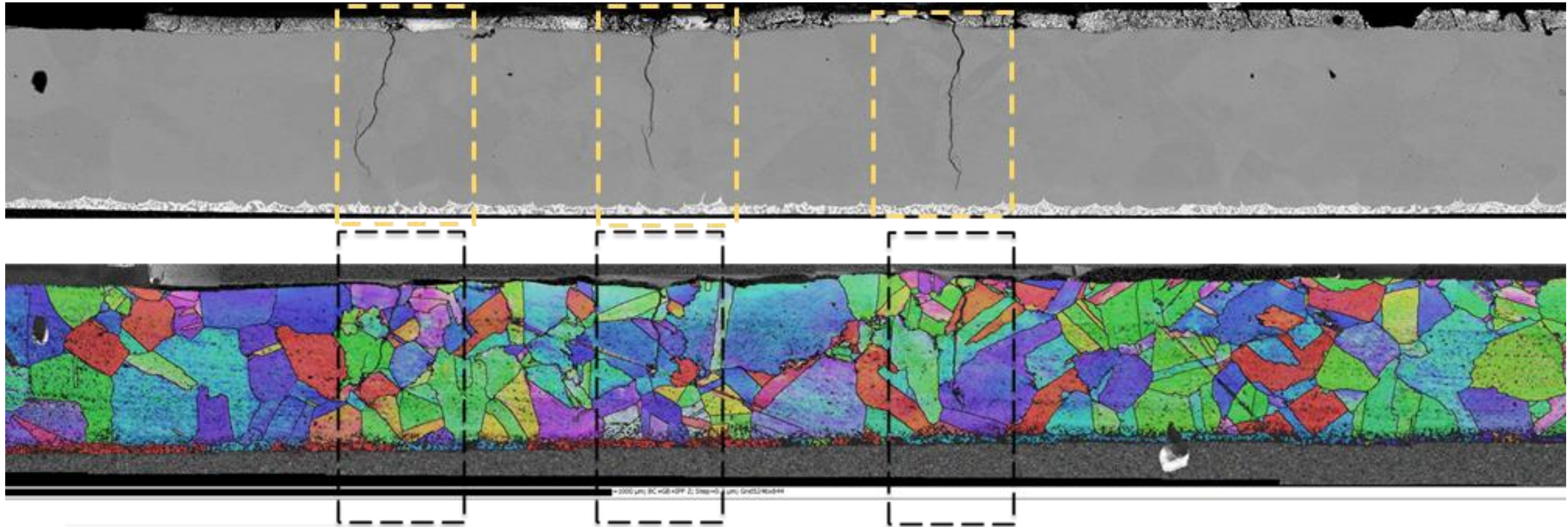
WP2.1 Detailed Microstructural Analysis of Sintered Attachment Degradation

EBSD microstructures showing transgranular crack propagation through copper substrate after 650K power cycles



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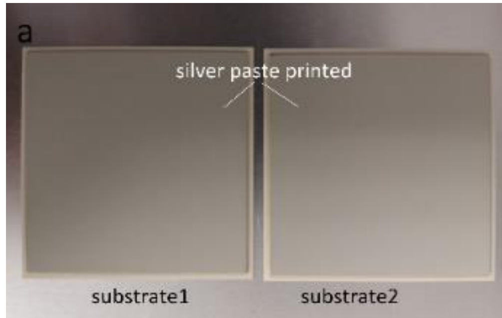
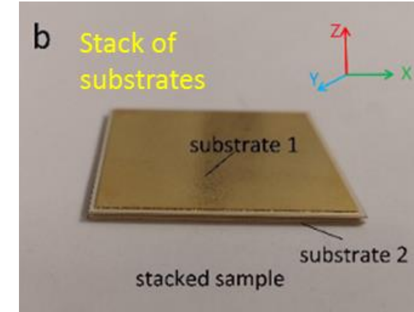
WP2.1 Large Area Sintered Attachments

Materials: 40 mm × 40 mm × 0.85 mm Si_3N_4 ceramic substrate by Rogers Corp.
Substrate tile: 0.25 mm-thick Si3N4 ceramic tile sandwiched between 0.3 mm Cu tracks.
Surface finish: 3-7 µm Ni, plus 30-130 nm Au.





Pressure-assisted (Argomax 2020 (100nm))

- Silver paste printed on two substrates with 80 µm thick stainless-steel stencils
- dried at 130 °C for 20 minutes to evaporate organics
- Put together & fixed in position using Kapton tape
- Sintering at 250 °C and under a pressure of 3 MPa for 20 mins, then cooled down to room temperature before releasing the pressure.

'Pressure-less'(NJ-Surface from Nano-Joint (20 nm))

- Silver paste manually printed on one substrate with 80 µm thick stainless stencil, then 2nd substrate placed on top
- Fixture used for alignment
- Samples were placed in an air convection oven, a 625g weight placed on top to facilitate full contact
- Pre-sintering drying
- Sintered at 250 °C for 1 h, oven-cooled to room temperature

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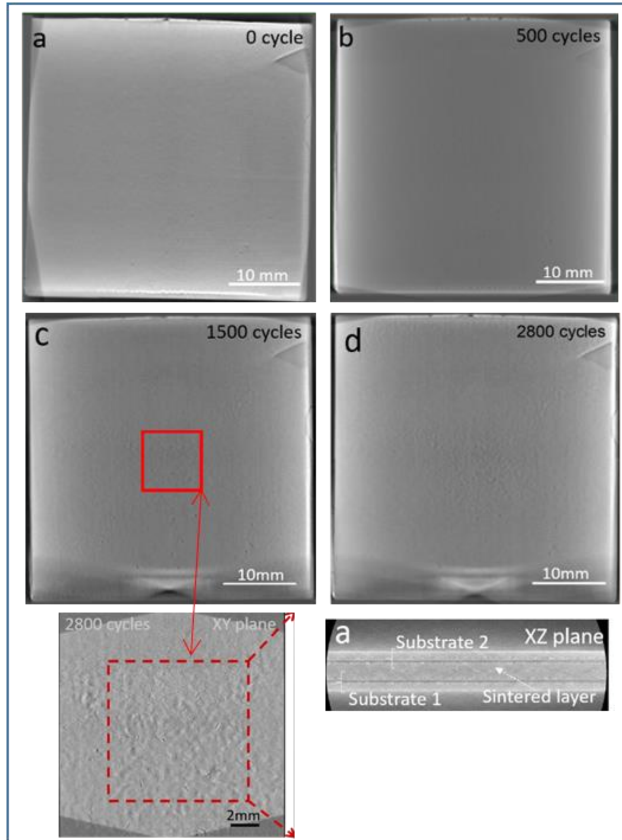
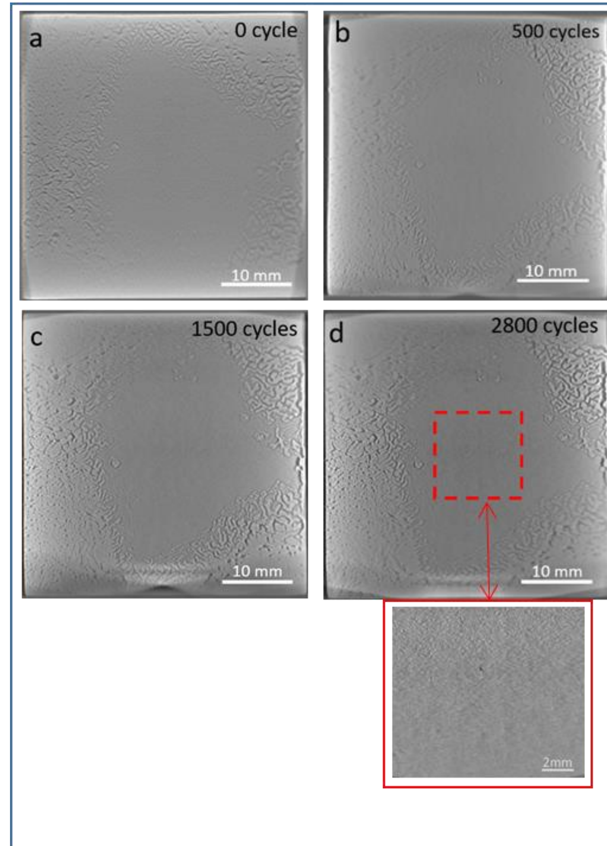
WP2.1 Large Area Sintered Attachments





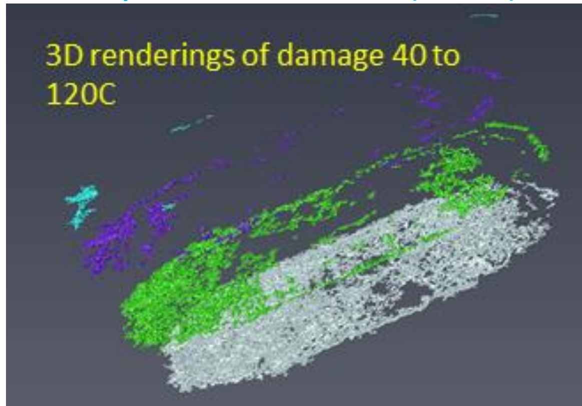
- 'Large-area' sintered attachments:
- X-ray CT of thermally cycled joints (-55 °C to 170 °C)
- *Insignificant damage after ~ 3000 cycles*

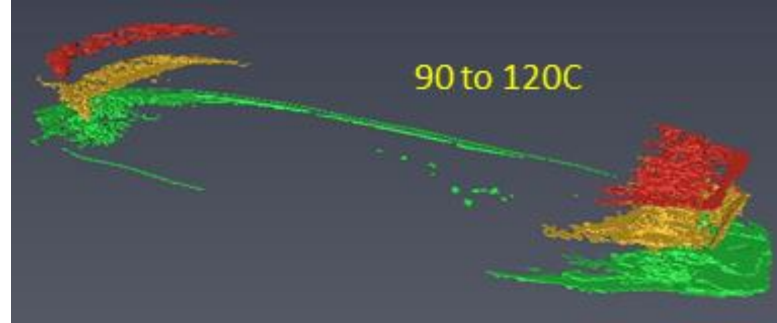
Spatial resolution : ~21.3µm
4.85~7.62 µm for red boxes

Finite Element Modelling of Wirebond Damage

- Quantification of legacy wire bond lifetime tomography data from to support damage model development
- Greenwich have simulated power module test specimen using VEPP and a FEA code & to predict strains and stresses for cyclic loading conditions (wire bonds, solder joints)
- Ongoing work: develop crack propagation part of time-domain model, validate over wider range of test conditions
- The lifetime model will be embedded in VPPE

Experimental data (XRCT)





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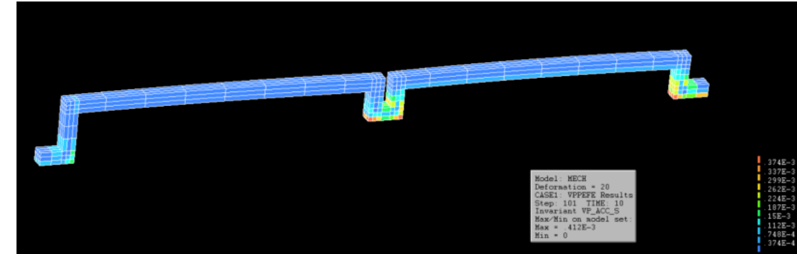
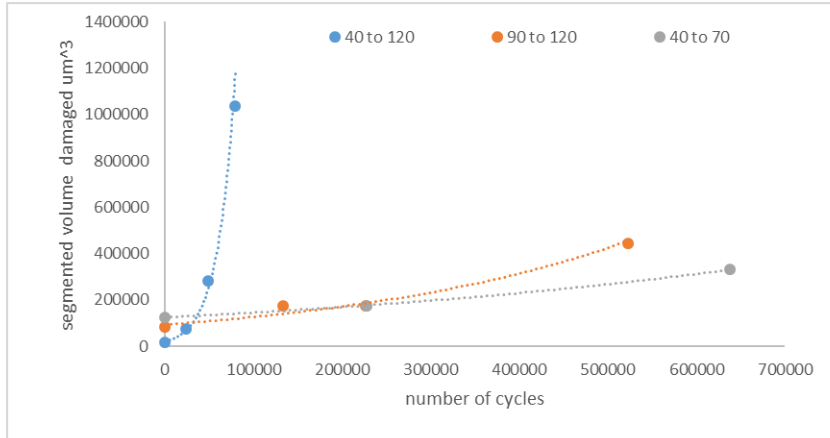
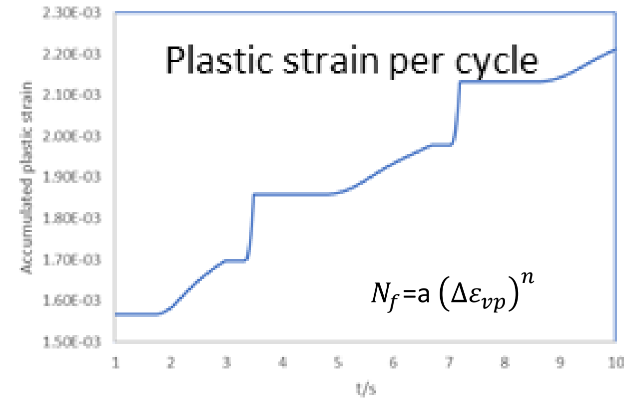
Finite Element Modelling of Wirebond Damage

- Greenwich have simulated power module test specimen using VEPP and a FEA code & to predict strains and stresses for cyclic loading conditions (wire bonds, solder joints)
- Ongoing work: develop crack propagation part of time-domain model, validate over wider range of test conditions
- The lifetime model will be embedded in VPPE







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Outputs/dissemination/knowledge transfer

Invited talks

Agyakwa, P., (Keynote) “Three-dimensional damage microstructures of thermomechanically stressed power electronics module interconnects” EUROMAT 2021, 13/09/2021.

Agyakwa, P., “3D microstructural perspectives of degradation in power electronics packaging interconnects”, Oxford Micromechanics Group Symposium 08/07/2021

Agyakwa, P., “Advances in packaging interconnects”, IMAPS Research Showcase: Recent Advances on Reliability and Gate Driving of WBG Power Electronics, January 2021

KTP

KTP with Littelfuse Group on implementing reliable power terminals for high performance power electronics modules (ref KTP 11574) awarded Jan 2019, Innovate UK, £104k. Project duration Sept 2019 – Dec 2021

Journals & conferences

Agyakwa, P., Robertson, S., Dai, J., Mouawad, B., Zhou, Z., Johnson, CMJ., “Microstructural evolution under power cycling of sintered nanosilver particle attachments for SiC power modules”, In preparation for submission to Acta Materialia

Agyakwa, P, Dai, J, Li, J, Mouawad, B, *et al*., Three-dimensional damage morphologies of thermomechanically deformed sintered nanosilver die attachments for power electronics modules (2020), J. Microsc. 277 (3) pp.140-153

Dai, J, Li, J, Agyakwa, P, *et al*., Shear strength of die attachments prepared using dry nanosilver film by a time-reduced sintering process (2020), Microelectron. Reliab. 111 DOI: 10.1016/j.microrel.2020.113740

Agyakwa, P. et al., “Three-dimensional damage morphologies of thermomechanically deformed sintered nano-silver die attachments for power electronics modules” RMS ToSCA 2018, WMG, Coventry, UK.

Agyakwa P., Mouawad, B., Yang, L., Corfield, M., Evans, P., Johnson, CMJ, Chan, LH, Bale, H., Sun, J., “A study of fractured aluminium bond wires via absorption and diffraction contrast tomography modes, RMS ToSCA 2019, Southampton, UK”

Mouawad, P. Agyakwa, M. Corfield and C. M. Johnson, "A correlative approach to observing the thermomechanically driven microstructural evolution of ultrasonically bonded copper wires," *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1-6.

Questions