

# Research Trends in Modular Multilevel Cascade Converters

---

Hirofumi (Hiro) Akagi  
Tokyo Institute of Technology  
13<sup>th</sup> July 2021



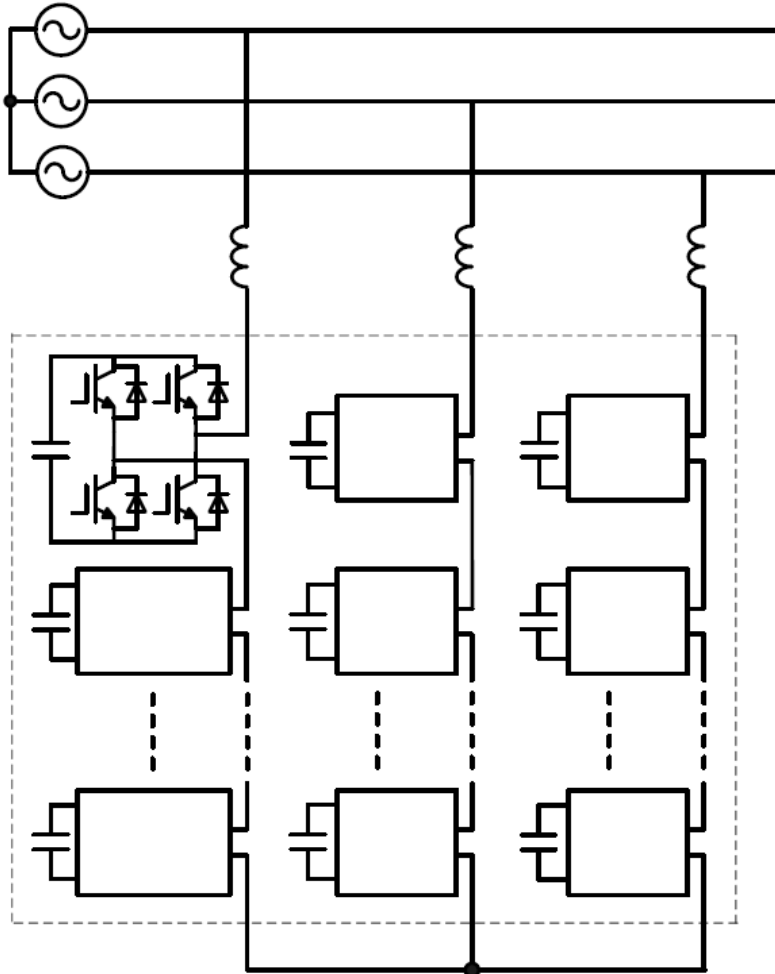
# Terminology Issue of Cascade Multilevel Converters and Modular Multilevel Converters

---

H. Akagi, “Multilevel Converters: Fundamental Circuits and Systems,”  
*The Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048-2065, Nov.  
2017. (invited paper)



# Terminology Issue of Cascade Multilevel Converters



Single-Star Bridge Cells (SSBC)

## Three Different Technical Terms

### “Cascade Multilevel Converter”

F. Z. Peng and J. S. Lai,  
*IEEE Trans. Ind. Appl.*, 1997

### “Cascaded H-Bridge Converter”

Y. Fukuta and G. Venkataramanan,  
*IEEE IAS Annual Meeting*, 2002

### “Chain-Link Converter”

C. Oates, *EPE*, 2009

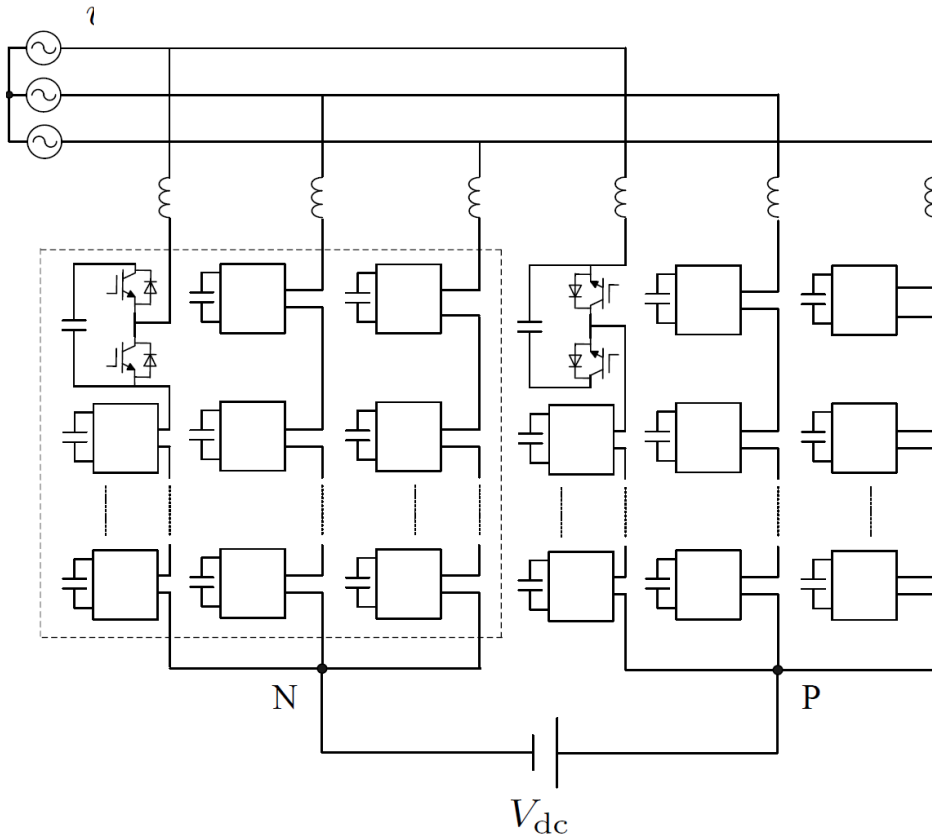
“Modular” structure and

“Multilevel” voltage waveforms

One of Modular Multilevel  
Converters



# Terminology Issue of Modular Multilevel Converters



Double-Star Chopper Cells (DSCC)

## Technical Term

“Modular Multilevel Converter”

R. Marquardt and A. Lesnicar,  
*EPE 2003*

“Cascade” structure and  
“Multilevel” voltage waveforms

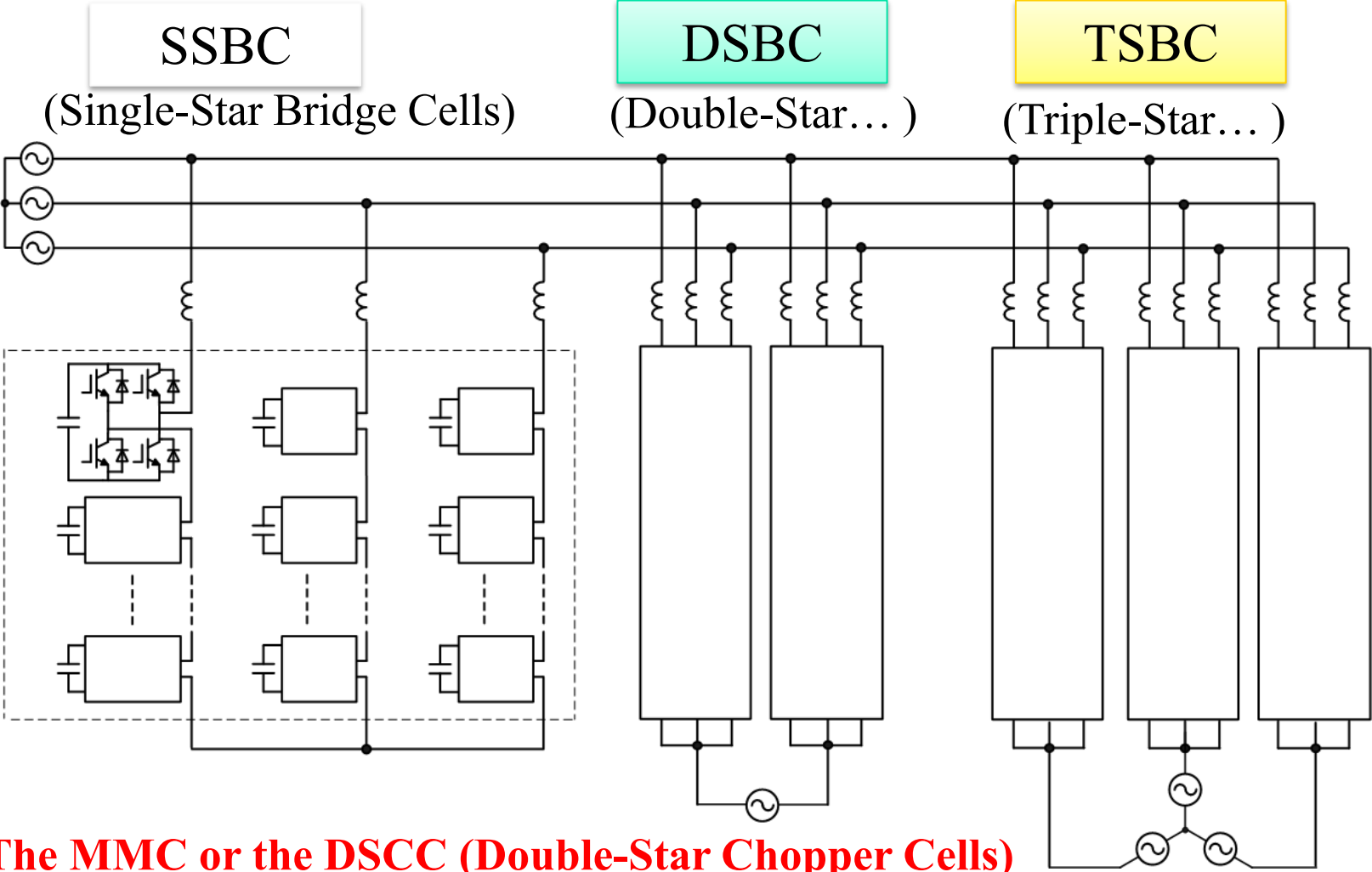
One of Cascade Multilevel  
Converters

The two original names may cause confusion or misunderstanding.



# Classification and Terminology of the MMCC Family

**Family name: MMCC (Modular Multilevel Cascade Converter)**



**The MMC or the DSCC (Double-Star Chopper Cells) is a special case of the DSBC converter**



# Medium-Voltage SSBC-Based STATCOM with Phase-Shifted-Carrier PWM

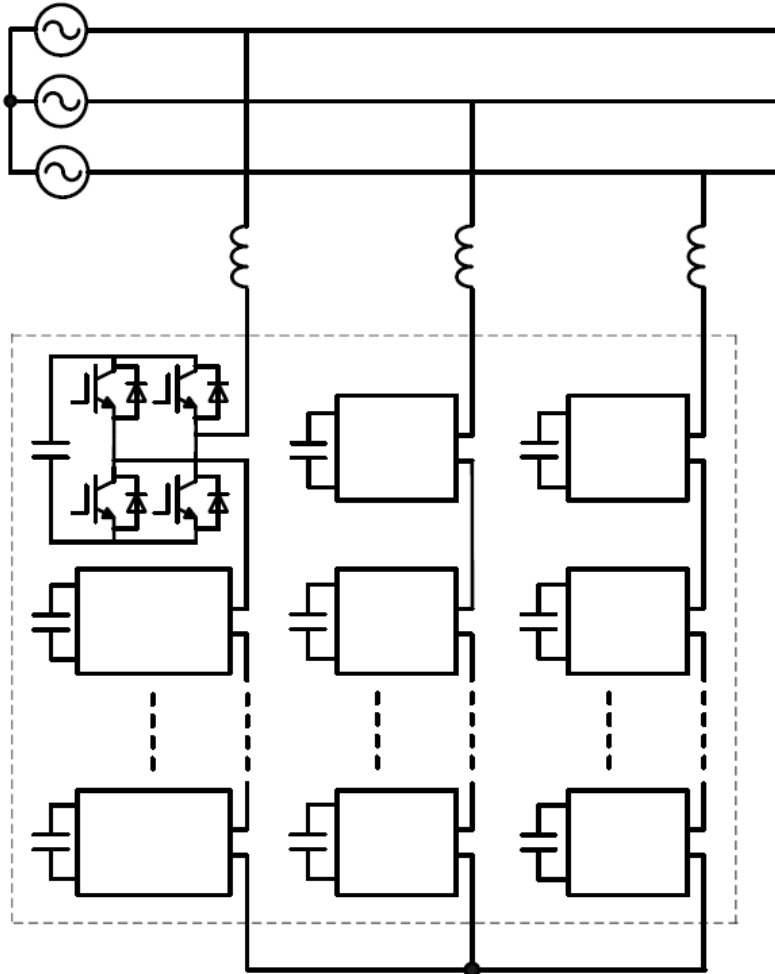
---

## SSBC: Single-Star Bridge Cells

H. Akagi, S. Inoue, and T. Yoshii, “Control and performance of a transformerless cascade PWM STATCOM with star configuration,” *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041-1049, Jul./Aug., 2007.



# Staircase Modulation and Phase-Shifted-Carrier PWM



Single-Star Bridge Cells (SSBC)

F. Z. Peng and J. S. Lai,  
*IEEE Trans. Ind. Appl.*, 1997

The use of GTO thyristors:

**Staircase modulation (SCM)**

Capacitor-voltage balancing:

**Swapping control**

H. Akagi, S. Inoue, and T. Yoshii,  
*IEEE Trans. Ind. Appl.*, 2007

The use of IGBTs:

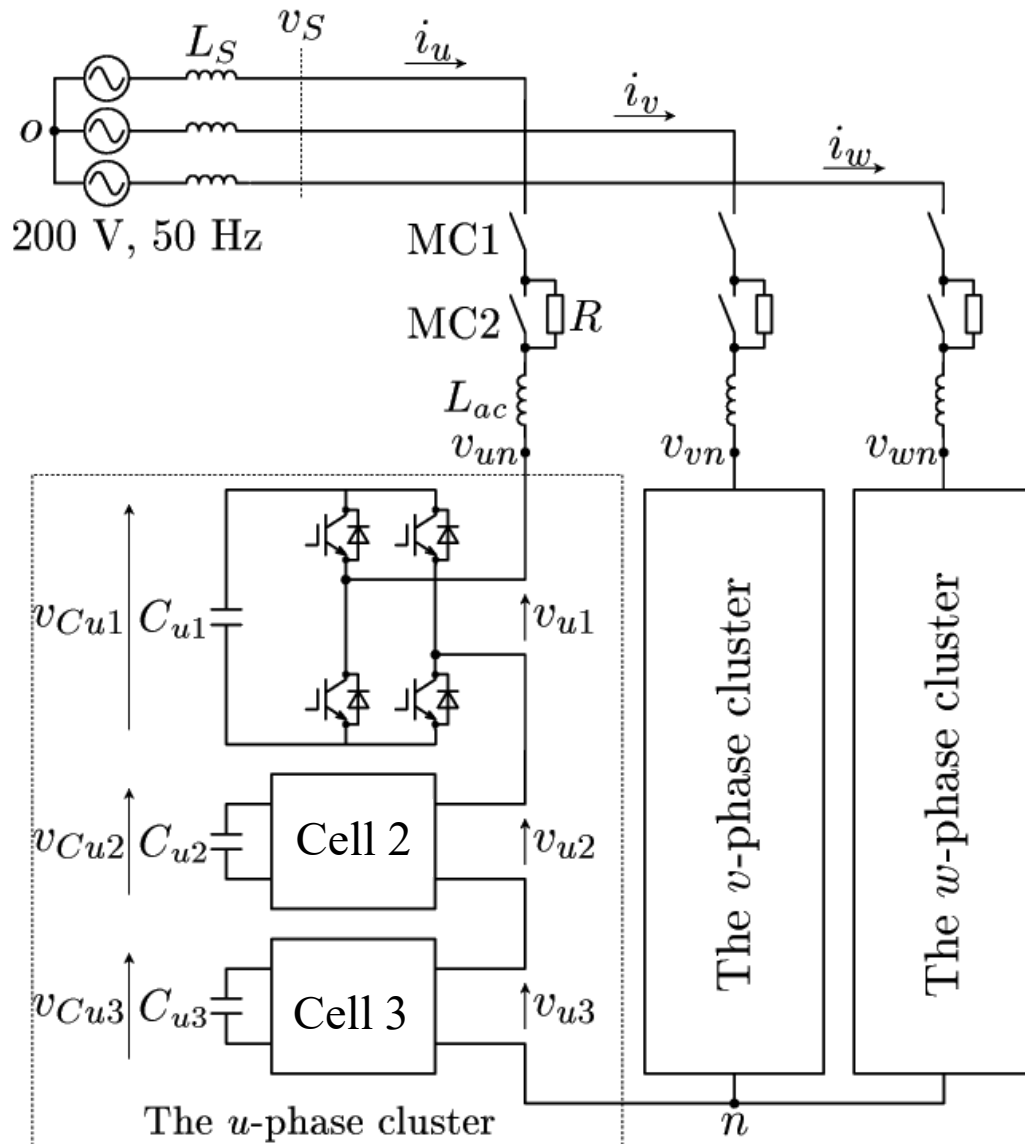
**Phase-shifted-carrier PWM**

Capacitor-voltage balancing:

**Hierarchy control**



# 200-V 10-kVA 50-Hz STATCOM for Experiment



Cell count per cluster: 3

7-level in line-to-neutral

13-level in line-to-line

**Phase-Shifted-Carrier PWM**

Carrier frequency: 1 kHz

Equiv. frequency: 6 kHz

$$L_S = 0.4\% \text{ (40 mH)}$$

$$L_{ac} = 10\% \text{ (1.2 mH)}$$

$$H = 36 \text{ ms (} v_C = 70 \text{ V)}$$

$$C = 16.4 \text{ mF}$$





# What Brought both **Phase-Shifted-Carrier PWM** and **Hierarchy Control** to the STATCOM?

SSBC: Single-Star Bridge Cells

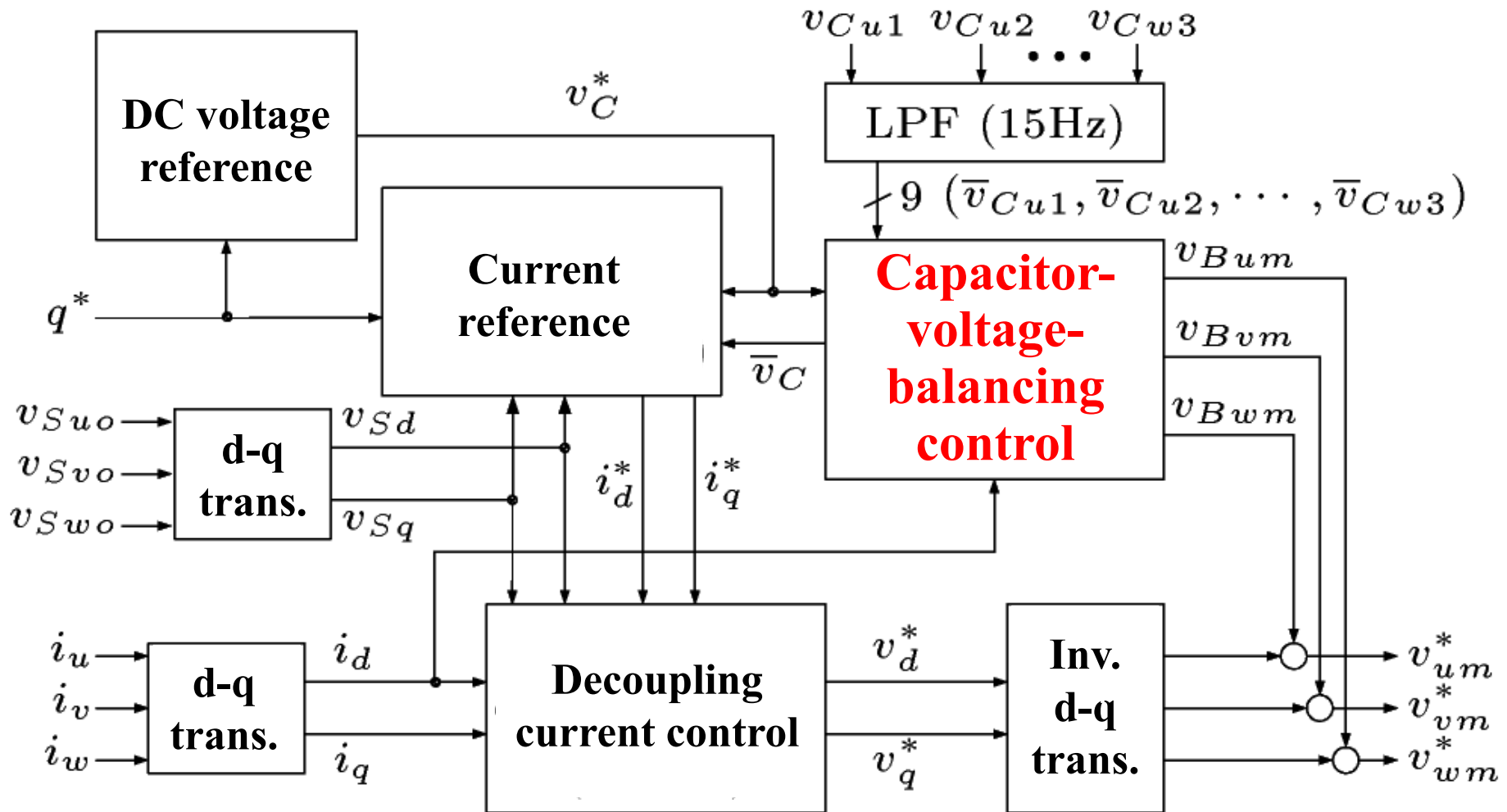
Easy expansion to any bridge-cell count per cluster for any SSBC-based STATCOM.

H. Akagi, “What led to success in academic research on the family of modular multilevel cascade converters,” ECCE-Asia/IPEC-Niigata, pp. 2353-2359, 2018.

H. Akagi, “A review of developments in the family of modular multilevel cascade converters,” IEEJ (IEE of Japan) Transactions, vol. 13, pp. 1222-1235, 2018. (invited paper)

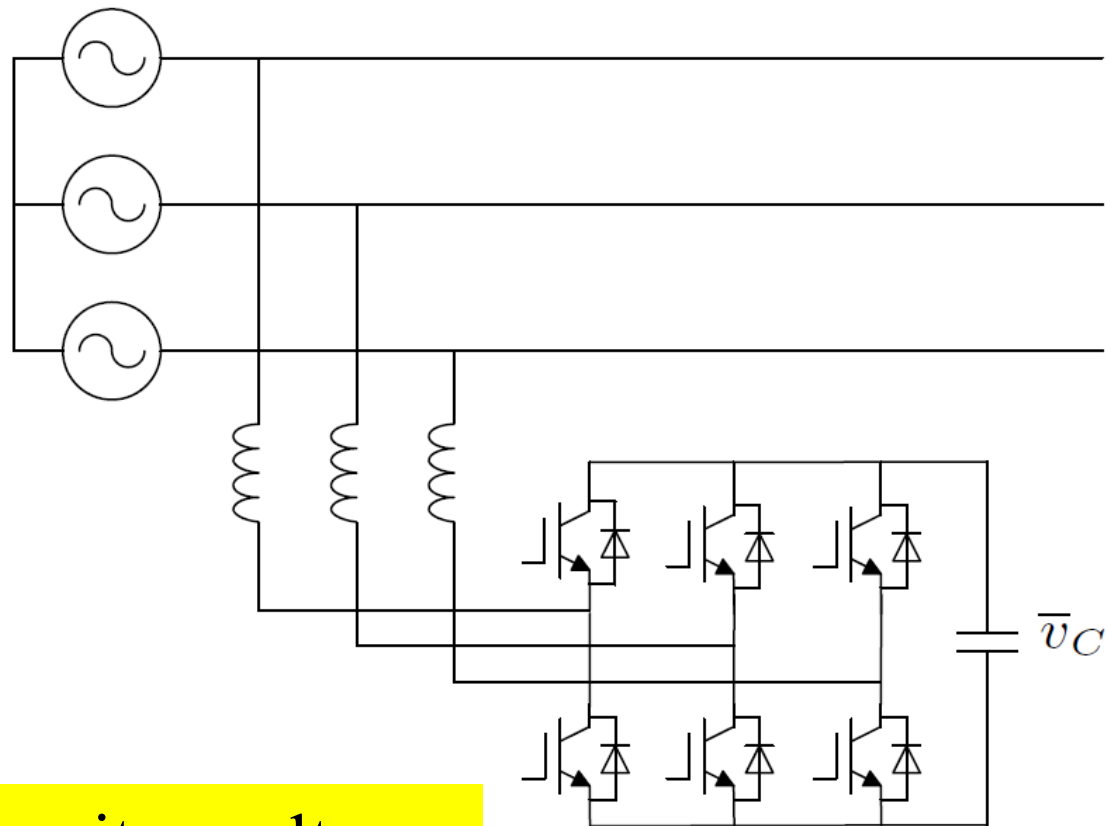


# Control Block Diagram for the STATCOM



# Top Layer in Hierarchy Control

## Overall Voltage Control and Reactive-Power control



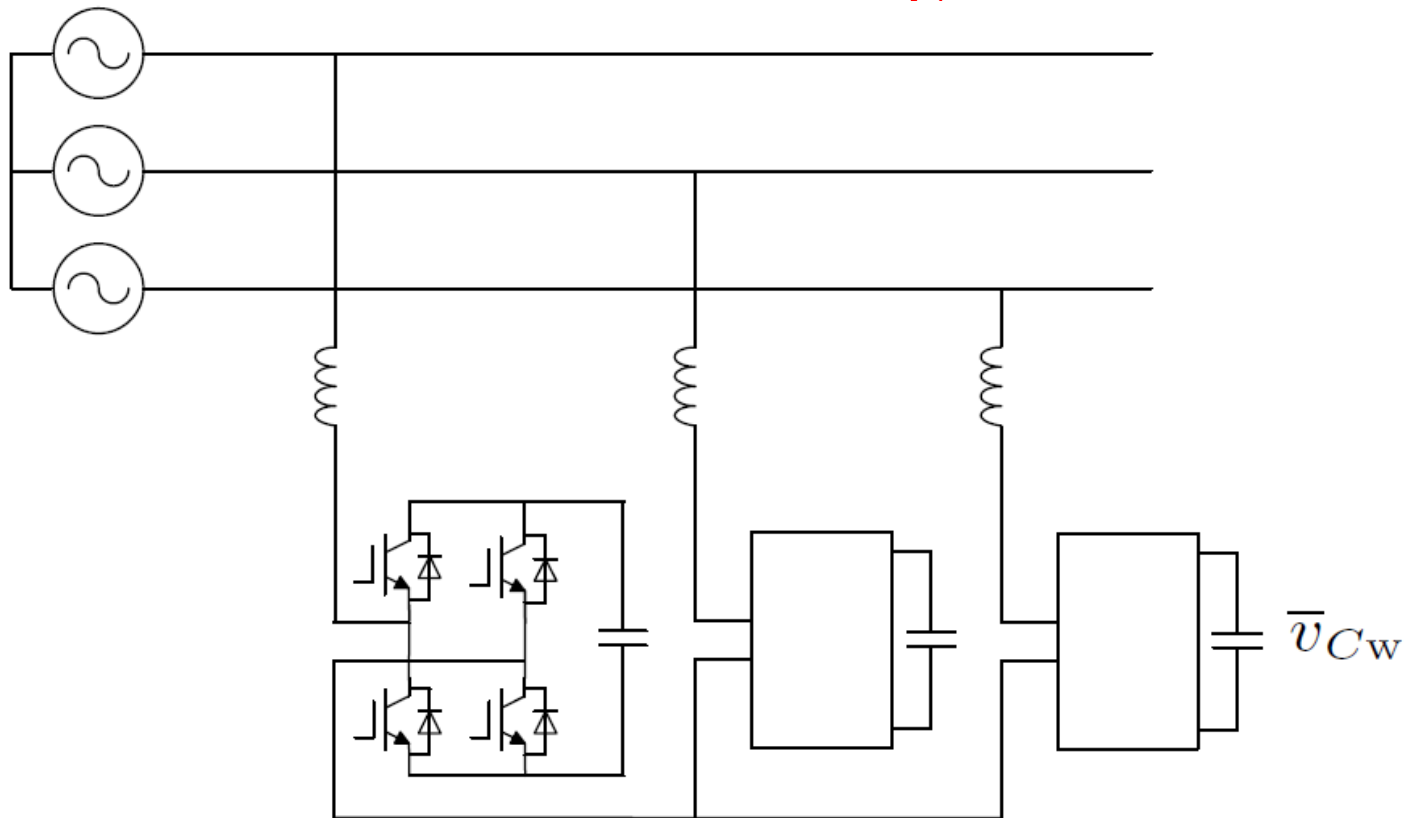
The single dc capacitor voltage:

Arithmetic average of all the dc capacitor voltages.



# Middle Layer in Hierarchy Control

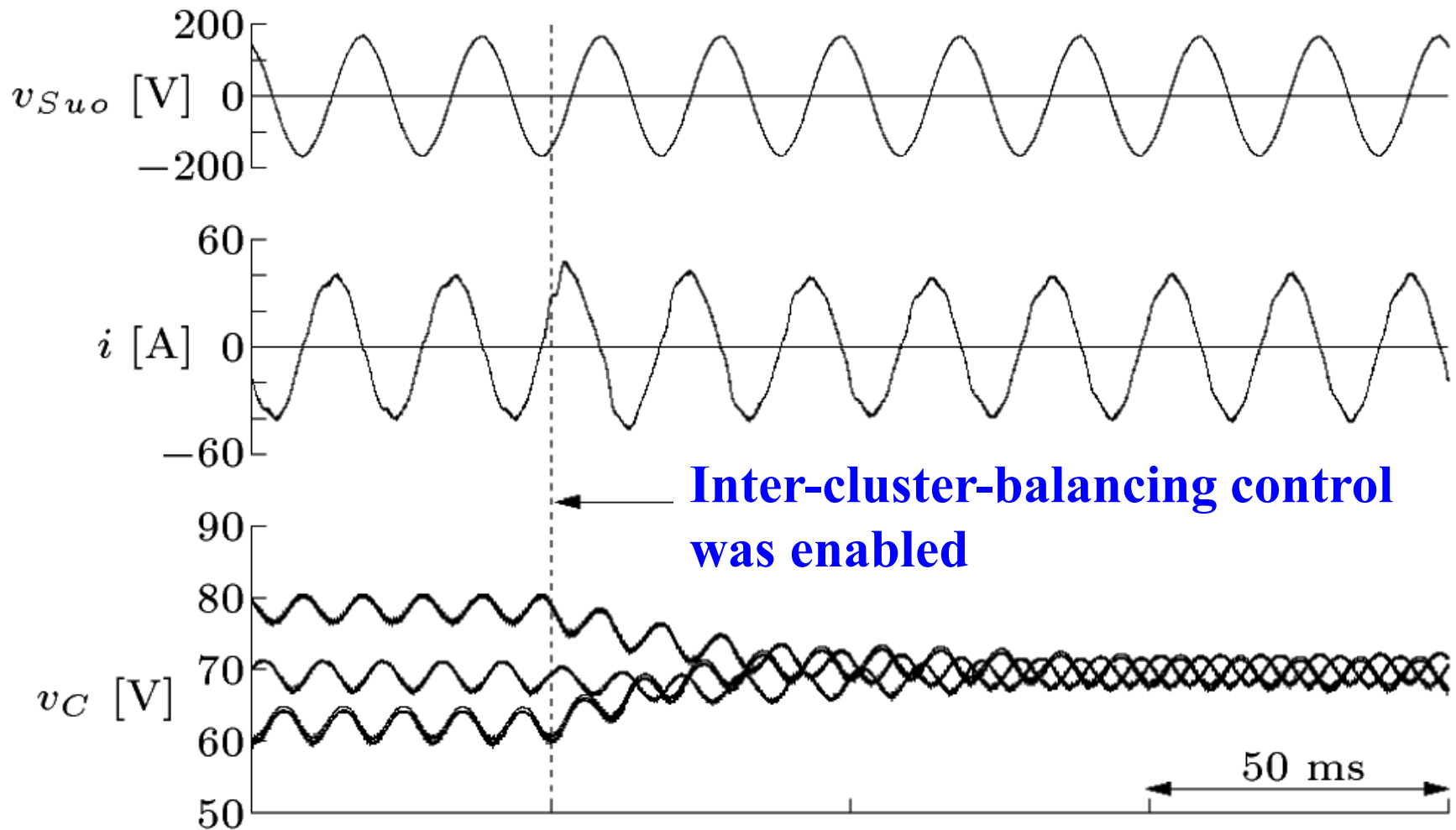
## Inter-Cluster-Balancing Control



The single capacitor voltage in each bridge cell:  
Arithmetic average of all the capacitor voltages in each cluster



# Effect of Inter-Cluster-Balancing Control



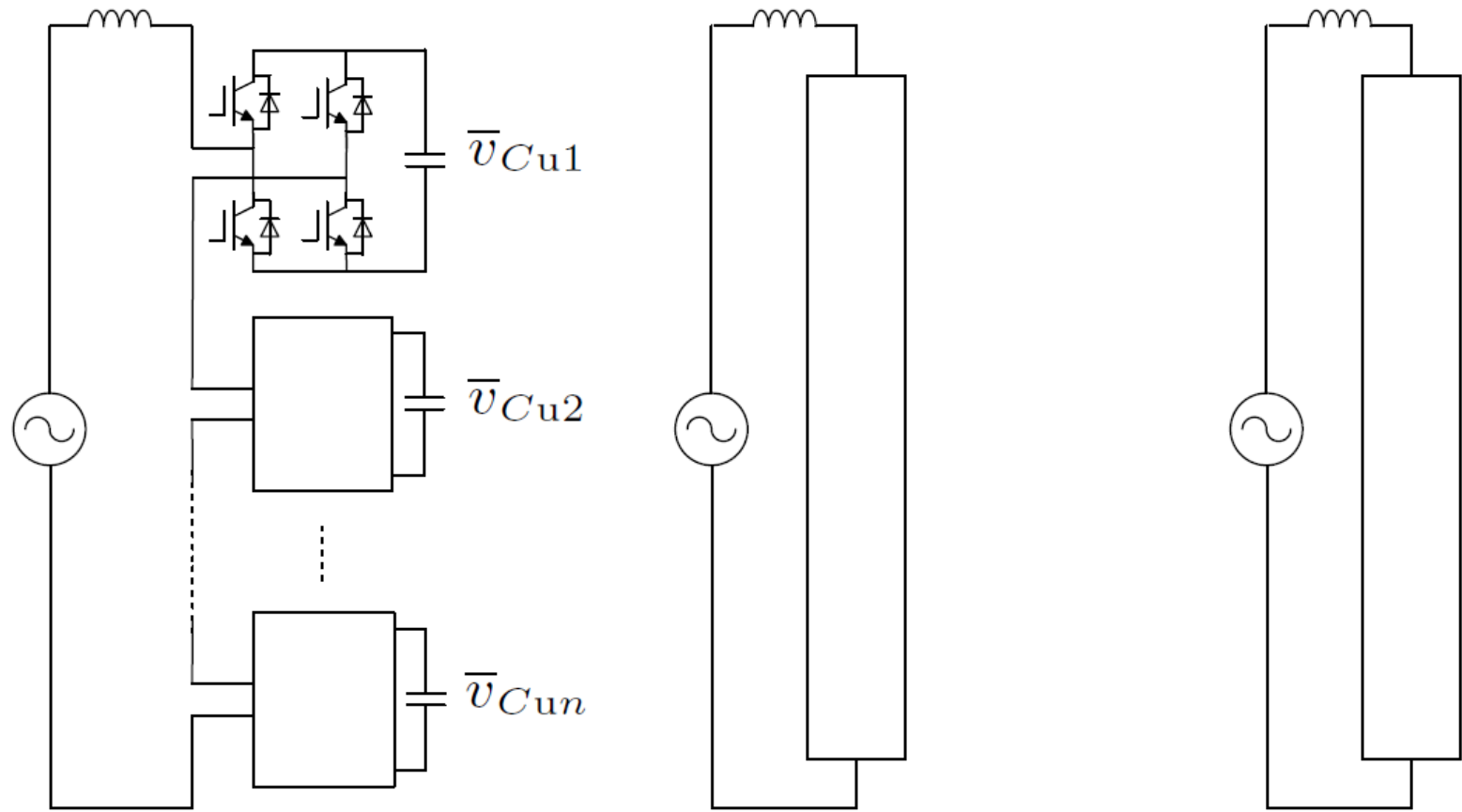
**Inter-cluster-balancing control  
was enabled**

**Intra-cluster-balancing control remained enabled**



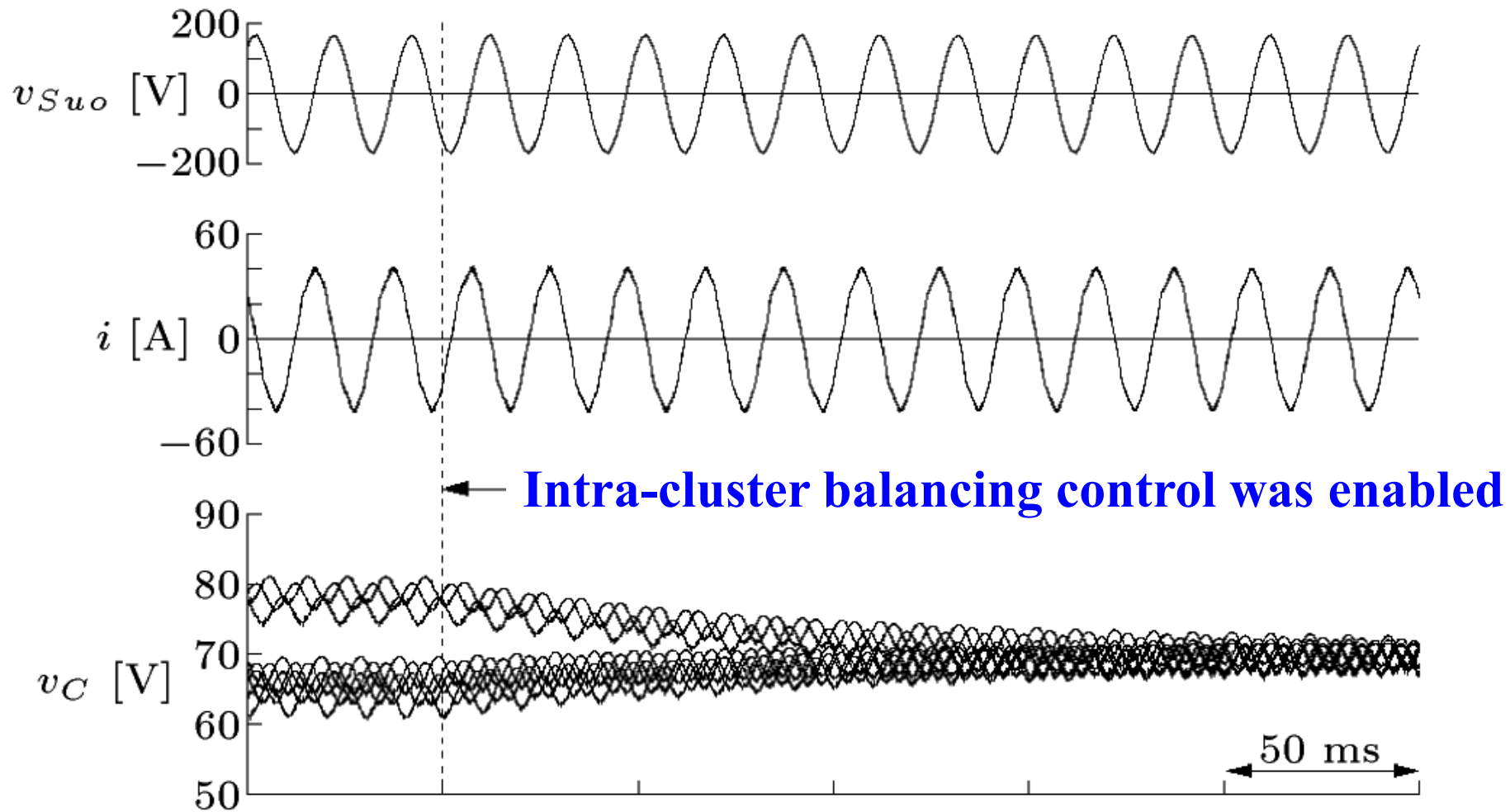
# Bottom Layer in Hierarchy Control

## Intra-Cluster-Balancing Control



Voltage balancing inside each cluster, independent of the three clusters

# Effect of Intra-Cluster-Balancing Control



**Inter-clustered balancing control remained enabled**



# DSCC-Based BTB(Back-To-Back) System with Phase-Shifted-Carrier PWM

---

DSCC: Double-Star Chopper Cells  
Key Concept: “Circulating Current”

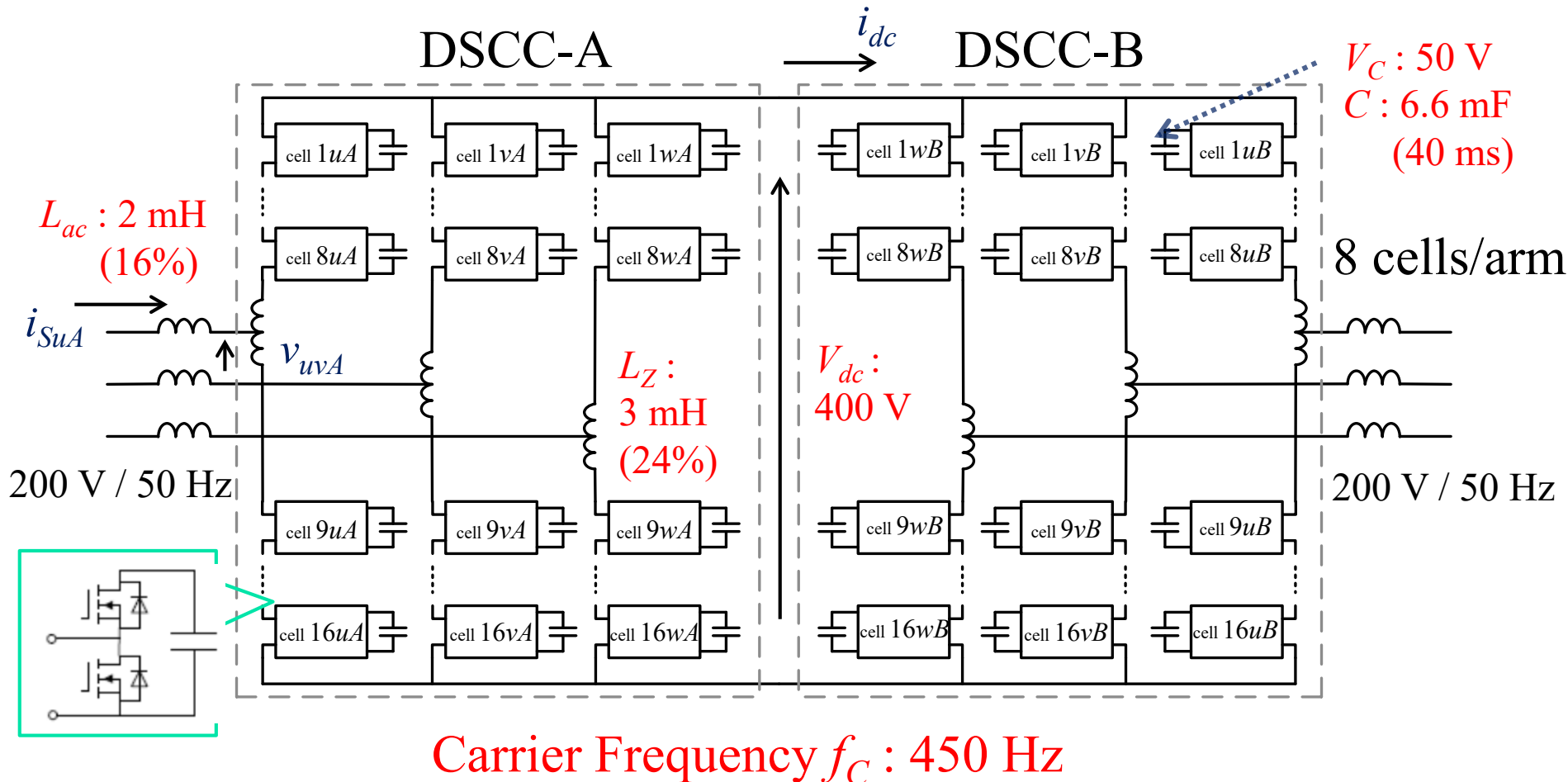
K. Sekiguchi, P. Khamphkdi, M. Hagiwara, and H. Akagi, “A grid-level high-power BTB (back-to-back) system using modular multilevel cascade converters without dc-link capacitor,” *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2648-2659, Jul./Aug. 2014



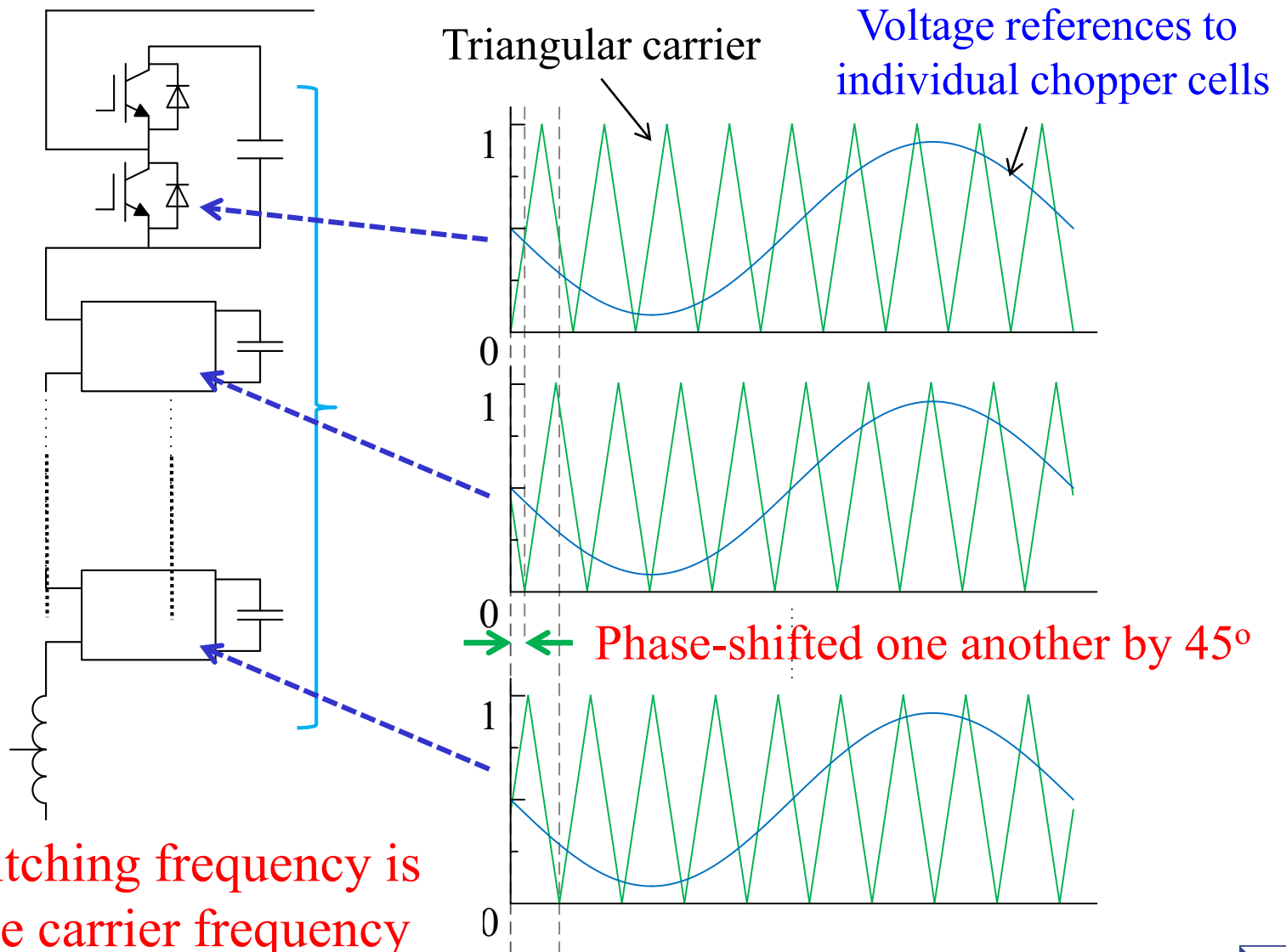


# Downscaled Model Rated at 400 Vdc and 10 kW

## Neither DC-Link Capacitor nor DC Voltage Sensor



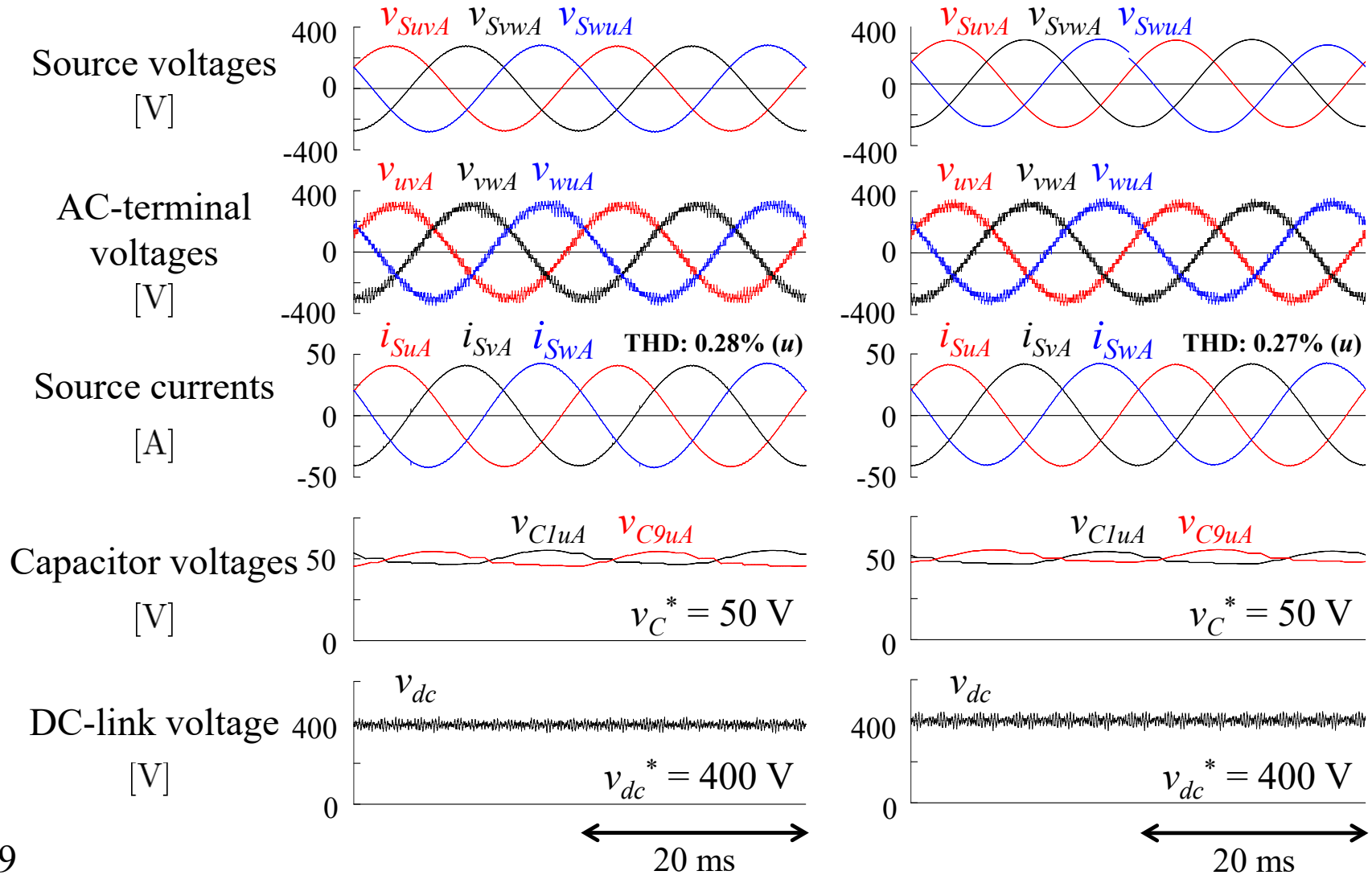
# Phase-Shifted-Carrier PWM in Eight Chopper Cells per Arm



# Steady State at 8.7 kW and 5.0 kvar (Capacitive)

## Experiment

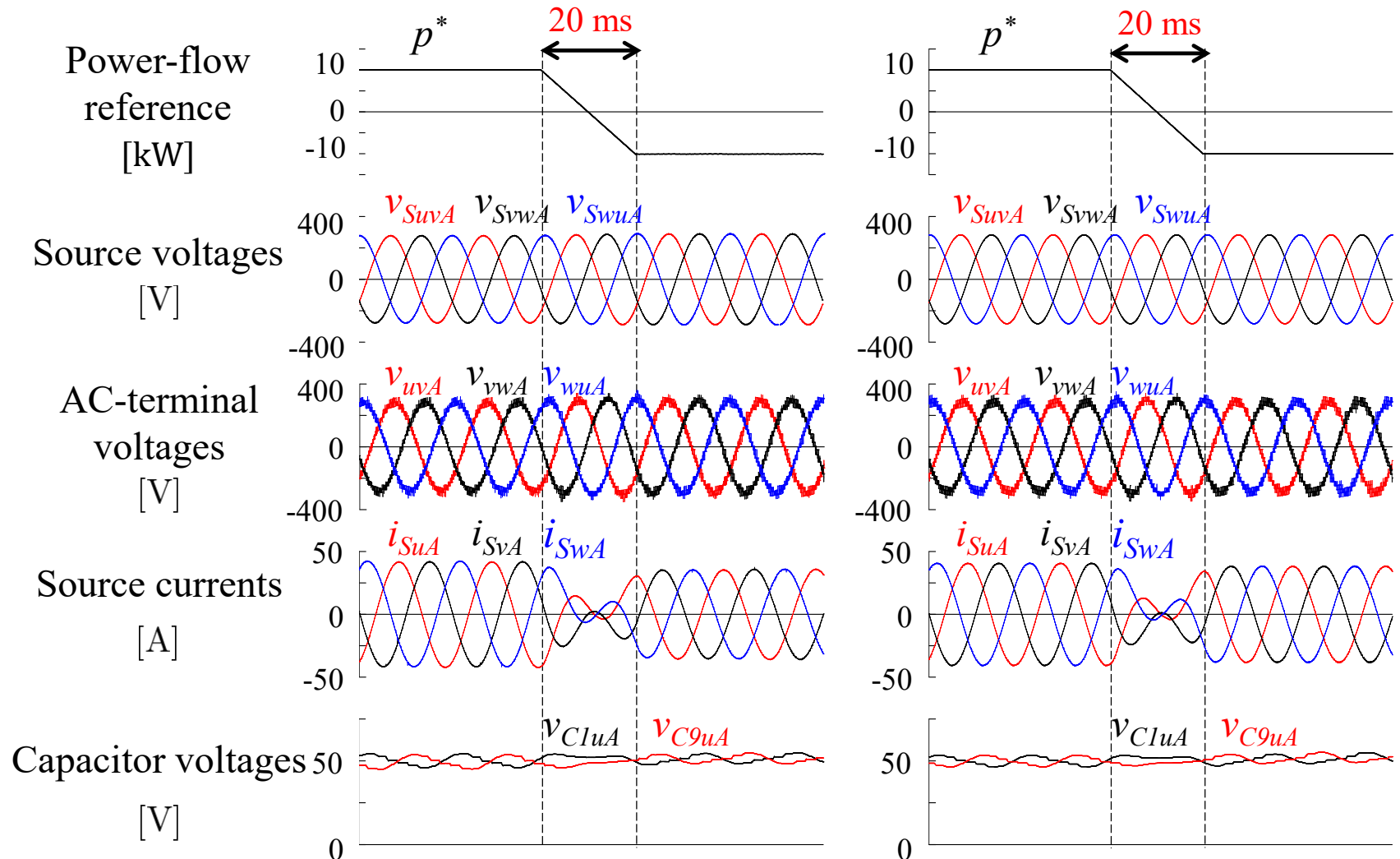
## Simulation



# Transition State: $p^* = \pm 10 \text{ kW}$ and $q^* = 0$

## Experiment

## Simulation



# What Brought the **Concept of Circulating Currents** to the DSCC Converters with Phase-Shifted-Carrier PWM?

DSBC: Double-Star Chopper Cells

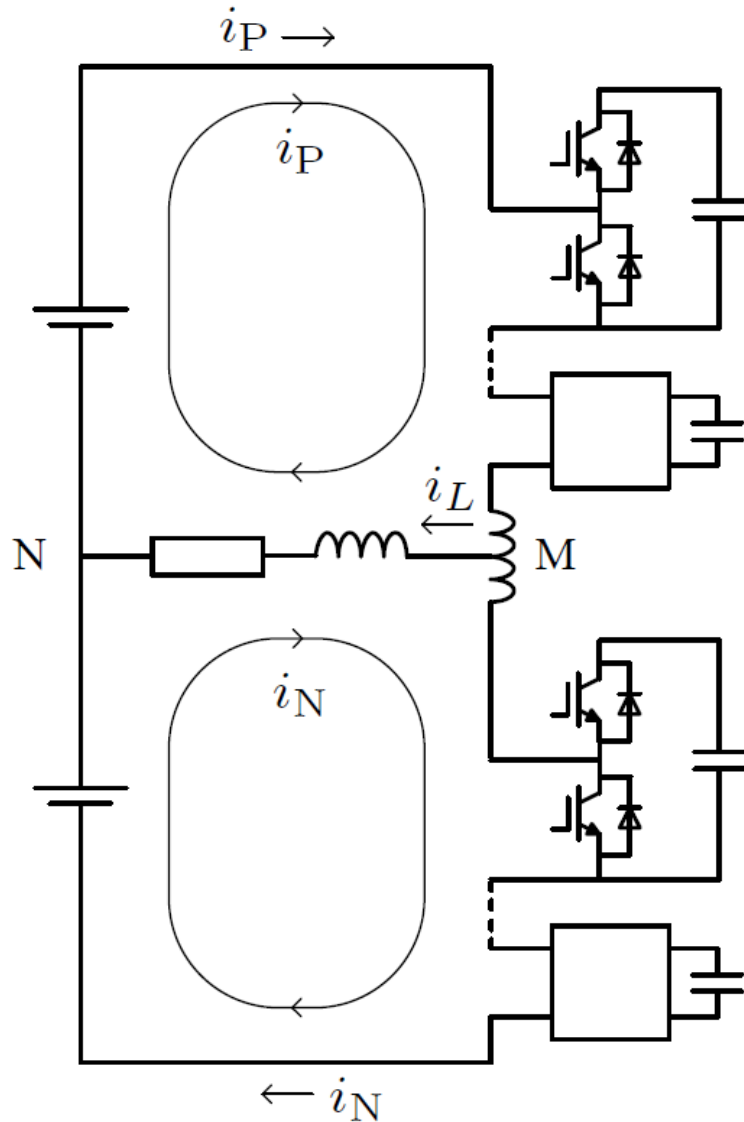
Similarity and Analogy between a Line-Commutated Cycloconverter with Circulating-Current Mode and a DSCC Converter

H. Akagi, “What led to success in academic research on the family of modular multilevel cascade converters,” ECCE-Asia/IPEC-Niigata, pp. 2353-2359, 2018.

H. Akagi, “A review of developments in the family of modular multilevel cascade converters,” IEEJ (IEE of Japan) Transactions, vol. 13, pp. 12222-1235, 2018. (invited review paper)



# Two Independent Loop Currents $i_P$ and $i_N$



DSCC inverter per leg

Applying KCL at point M

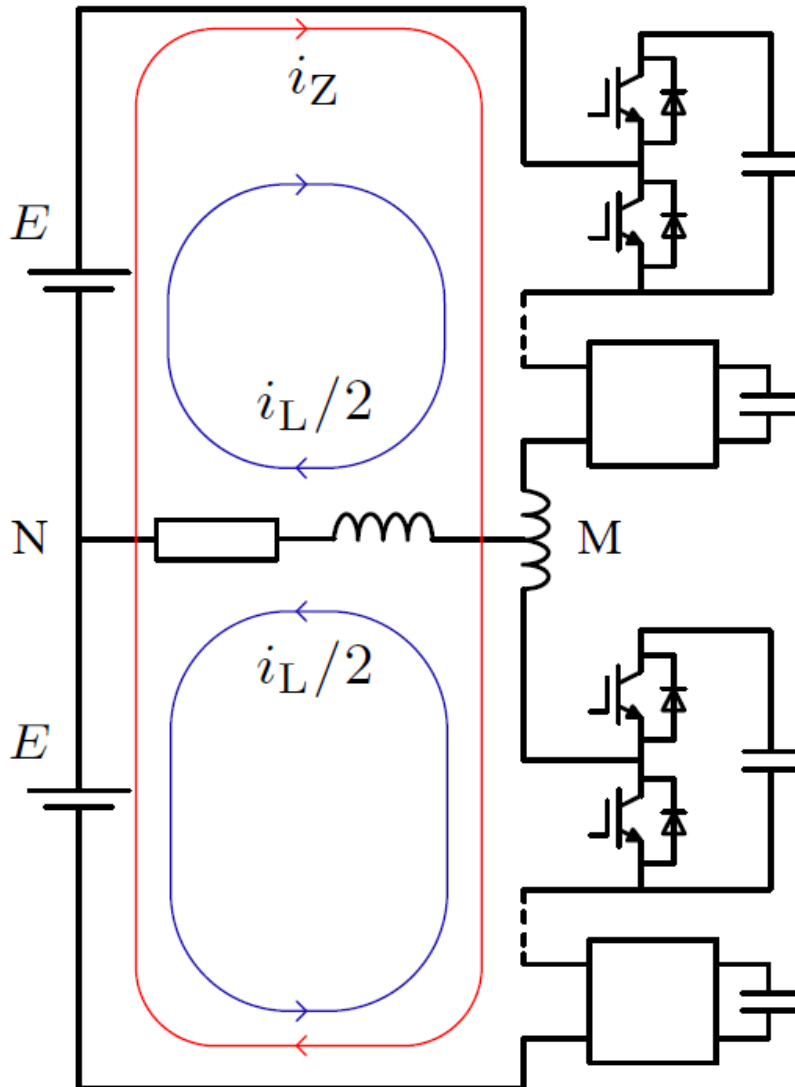
$$i_L = i_P - i_N$$

Two independent currents among  $i_L$ ,  $i_P$ , and  $i_N$

Selecting a pair of  $i_P$  and  $i_N$  **failed** in capacitor-voltage balancing.



# Two Independent Loop Currents, $i_Z$ and $i_L$



Selecting a pair of  $i_Z$  and  $i_L$  succeeded in capacitor-voltage balancing.

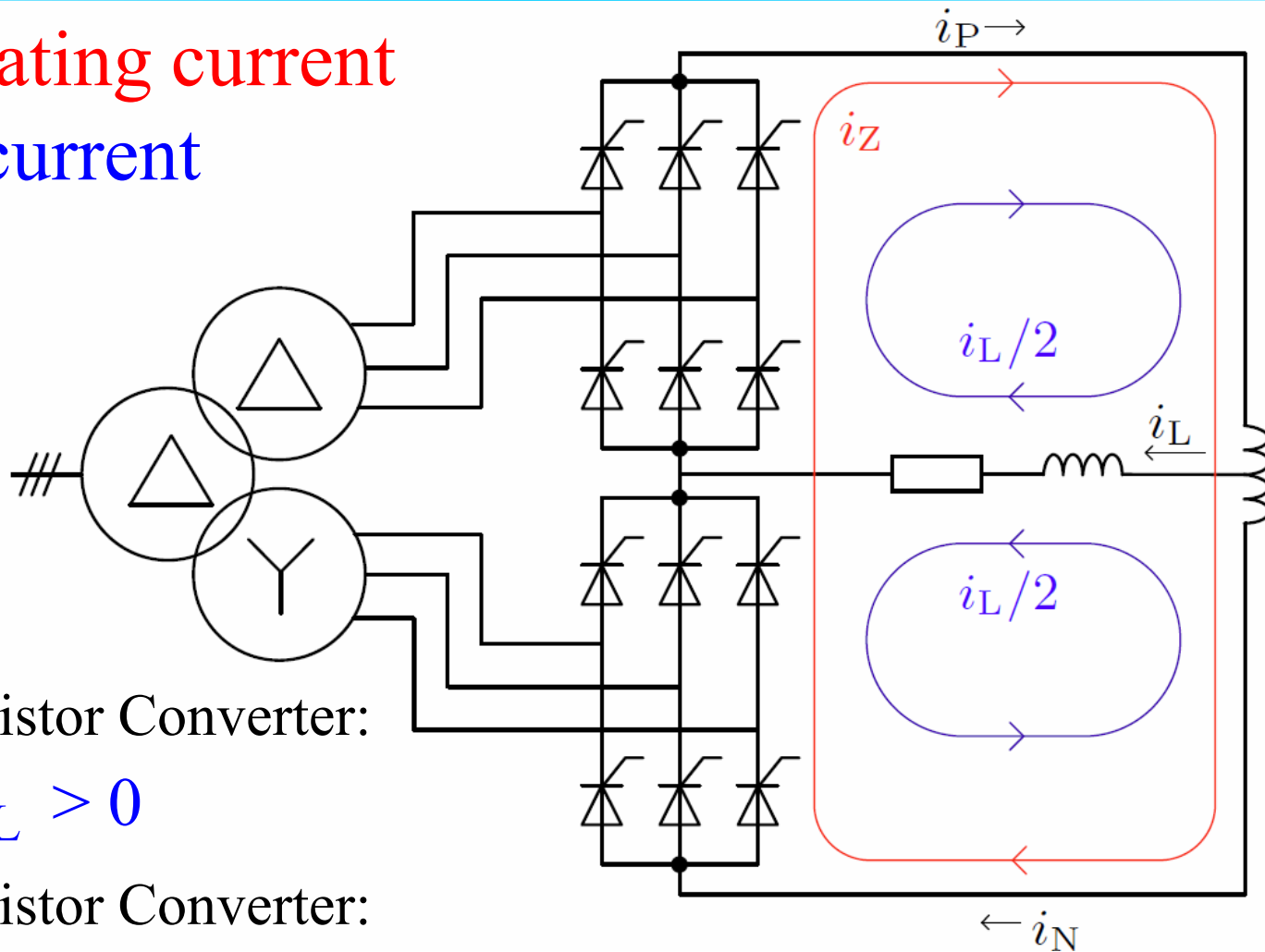
What triggered off this selection?



# A Cycloconverter with Circulating-Current Mode

$i_Z$  : Circulating current

$i_L$  : Load current



Positive Thyristor Converter:

$$i_P = i_Z + i_L > 0$$

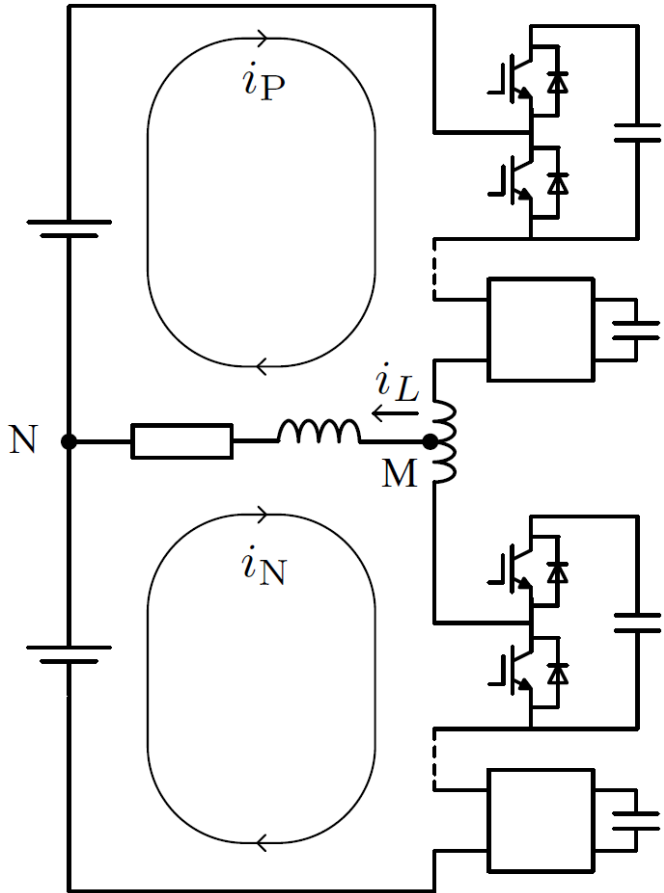
Negative Thyristor Converter:

$$i_N = i_Z - i_L > 0$$

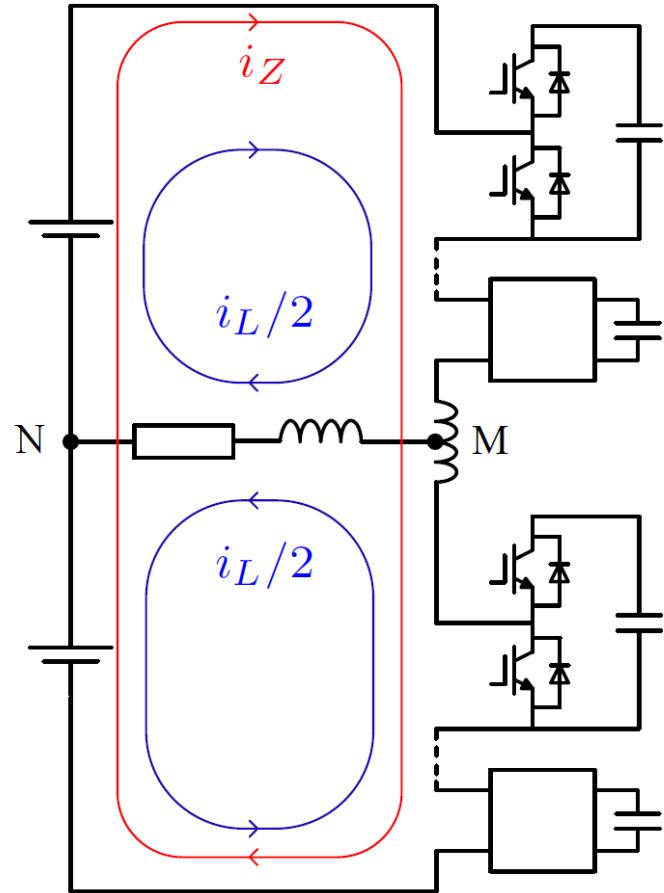




# One pair of $i_P$ and $i_N$ , and the other of $i_Z$ and $i_L$



$i_P$  and  $i_N$



$i_Z$  and  $i_L$



# Reversible Linear Transformation

The relation between a pair of  $i_P$  and  $i_N$  and that of  $i_Z$  and  $i_L$

$$\begin{bmatrix} i_L \\ i_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} i_P \\ i_N \end{bmatrix}$$

The determinant of the two-dimensional matrix is **unity**.

$$\begin{aligned} \begin{bmatrix} i_P \\ i_N \end{bmatrix} &= \begin{bmatrix} 1 & -1 \\ 0.5 & 0.5 \end{bmatrix}^{-1} \begin{bmatrix} i_L \\ i_Z \end{bmatrix} \\ &= \begin{bmatrix} 0.5 & 1 \\ -0.5 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ i_Z \end{bmatrix} \end{aligned}$$



# Tomorrow's AC-Link Multi-Drive System

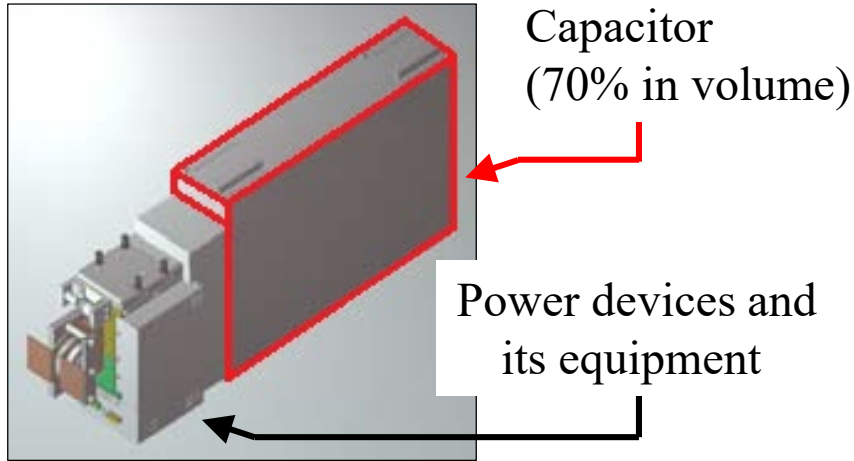
---

Y. Okazaki and H. Akagi,  
“Feasibility Study of a Modular Multilevel DSBC Conversion System  
Equipped With Medium-Frequency Isolation Transformers for Driving  
Multiple Medium-Voltage Motors,”  
IEEJ Transactions on Industry Applications, vol. 136, no. 12, pp. 1005-1014,  
Dec. 2016. (in Japanese)



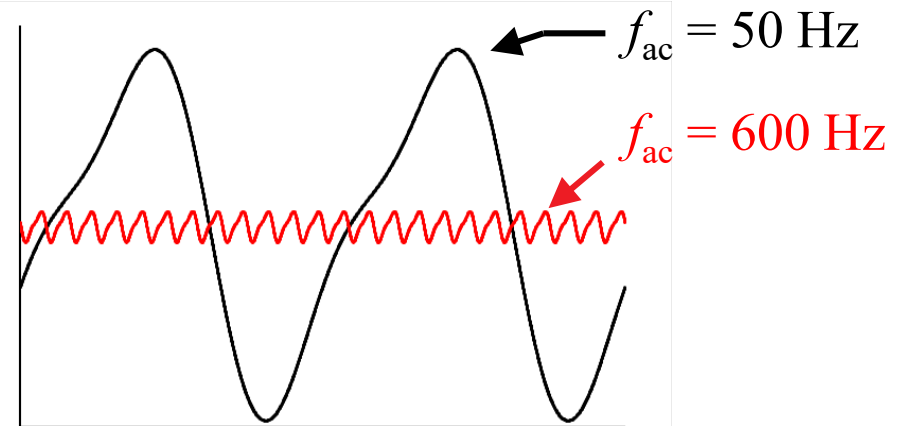
# How to Reduce the Capacitor Size in MMC or DSCC

Chopper cell  
at  $f_{ac} = 50$  Hz



[www.energy.siemens.com](http://www.energy.siemens.com)  
Siemens HVDC Plus

Capacitor voltage waveforms



Voltage fluctuations  $\propto 1/(C f_{ac})$

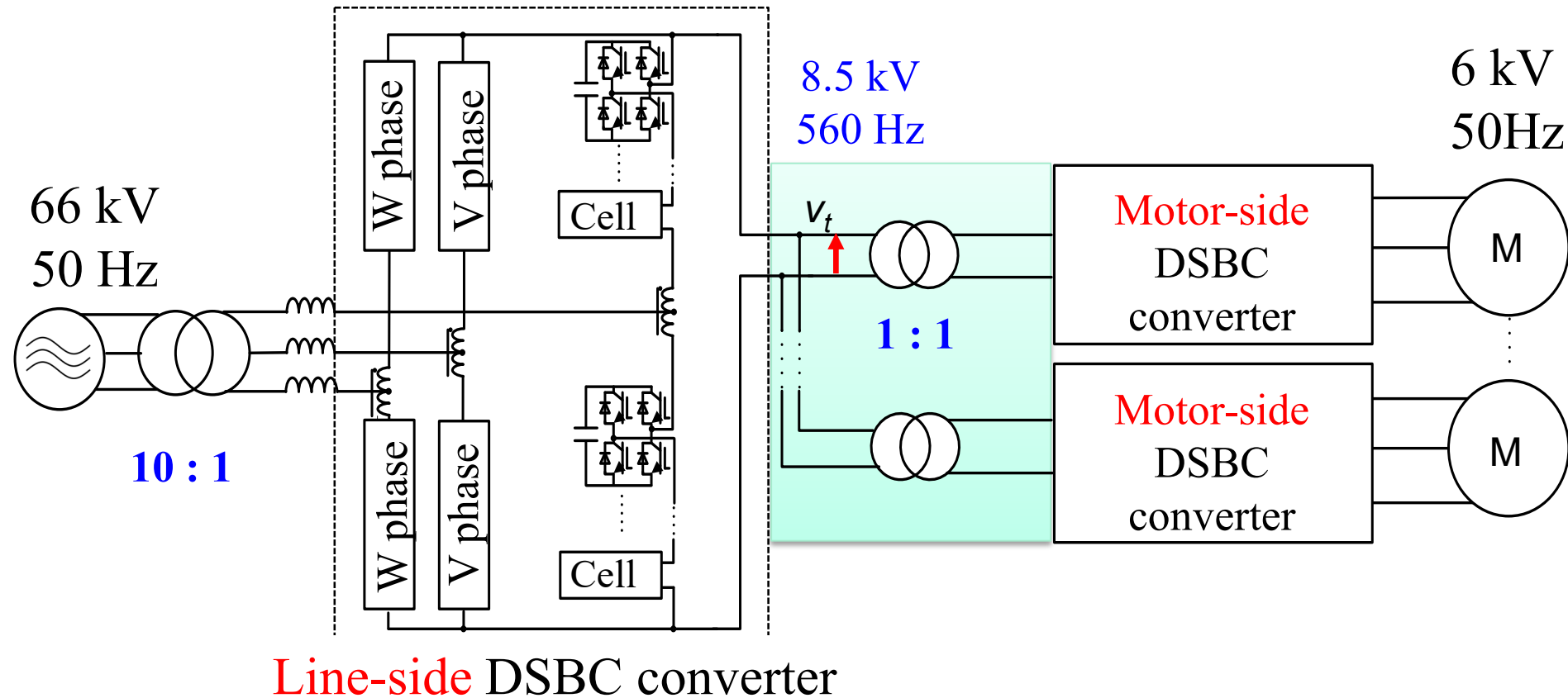
$f_{ac}$ : Inverter ac frequency

$C$ : Capacitance value

Making the ac frequency  $f_{ac}$  higher is accompanied by reducing the capacitor size.



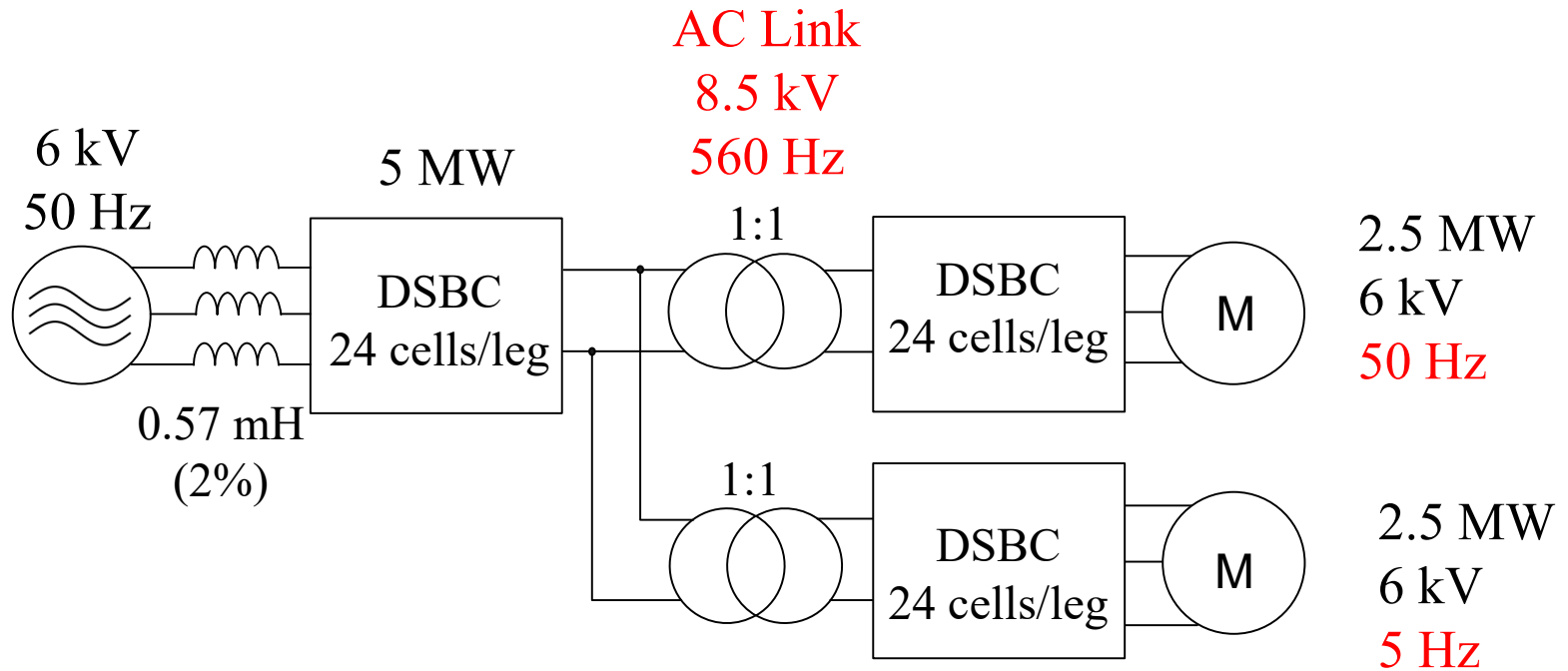
# Tomorrow's AC-Link Multi-Drive System



Each motor is galvanically isolated from the others as well as the ac mains.



# A Basic System Configuration for Simulation



## Simulation Conditions

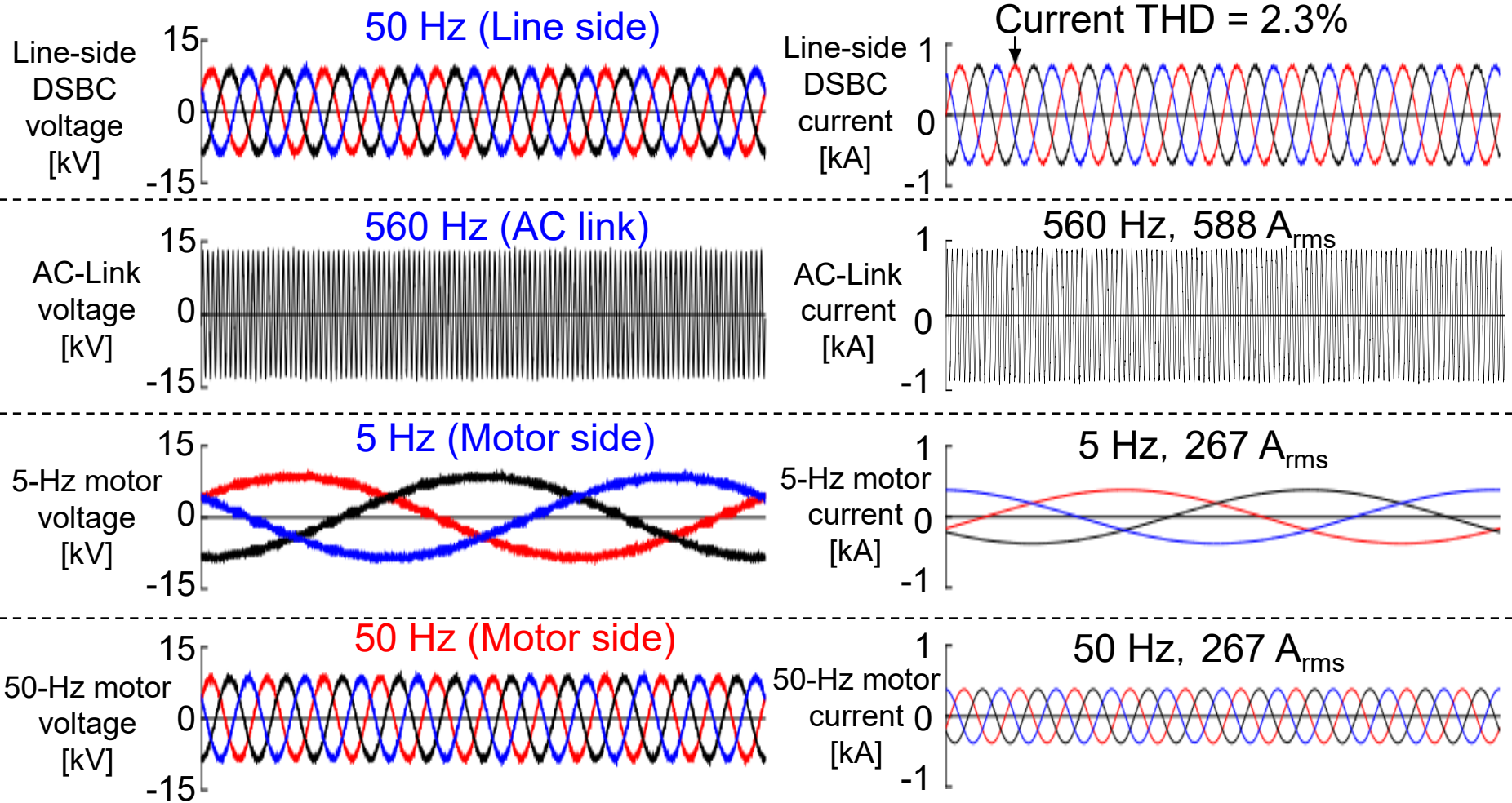
Switching devices: 1.7-kV IGBTs

Each triangular carrier frequency: 1 kHz

Equivalent carrier frequency: 48 kHz



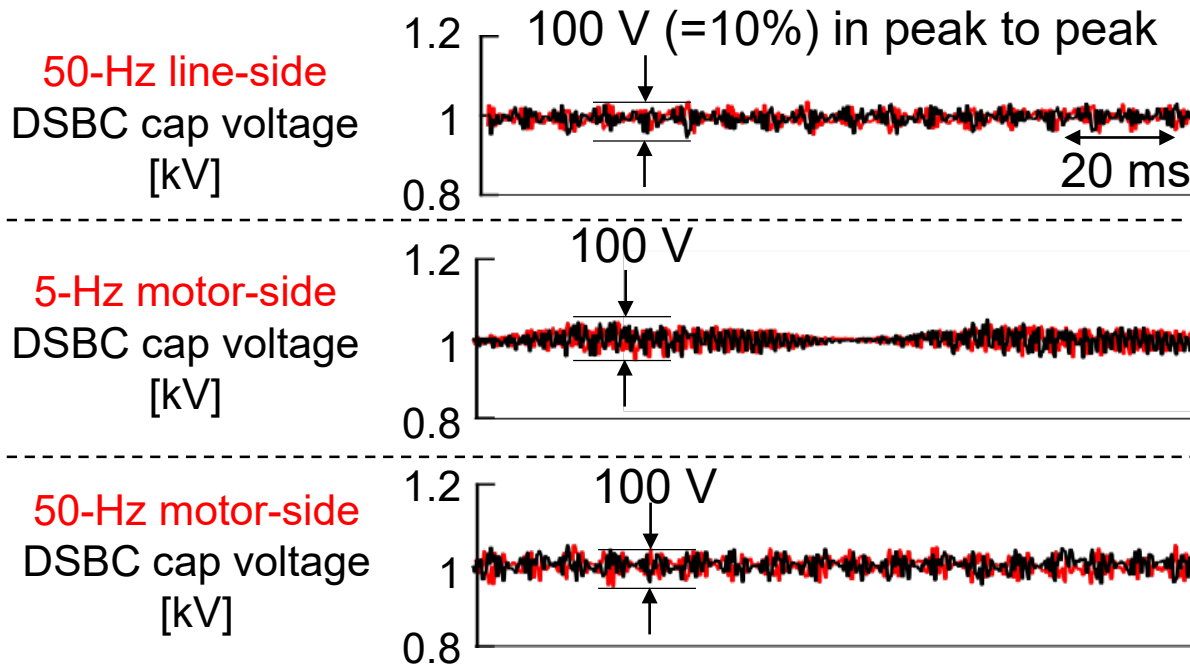
# Simulated Waveforms of the three DSBC Converters



“Decoupled control” was confirmed among the three DSBC converters.



# Simulated Waveforms of DC Capacitor Voltages



Unit capacitance constant: 20 ms

The capacitor size can be reduce practically to 1/10 or more, compared to that of an ac-link frequency of 50 Hz.





# Conclusion

---

What has led to success in research on the modular multilevel cascade converters?

## 1. Phase-Shifted-Carrier PWM:

Actual switching frequency equal to carrier frequency.

## 2. Hierarchy Control:

Easy expansion to any bridge-cell or chopper-cell count.

## Tomorrow's AC-Link Multi-Drive System:

Capable of galvanic isolation and voltage matching

