Gate Interface Reliability in SiC/GaN Power Devices

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CONTENTS/OUTLINE

Silicon Carbide MOSFETs

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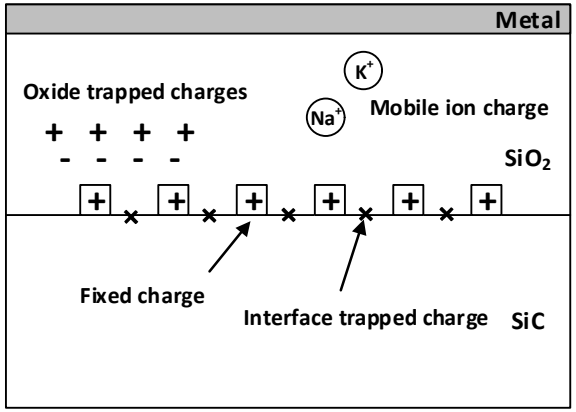
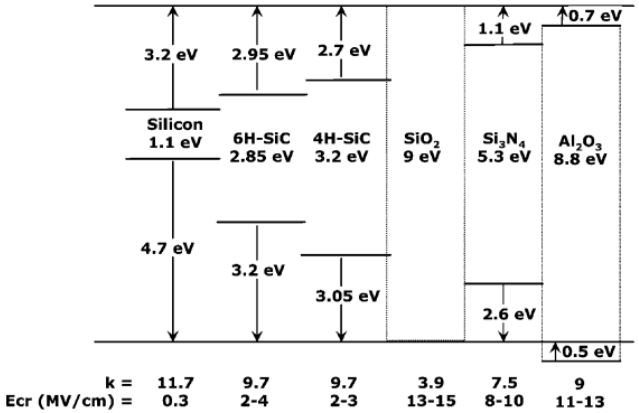
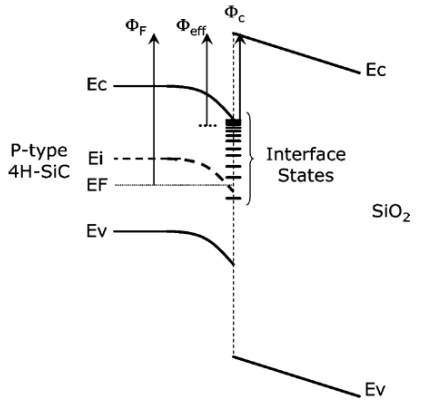
- **Introduction**
- Characterizing BTI using 3rd Quadrant Characteristics
- Characterizing BTI using Crosstalk

INTRODUCTION TO OXIDE RELIABILITY

- Gate oxide has been/was a reliability concern in SiC MOSFETs
- Semiconductor-oxide interface
  - SiC/SiO_2 is not Si/SiO_2 (more complex)
  - Wider bandgap of SiC (3.3 eV) and narrower band offsets to the dielectric
  - Existence of carbon
  - Interface and near oxide trap density D_{it} in SiC/SiO_2 is 100x D_{it} in Si/SiO_2







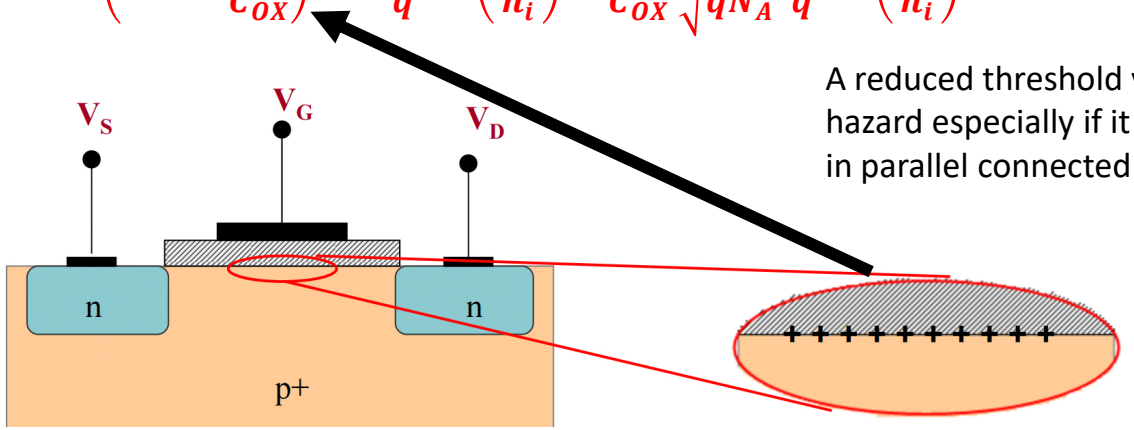
T. Aichinger, et al. "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability,* vol. 80, pp. 68-78, 2018.

INTRODUCTION TO OXIDE RELIABILITY

- The oxide interface between SiC and SiO_2 is not as reliable as that between Si and SiO_2.

- Fixed oxide and interface traps capture electrons during positive bias and holes during negative bias. This causes a shift in V_{TH} which is detrimental to device reliability.

$$V_{TH} = \left(\emptyset_{MS} - \frac{Q_f}{C_{OX}}\right) + 2\frac{kT}{q} ln\left(\frac{N_A}{n_i}\right) + \frac{qN_A}{C_{OX}}\sqrt{\frac{4\varepsilon}{qN_A}\frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)}$$



A reduced threshold voltage is a circuit hazard especially if it occurs unevenly in parallel connected devices.

Simplified MOSFET diagram showing MOS interface

INTRODUCTION

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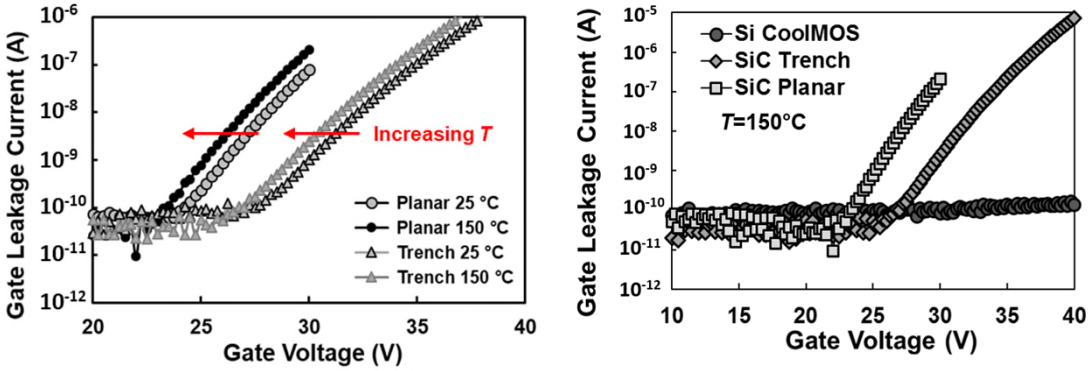
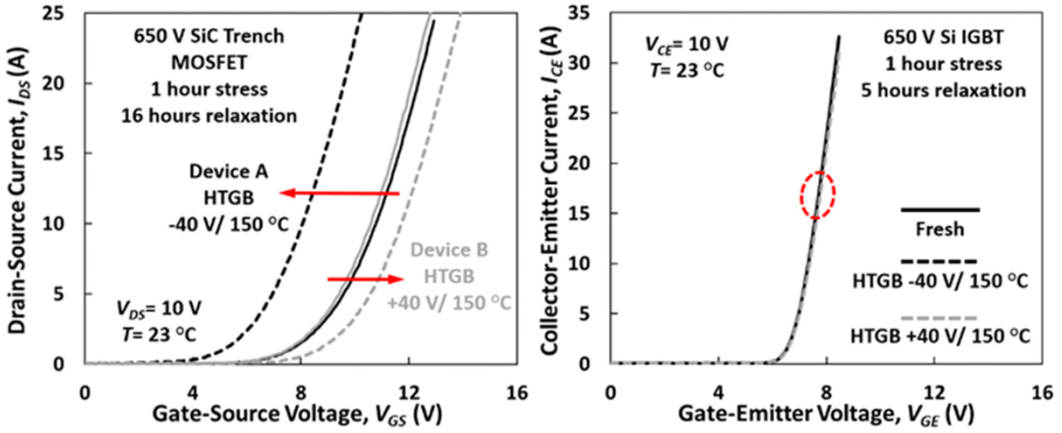
- Different studies had shown a reduced reliability of the gate oxide of SiC MOSFETs
- Just some examples. There are MANY more.
  - R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs," *Japanese Journal of Applied Physics,* vol. 55, no. 4S, p. 04EA03, 2016. (FREE ARTICLE)
  - M. Beier-Moebius and J. Lutz, "Breakdown of Gate Oxide of SiC-MOSFETs and Si-IGBTs under High Temperature and High Gate Voltage," PCIM Conference, 2017
  - T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability,* vol. 80, pp. 68-78, 2018.
  - K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Understanding BTI in SiC MOSFETs and its impact on circuit operation," *IEEE Trans. on Device and Materials Reliability*, vol. 18, no. 2, pp. 144 - 153, 2018.
  - K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability," *IEEE Trans. on Electron Devices*, vol. 66, no. 11, pp. 4604-4616, 2019.

INTRODUCTION TO OXIDE RELIABILITY

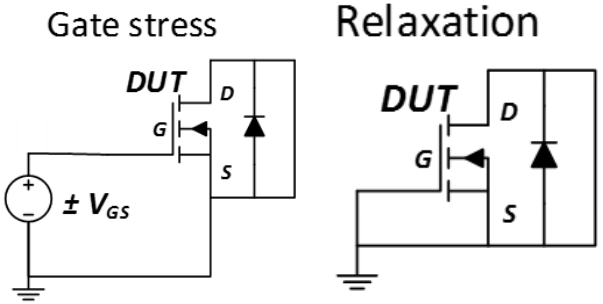


Gate Oxide Breakdown characteristics for Si/SiC MOSFETs



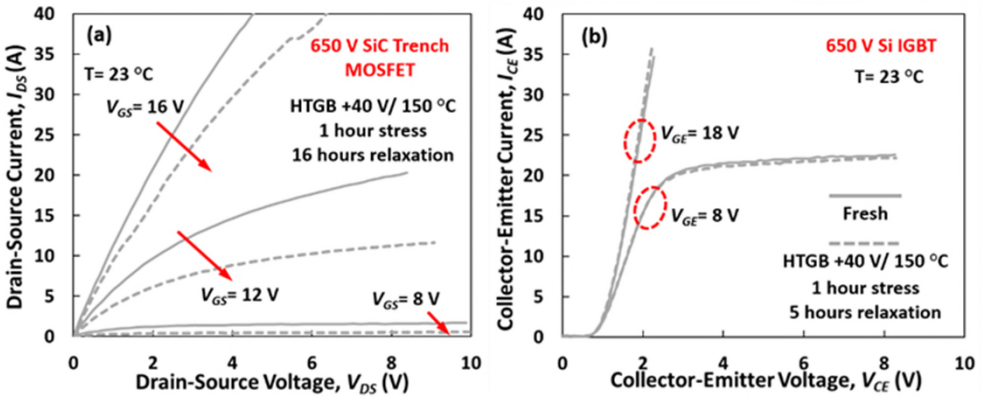
SiC and IGBT Gate Transfer characteristics before and after BTI Stressing

- Accelerated stress tests are performed to investigate the extent of BTI in power MOSFETs/IGBTs
- Stress tests can be with positive or negative gate voltages

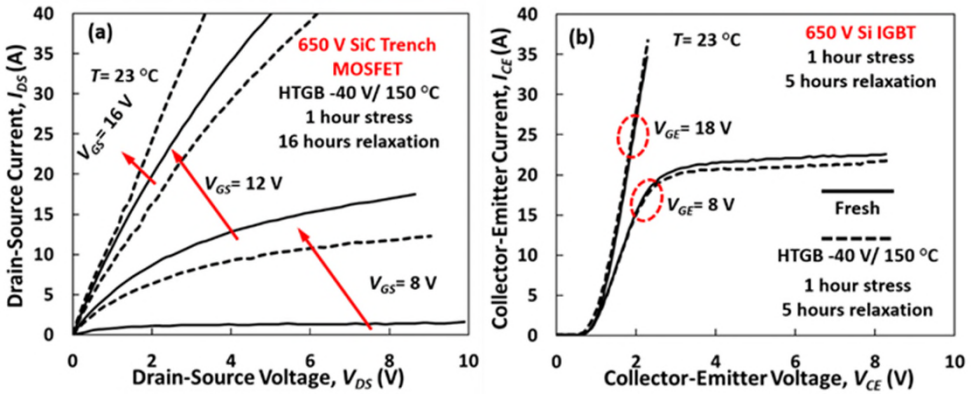


J. O. Gonzalez and O. Alatise, 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 837-844.

IMPACT OF BTI ON OUTPUT CHARACTERISTICS



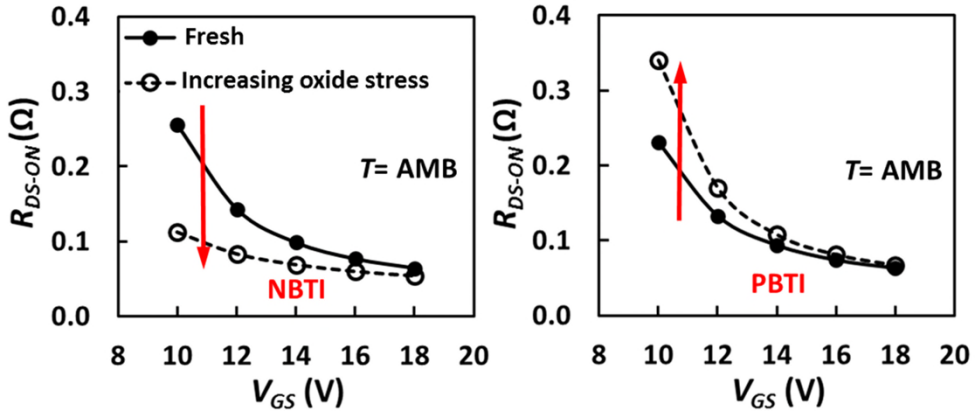
Impact of PBTI on the output characteristics of SiC and silicon IGBT



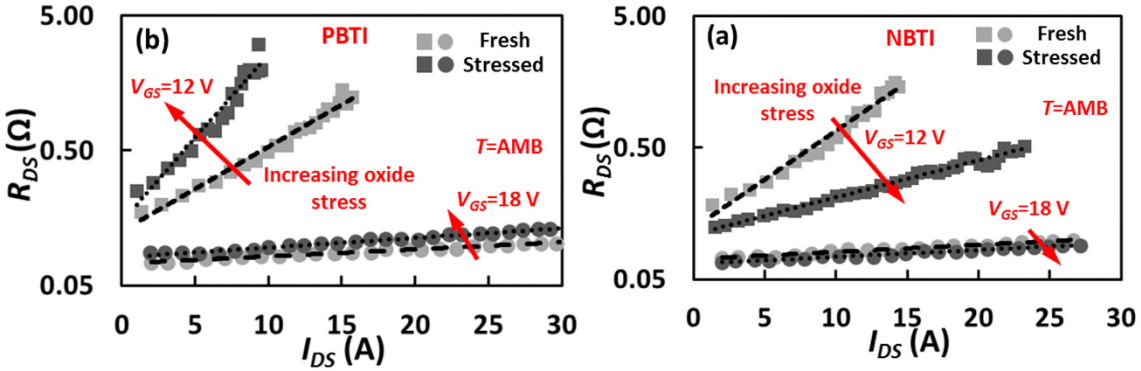
Impact of NBTI on the output characteristics of SiC MOSFET and silicon IGBT

- When a positive V_{GS} stress is applied, negative charges are trapped in the oxide causing V_{TH} increase. This is called PBTI.
- When a negative V_{GS} stress is applied, positive charges are trapped in the oxide causing V_{TH} decrease. This is called NBTI.
- The impact of V_{TH} shift is to change the output and transfer characteristics of the device.
- The phenomenon occurs in silicon devices however, to a much reduced extent. In SiC, it is a more critical problem due to the lower quality oxide interface.

IMPACT OF BTI ON ON-STATE RESISTANCE



Impact of NBTI and PBTI on R_{DSON} vs V_{GS} characteristics



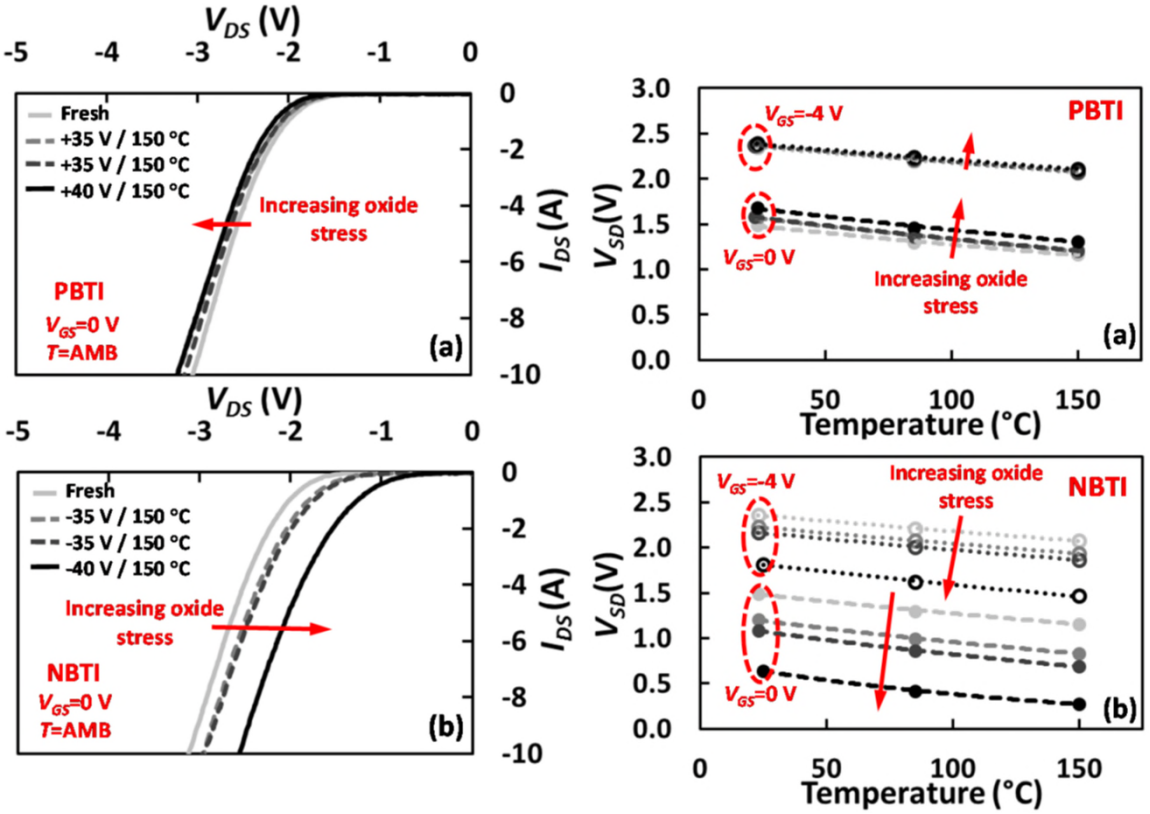
Impact of PBTI and NBTI on R_{DSON}

- For the SiC MOSFET, ON-state resistance increased under P-HTGB and reduced with N-HTGB
- This compromises R_{DSON} as a TSEP
- It is more apparent at lower V_{GS} because of the increased share of the channel resistance.

$$R_{DSON} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS} - V_{TH})} + \frac{L_{drift}}{q\mu N_D A}$$

J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018.

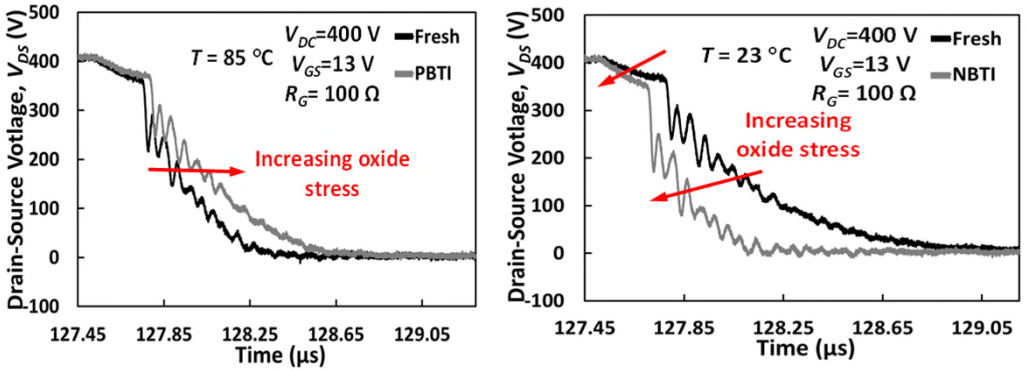
IMPACT OF BTI ON 3RD QUADRANT CHARACTERISTICS



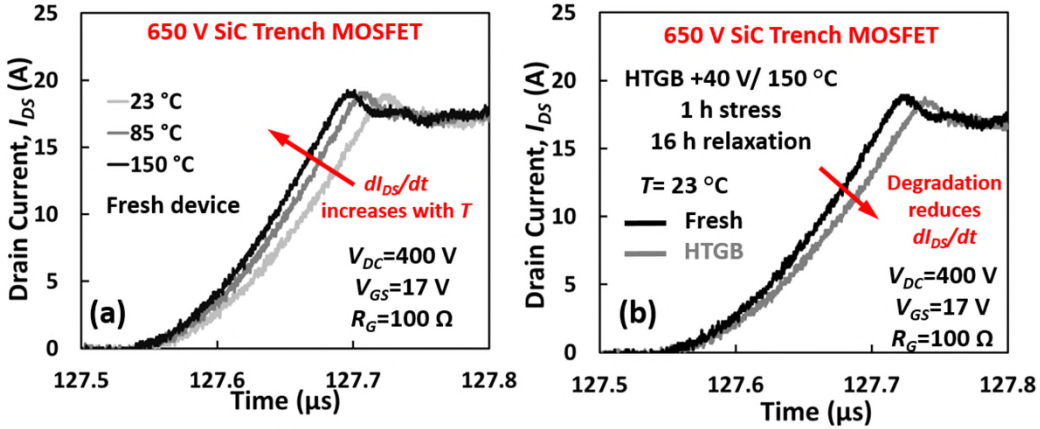
Impact of NBTI and PBTI on 3rd quadrant characteristics of SiC MOSFETs

- The change in V_{TH} affects the 3rd quadrant (body diode) characteristics.
- 3rd quadrant characteristics are more affected by NBTI than PBTI.
- This is because increasing V_{TH} reduces subthreshold conduction and hence, reduces the V_{SD} dependence on V_{GS}.
- The temperature sensitivity of V_{SD} should account

IMPACT OF BTI ON 3RD SWITCHING TRANSIENTS



Impact of NBTI and PBTI on drain voltage transients in SiC MOSFETs



Impact of NBTI and PBTI on drain current transients in SiC MOSFETs

- The change in V_{TH} affects the turn-ON and turn-OFF V_{DS} and I_{DS} transients.
- PBTI causes delayed transients during turn-ON due to increase in V_{TH}.
- NBTI causes accelerated transients during turn-ON due to reduction in V_{TH}.

$$\frac{dI_{DS}}{dt} = \frac{\beta V_{GG}(V_{GS} - V_{TH})e^{-\frac{t}{R_G(C_{GS}+C_{GD})}}}{R_G(C_{GS}+C_{GD})}$$

$$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{GP}}{R_G C_{GD}}$$

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- Characterizing BTI using Crosstalk

CHARACTERIZING BIAS TEMPERATURE INSTABILITY

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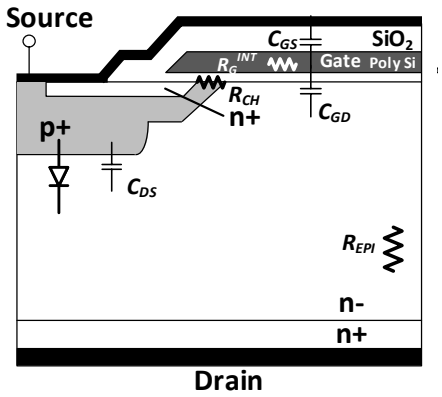
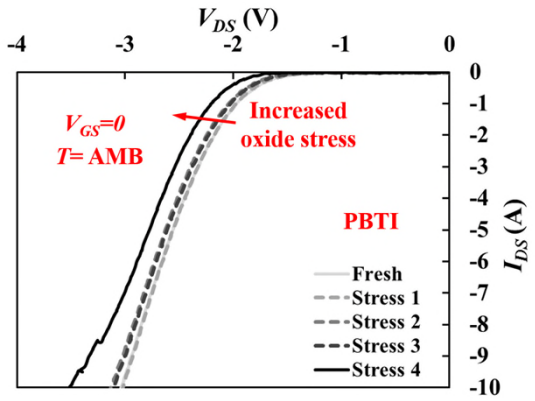
- Some methods are proposed in:
  - D. B. Habersat, A. J. Lelis, and R. Green, "Measurement considerations for evaluating BTI effects in SiC MOSFETs," Microelectronics Reliability, vol. 81, pp. 121-126, 2018
  - G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser, "Preconditioned BTI on 4H-SiC: Proposal for a Nearly Delay Time-Independent Measurement Technique," IEEE Trans. on Electron Devices, vol. 65, no. 4, pp. 1419-1426, 2018.
  - K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Understanding BTI in SiC MOSFETs and its impact on circuit operation," IEEE Trans. on Device and Materials Reliability, vol. 18, no. 2, pp. 144 - 153, 2018.
  - K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability," IEEE Trans. on Electron Devices, vol. 66, no. 11, pp. 4604-4616, 2019.
- Role of V_{TH} shift in power cycling has also been evaluated
  - H. Luo, F. Iannuzzo and M. Turnaturi, "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 2, pp. 1657-1667, June 2020,

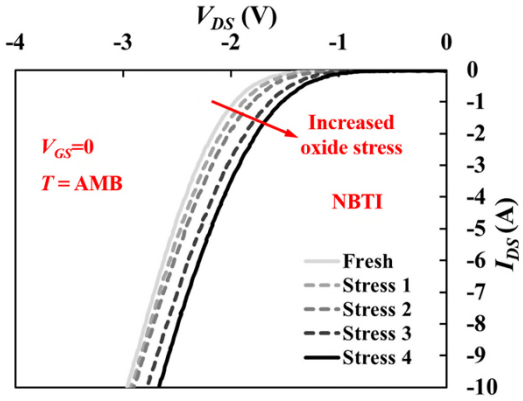
CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT

- Body diode voltage – 3rd quadrant characteristics
  - Current flowing through the channel due to partial turn-ON during reverse conduction when V_{GS}=0



MOSFET with Body diode





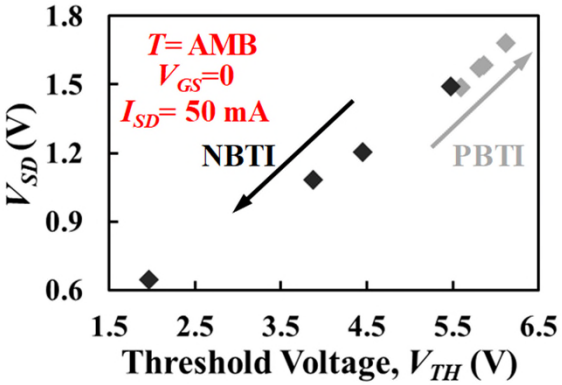
Impact of NBTI and PBTI on 3RD Quadrant characteristics in SiC MOSFETs

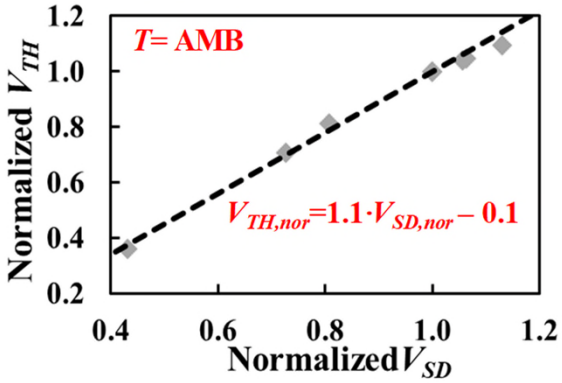
J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

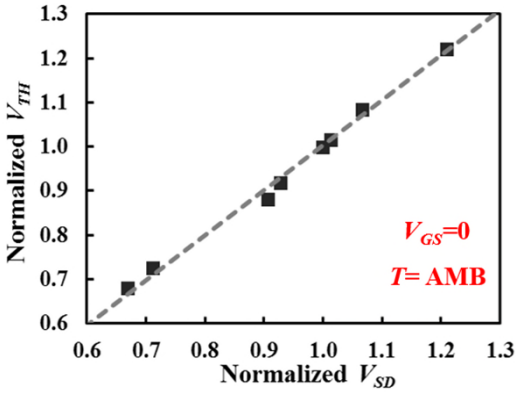
J. Lutz et al., *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 2nd ed.: Springer-Verlag Berlin Heidelberg, 2018

CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT

- Novel methodology for BTI characterization
  - Using the body diode voltage when V_{GS}=0
  - Similar to the use of V_{SD} as temperature sensor, but for detecting oxide degradation/V_{TH} shifts.
  - Calibration required. Using accelerated stress tests.





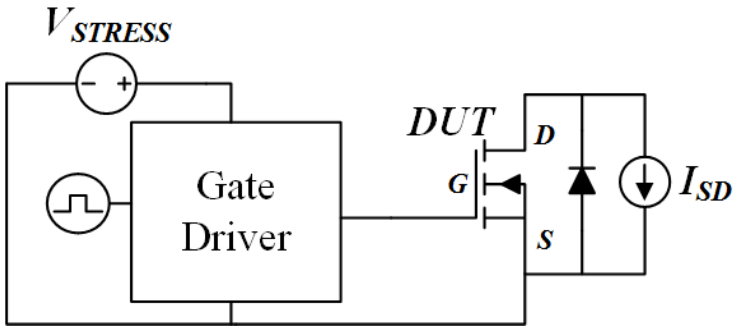


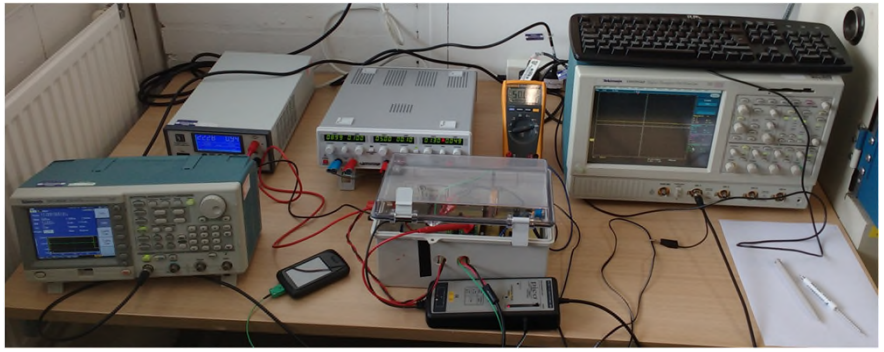
J. O. Gonzalez, O. Alatise and P. Mawby, "Non-Intrusive Methodologies for Characterization of Bias Temperature Instability in SiC Power MOSFETs," IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2020, pp. 1-10

J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT

- Circuit
  - Gate driver is used to apply stress voltage to the gate
  - Constant current source: low sensing current I_{SD} flowing in the source-drain direction

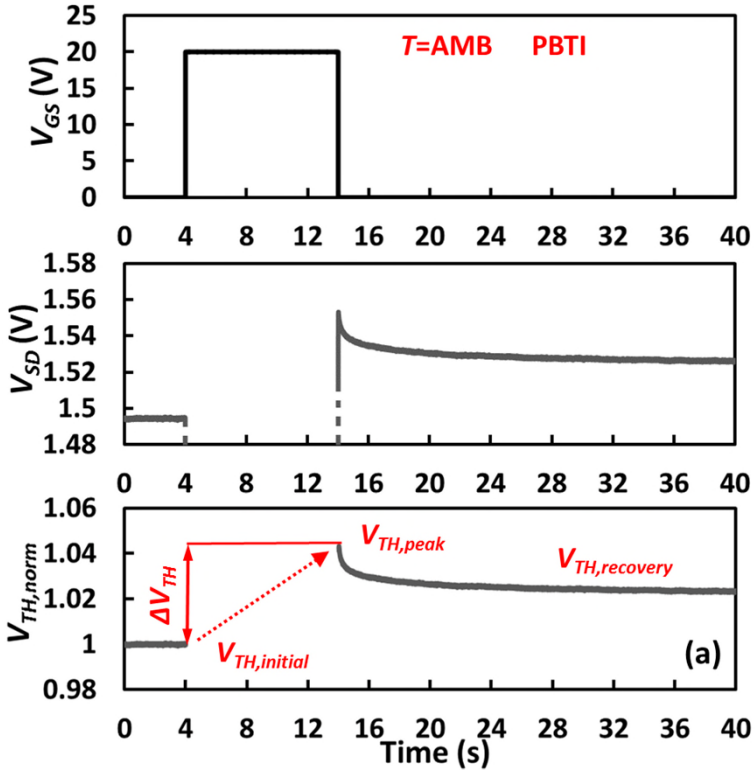




Experimental set-up for characterising BTI using 3rd quadrant characteristics

J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT

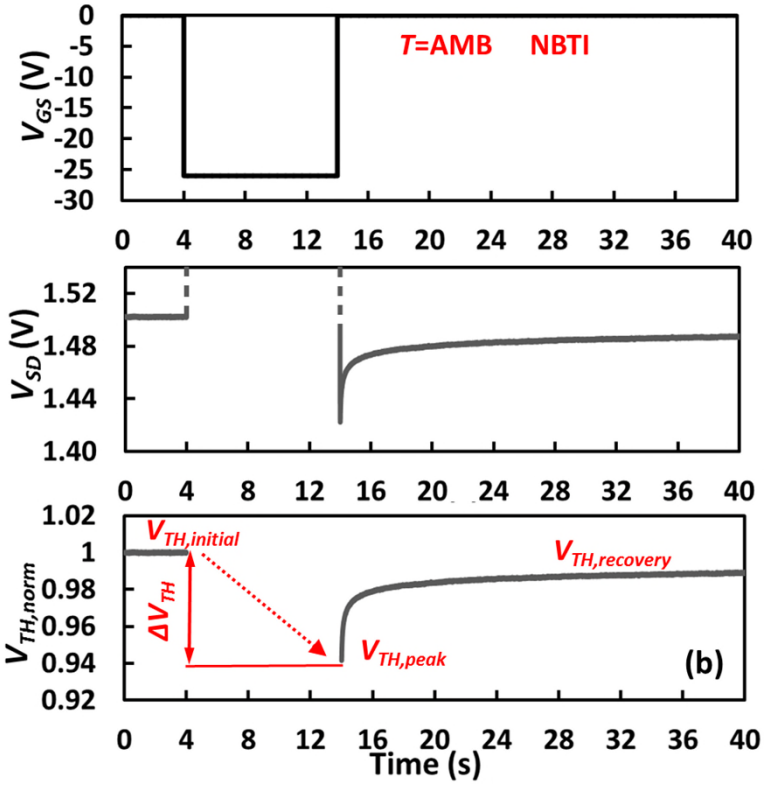


V_{GS}, V_{SD} and V_{TH} during stress and recovery for PBTI

- PBTI evaluation
  - Pre-stress phase (V_{GS}=0 V): The current flows through the body diode and channel. I_{SD}= 50 mA , $V_{TH,initial}$
  - Stress phase (V_{GS}=20 V): The current flows through channel. Device is ON.
  - Recovery phase (V_{GS}=0 V): The current flows through the body diode and channel. $V_{TH,peak}$ and $V_{TH,recovery}$

J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018.

CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT



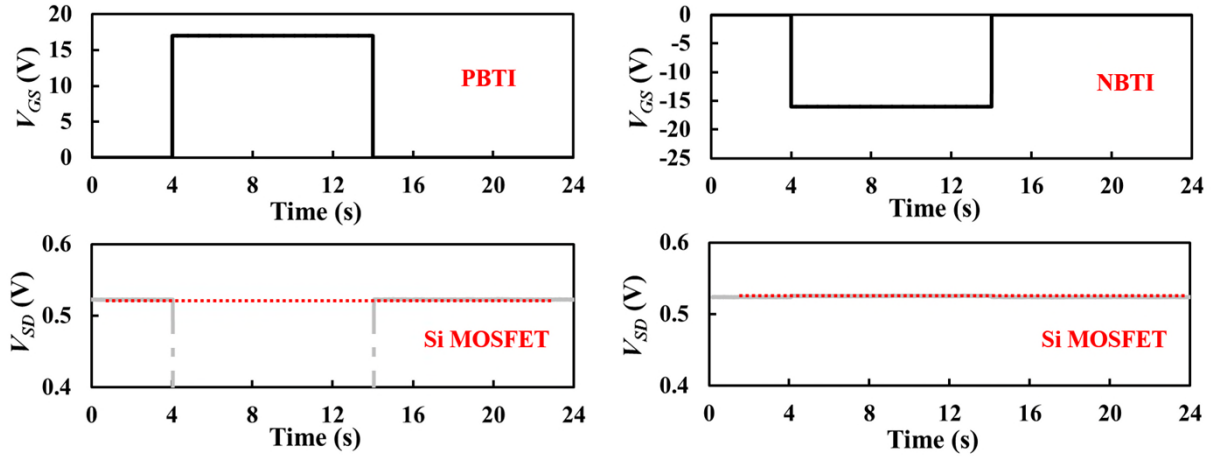
V_{GS}, V_{SD} and V_{TH} during stress and recovery for NBTI

- NBTI evaluation
  - Pre-stress phase (V_{GS}=0 V): The current flows through the body diode and channel. I_{SD}= 50 mA , $V_{TH,initial}$
  - Stress phase (V_{GS}=-26 V): The current flows through body diode only. SiC PN junction voltage
  - Recovery phase (V_{GS}=0 V): The current flows through the body diode and channel. $V_{TH,peak}$ and $V_{TH,recovery}$

J. Ortiz Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability,* vol. 88-90, pp. 557-562, 2018.

CHARACTERIZATION TECHNIQUES FOR BTI USING 3RD QUADRANT

- Silicon MOSFET
  - This is not observed for both positive and negative gate stresses



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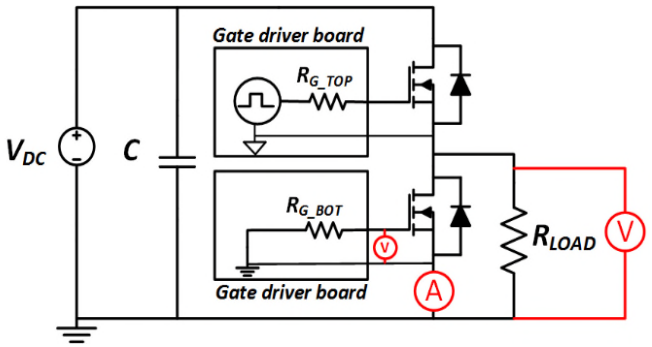
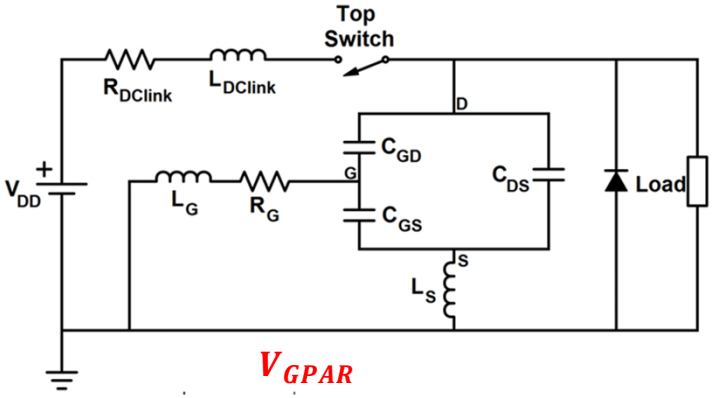
CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK



Test rig for using crosstalk



- As the top side device is switched ON, the supply voltage falls across the bottom side device with a dV/dt determined by the R_{GTOP}.
- This coupled with the MOSFET C_{GD} causes a parasitic gate voltage on the bottom side device
- The Miller Feedback current is

$$C_{GD}\frac{dV_{DS}}{dt}$$

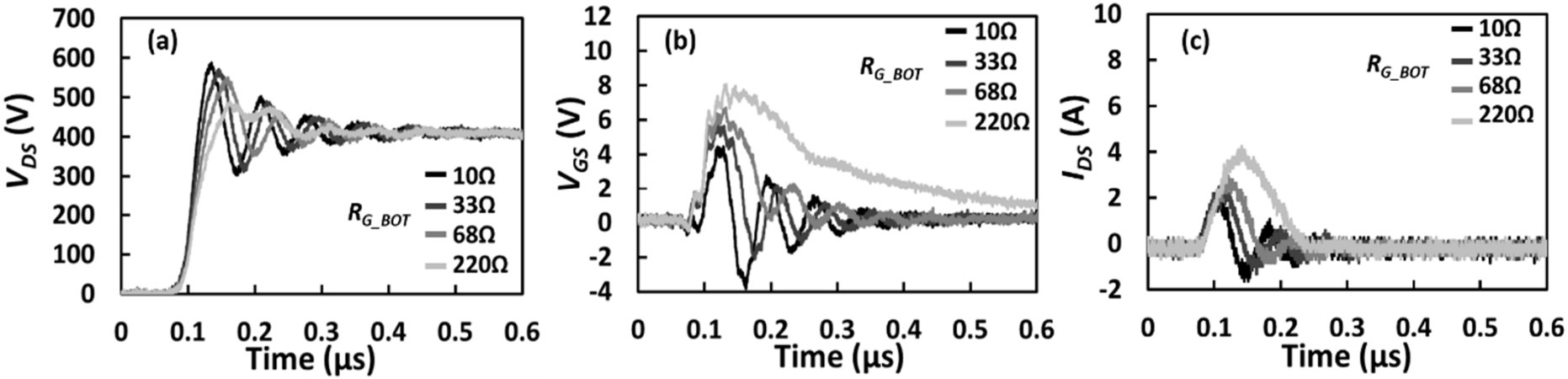
- The parasitic gate voltage is given by

$$V_{GPAR} = R_{G\_BOT}C_{GD}\frac{dV_{DS}}{dt}\left(1 - e^{-\frac{t}{R_{G\_BOT}(C_{GS}+C_{GD})}}\right)$$

CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

- Shoot-through current is usually a problem, however in the case, the V_{TH} sensitivity of Ishoot is used to track V_{TH}.

- To increase the shoot-through current
  - Large bottoms side R_G.
  - Small top side R_G.



SiC planar MOSFET (a) V_{DS} of bottom side device during cross-talk, (b) V_{GS} of bottom side device during cross-talk, (c) I_{shoot} of bottom side device during cross-talk

CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

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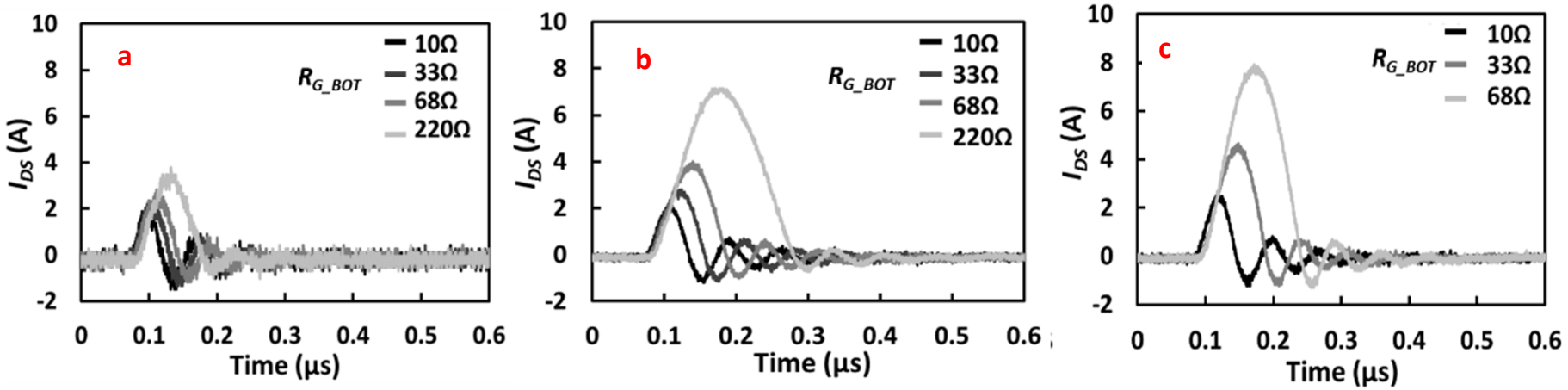
- Different SiC MOSFETs have different susceptibilities to crosstalk according to the ratio below

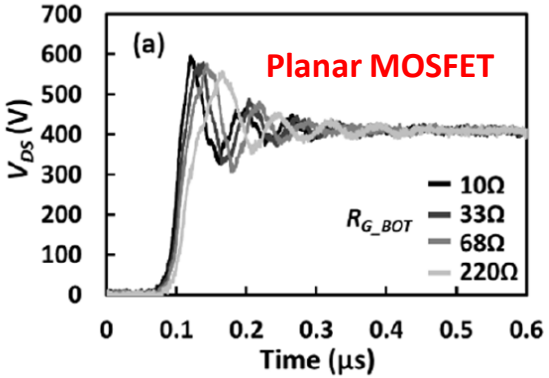
$$\frac{C_{GD}}{C_{GD} + C_{GS}}$$

- Three different MOSFET technologies have been measured for cross-talk

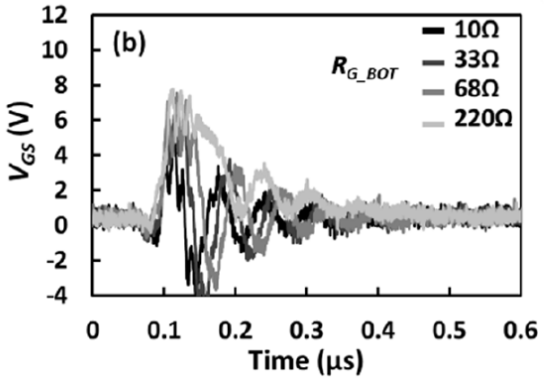


Shoot-trough currents for 3 different MOSFET technologies

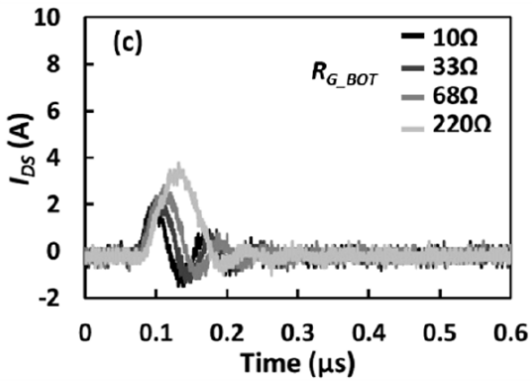
CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK



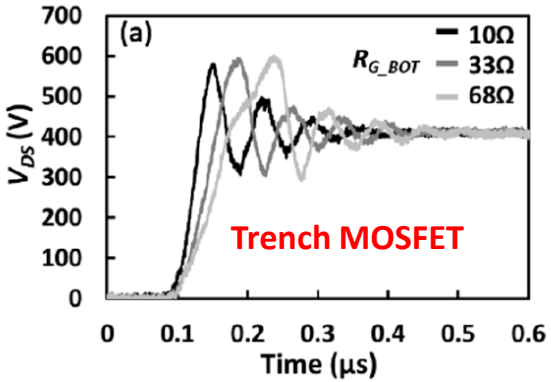
Low side V_{DS}



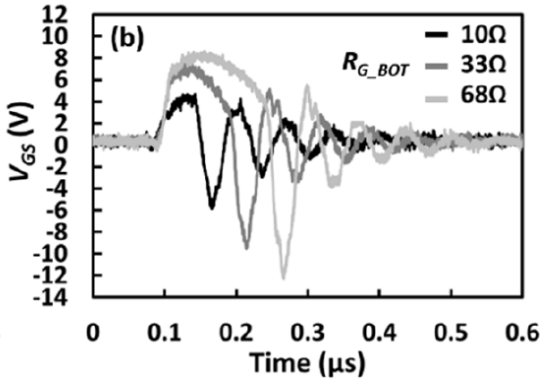
Low side V_{GS}



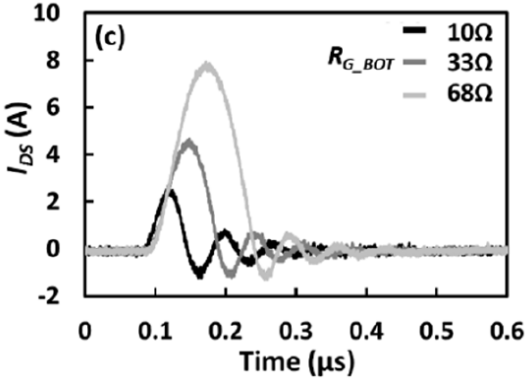
Shoot-through current



Low side V_{DS}



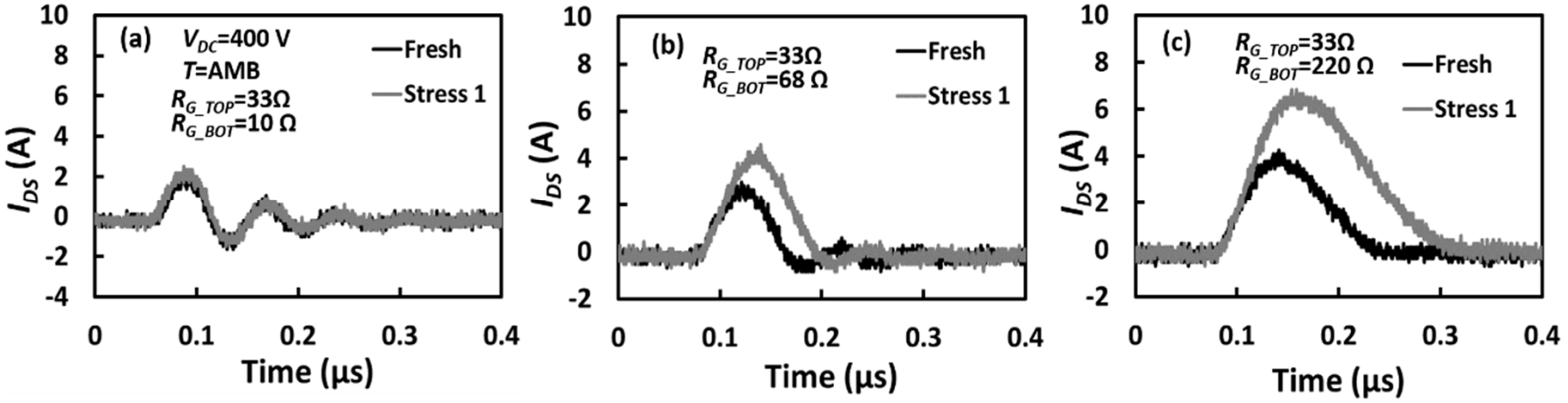
Low side V_{GS}



Shoot-through current

CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

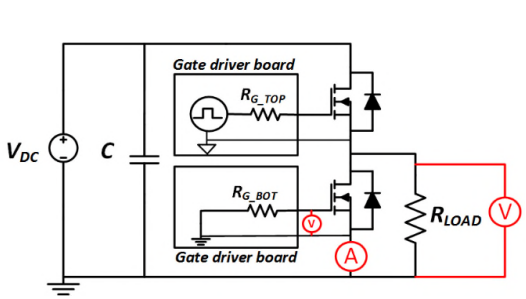
- By choosing the right combination of gate resistances to maximize the shoot-through current, V_{TH} shift can be monitored.
- The shoot-through increases with NBTI stress (due to decreasing V_{TH}) and decreases with PBTI stress (due to increasing V_{TH}).

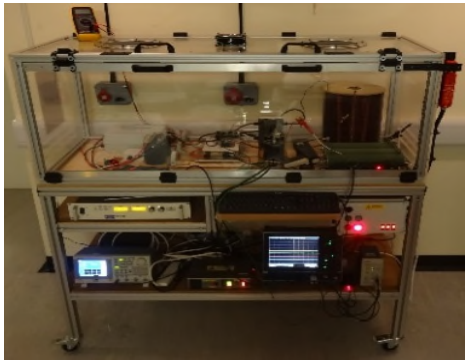


Shoot-through currents for different R_G combinations on SiC MOSFETs after NBTI stress

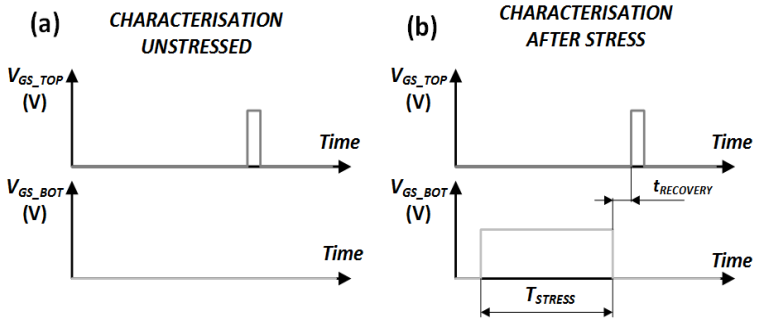
CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

- In the previous measurements, V_{TH} recovery was not taken into account.
- By tuning the stress and recovery times, it is possible characterise the BTI stress and recovery mechanisms.
- This technique is an improvement from traditional techniques that simply rely to extracting the static measurements.





Circuit and Picture Test rig for using crosstalk



Stress and characterisation sequence

CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

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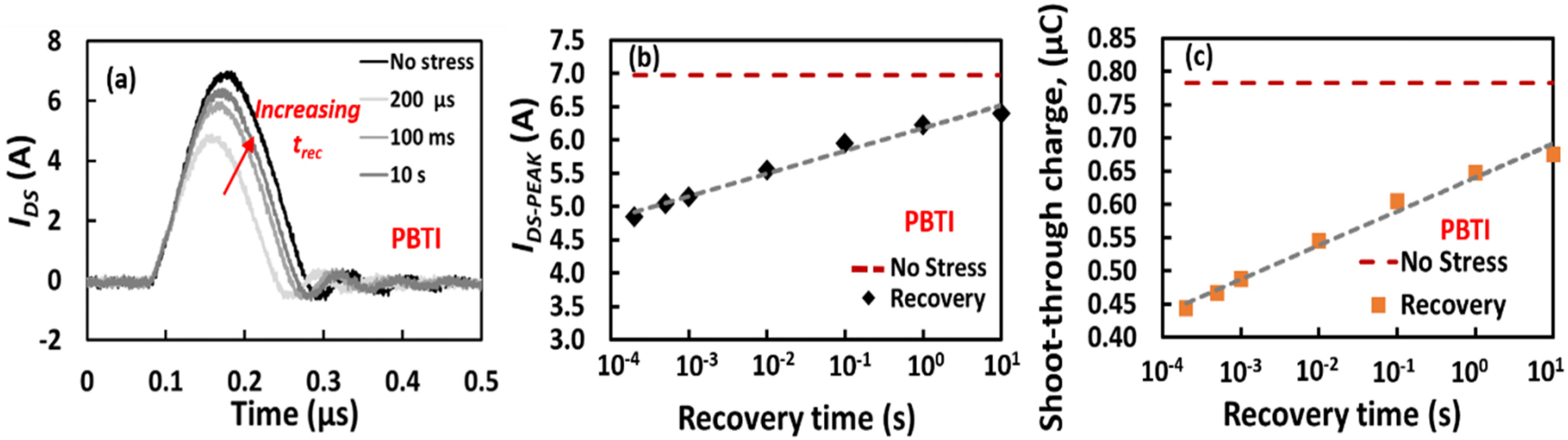
- The measurements below show the V_{TH} rise with a corresponding reduction in shoot-through current.
- With increasing recovery time, the shoot-through increases back to the unstressed value, thereby indicating a recovery in V_{TH}.



Threshold voltage stress and recovery using the proposed technique

CHARACTERIZATION TECHNIQUES FOR BTI USING CROSSTALK

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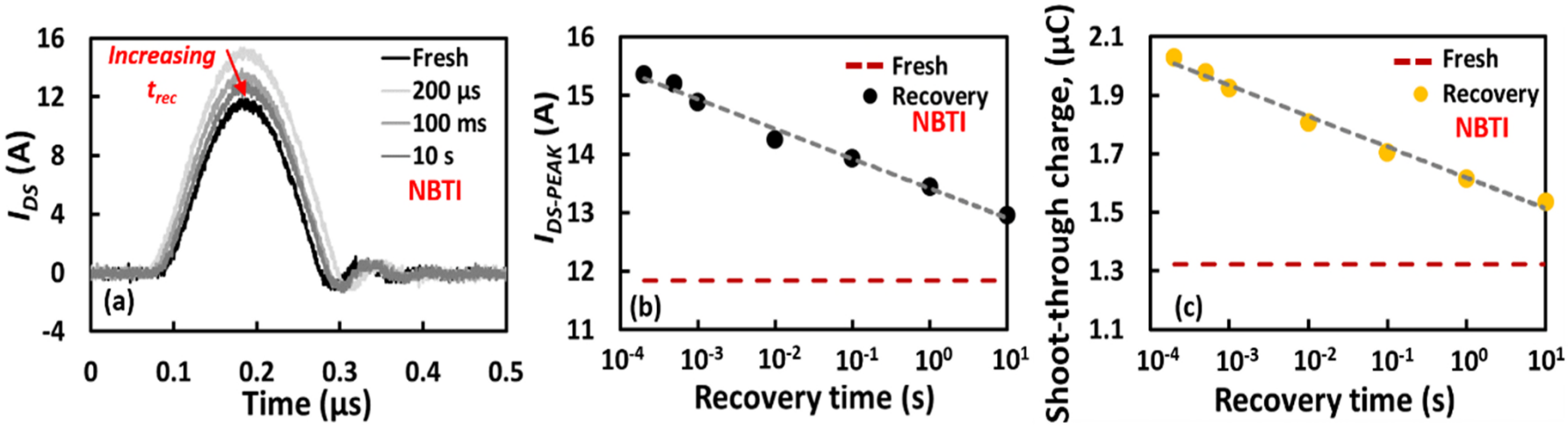
- The measurements below show the V_{TH} fall with a corresponding increase in shoot-through current.
- With increasing recovery time, the shoot-through reduces back to the unstressed value, thereby indicating a recovery in V_{TH}.



Threshold voltage stress and recovery using the proposed technique

Gate characteristics in GaN HEMTs

Dr Jose Ortiz Gonzalez

11th of January 2021

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Engineering and Physical Sciences Research Council

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- **Introduction**
- Gate Characteristics
- Third Quadrant Characteristics
- Gate Stresses and threshold voltage instability

INTRODUCTION

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- GaN devices are well recognized for their ultra-fast switching rates and good conduction losses.
- The good performance of GaN High Electron Mobility Transistors (HEMTs) is due to the two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface.
- The commercially available devices in the 650 V application range are **lateral devices** with two main gate structures for achieving **normally-OFF** operation

INTRODUCTION

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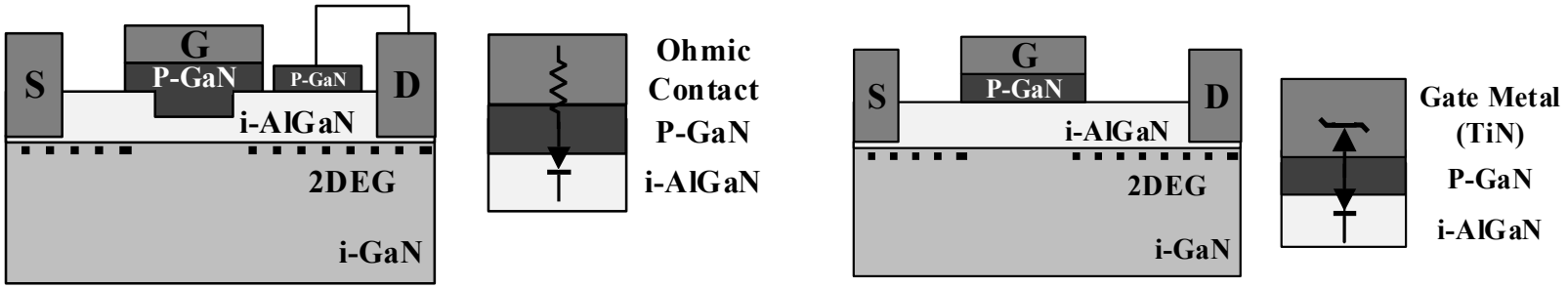
- (i) p-GaN gate on AlGaN with an Ohmic contact
- (ii) p-GaN gate on AlGaN with a Schottky contact



Ohmic contact

Schottky contact

[1] T. Detzel, "Reliability of GaN Power Devices from the Industrial Perspective - Tutorial," presented at the 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis - ESREF, September, 2018
[2] Y. Uemoto et al., "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," IEEE Trans. on Electron Devices, vol. 54, no. 12, pp. 3393-3399, 2007.
[3] A. N. Tallarico et al., "Investigation of the p-GaN Gate Breakdown in Forward-Biased GaN-Based Power HEMTs," IEEE Electron Device Letters, vol. 38, no. 1, pp. 99-102, 2017.

INTRODUCTION

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- Commercially available GaN HEMTs have been the subject of different studies, including electrothermal characterization and reliability.
  - JEDEC committee (JC-70) focused on the development of standards for GaN power devices
- Relevant studies for GaN power devices include:
  - Dynamic ON-state resistance
  - Threshold voltage instability
  - Power Cycling
- Previous studies highlight the **complexity** of the gate stack structure
  - Different threshold voltage shifts depending on the magnitude of the gate stress voltage have been reported

INTRODUCTION

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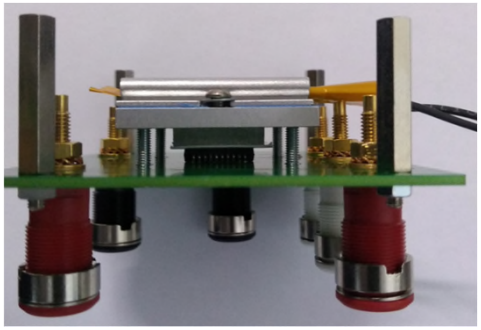
- Two commercially available normally-OFF GaN HEMTs have been studied
  - Similar voltage and current ratings



Prototype PCBs for testing
DC heater for adjusting the case temperature

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- Introduction
- **Gate Characteristics**
- Third Quadrant Characteristics
- Gate Stresses and threshold voltage instability

GATE CHARACTERISTICS

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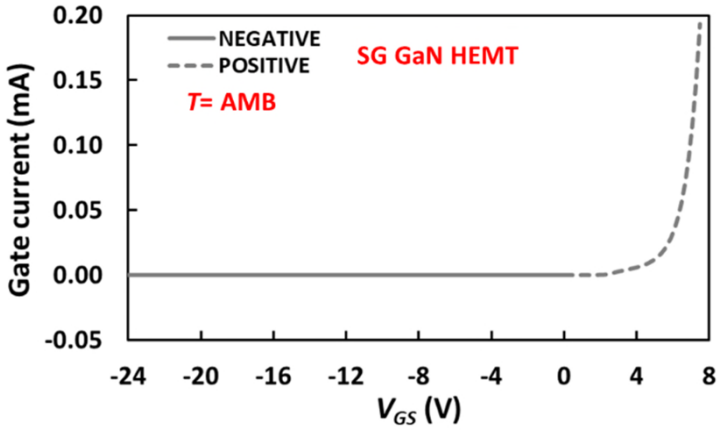
- Different gate structures mean different gate driving requirements.
- Gate reliability is key
  - Gate voltage limits
  - Gate leakage current
  - Role of temperature
- Studies are required: Our contribution

J. O. Gonzalez, B. Etoz and O. Alatise, "Characterizing Threshold Voltage Shifts and Recovery in Schottky Gate and Ohmic Gate GaN HEMTs," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 217-224,

J. O. Gonzalez, B. Etoz and O. Alatise, "Gate stresses and threshold voltage instability in normally-OFF GaN HEMTs," 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 2020, pp. P.1-P.10,

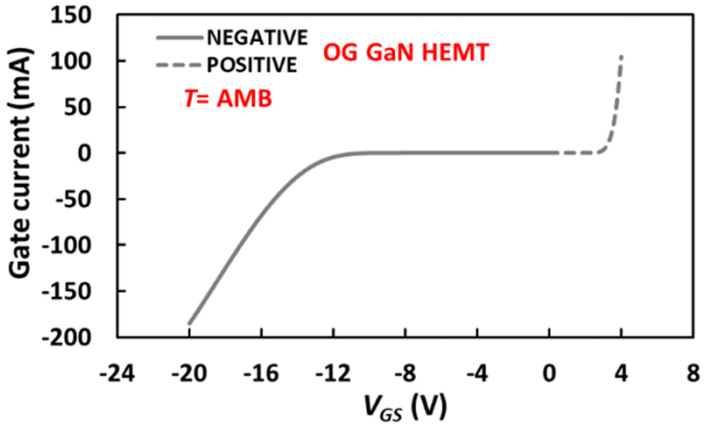
GATE CHARACTERISTICS

- Gate voltage and leakage current (gate voltage sweep)



Schottky Gate (SG):

- Low gate leakage currents
- "Asymmetric" performance



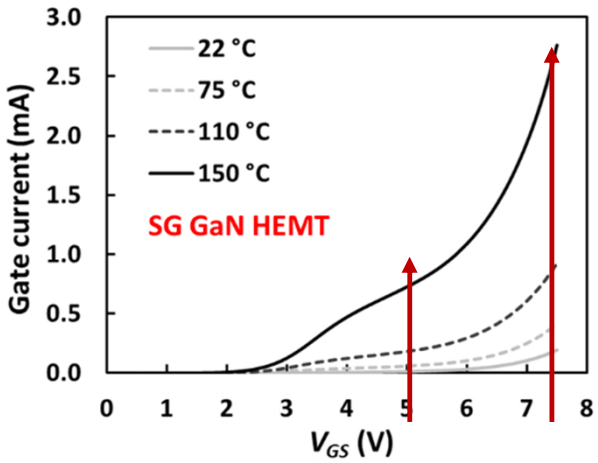
Ohmic Gate (OG):

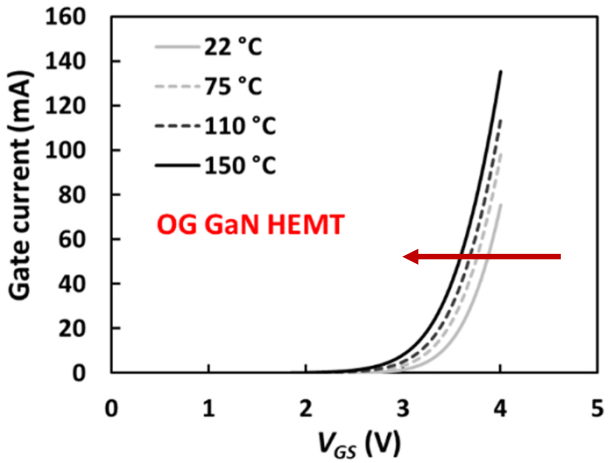
- High gate leakage currents
- Internal protection diode structure (Negative gate bias)

- **Important for driving the devices**

GATE CHARACTERISTICS

- Impact of temperature (Positive gate bias)

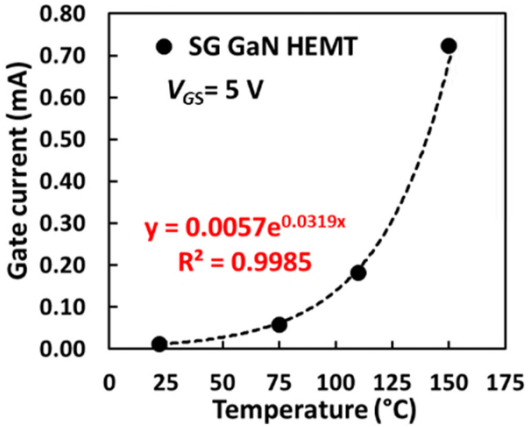




- **Important for driving the devices**

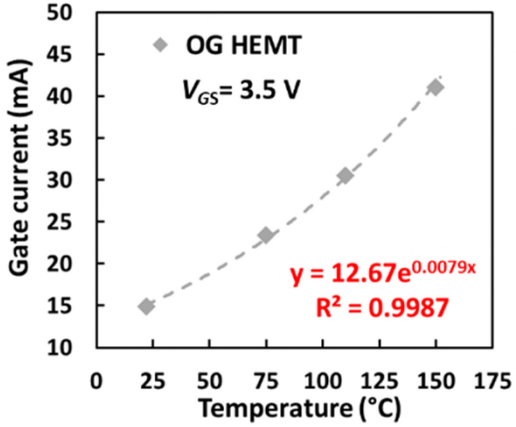
GATE CHARACTERISTICS

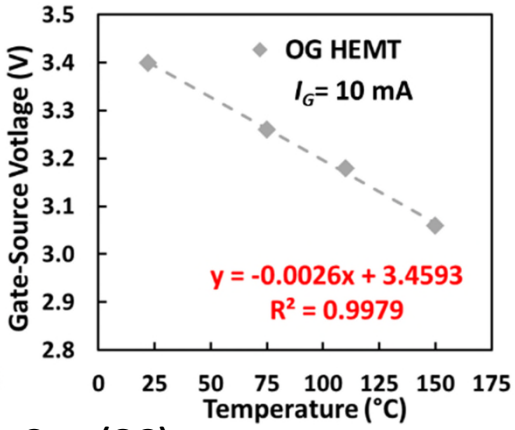
- Use of the gate characteristics as Temperature Sensitive Electrical Parameter (TSEP)



Schottky Gate (SG):

- Leakage current is very sensitive
  - 60x





Ohmic Gate (OG):

- Higher leakage currents
  - 2.7x
- Forward voltage at constant current is a good TSEP

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- Gate Stresses and threshold voltage instability

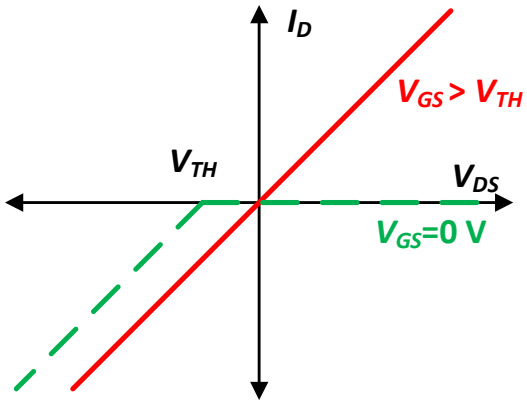
THIRD QUADRANT CHARACTERISTICS

- GaN HEMTs do not have a parasitic body diode
- Reverse conduction. What is the mechanism?

- GaN HEMT: Symmetric device
- Reverse Conduction Mechanism:
  - Self-commutated reverse conduction (SCRC)

$$V_{SD} = V_{GD\text{-}TH} - V_{GS} + I \cdot R_{SD}$$

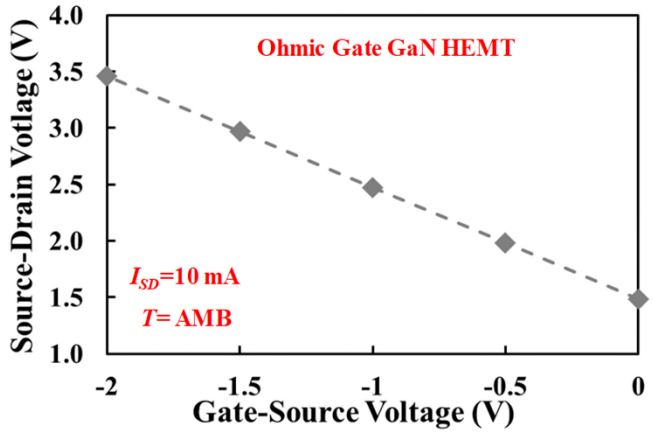
$$V_{GD\text{-}TH} \sim V_{GS\text{-}TH}$$



Adapted from: E. A. Jones et al. "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 3, pp. 707-719, 2016.

THIRD QUADRANT CHARACTERISTICS

- Negative gate voltage
  - Gate-Source voltage V_{GS} adds to Source-Drain Voltage V_{SD}



- Gate and source shorted (V_{GS}=0)
- Low current I

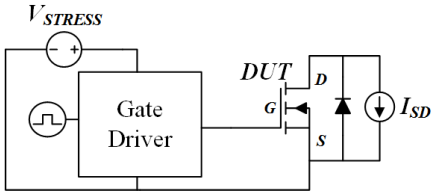
$$V_{SD} = V_{TH} - V_{GS} + I \cdot R_{SD}$$

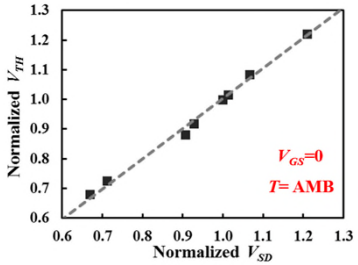
$$V_{SD} \sim V_{TH}$$

- Third Quadrant Voltage (V_{SD}) at low current and V_{GS}=0 can be used as an indicator for V_{TH} tracking

THIRD QUADRANT CHARACTERISTICS

- Method for characterizing V_{TH} shifts in SiC MOSFETs using the body diode.
  - Similar to the use of V_{SD} as temperature sensor
  - It requires a calibrated relationship between V_{SD} and V_{TH}
- GaN HEMTs
  - **There is direct a relationship between V_{SD} and V_{TH}**





J. A. O. González and O. Alatise, "A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5737-5747, June 2019,

	V_{TH} (V) V_{GS}=V_{DS} @ I= 10 mA	V_{SD} (V), V_{GS}=0, @ I = 10 mA
Ohmic Gate GaN HEMT	**1.478**	**1.483**
Schottky Gate GaN HEMT	**1.597**	**1.576**

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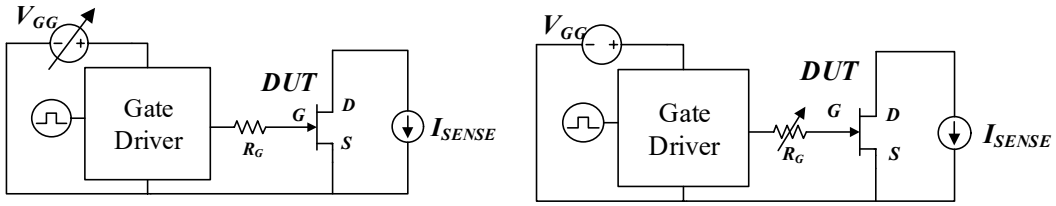
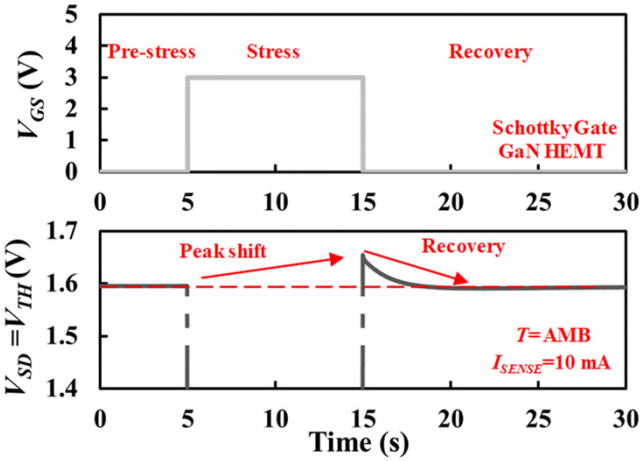
- Gate Characteristics
- Third Quadrant Characteristics
- **Gate Stresses and threshold voltage instability**

GATE STRESSES AND THRESHOLD VOLTAGE INSTABILITY

- We evaluated the third quadrant methodology in GaN devices for characterizing V_{TH} drift after gate stress
  - Gate voltage stress for the Schottky gate HEMT
  - Gate current stress for the Ohmic gate HEMT



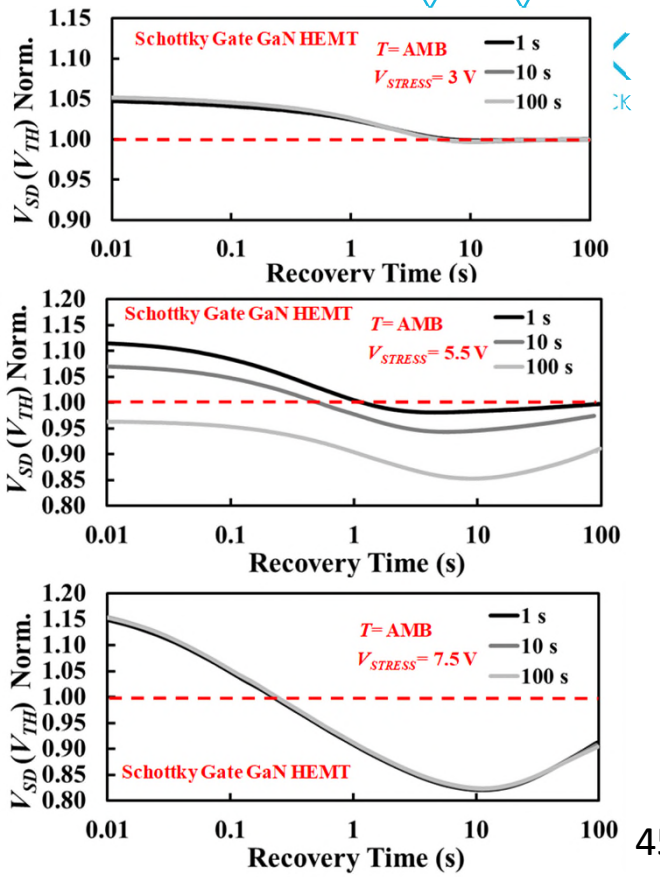
- Different stress parameters can be evaluated:
  - Stress time
  - Gate stress voltage/current
  - Temperature



Example for a 3 V/10 s stress pulse

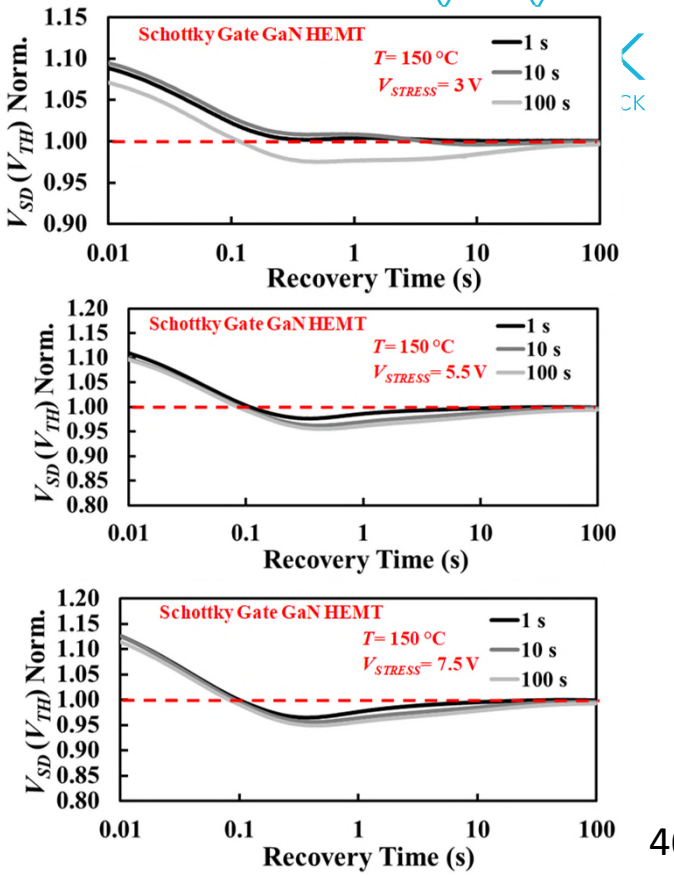
GATE STRESSES AND THRESHOLD VOLTAGE INSTABILITY

- Schottky Gate HEMT
- Single Pulse stress – Ambient temperature
  - V_{TH} shift dependent on gate stress level
  - The different shifts attributed to three different mechanisms: electron trapping at the AlGaN/GaN interface, hole trapping in the AlGaN barrier and hole depletion
  - The different time constants of the traps can be captured using this method
  - Stress duration (1 s to 100 s) has no apparent or very minor effect at 3 V and 7.5 V stresses
  - Affects peak shift when stress is 5.5 V



GATE STRESSES AND THRESHOLD VOLTAGE INSTABILITY

- Schottky Gate HEMT
- Single Pulse stress - 150 °C
  - Compared with ambient temperature, the gate stress level has a minor role on the V_{TH} shift
  - Minor impact of stress time on the V_{TH} shift. More apparent at 3 V gate stress.
  - Recovery is accelerated with temperature (range of minutes at ambient temperature)



GATE STRESSES AND THRESHOLD VOLTAGE INSTABILITY

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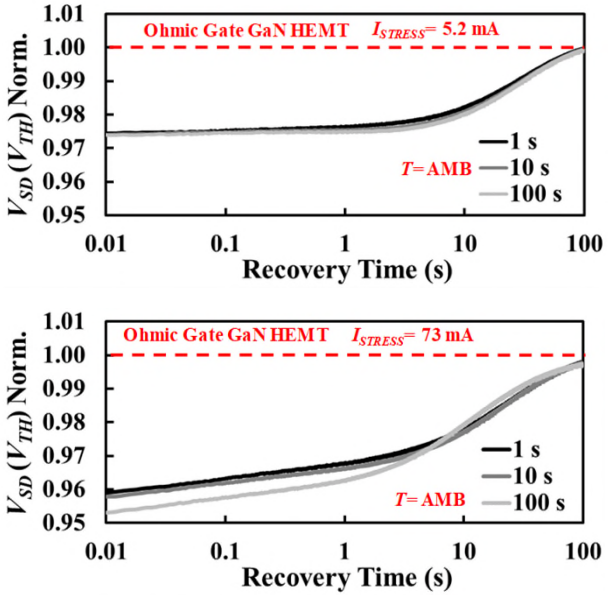
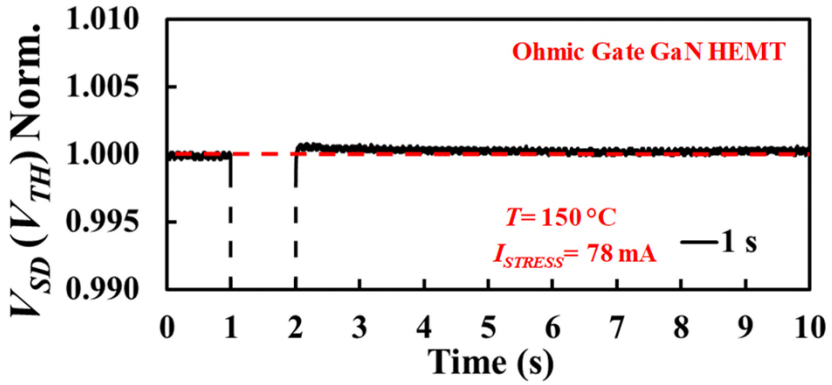
- Ohmic Gate HEMT
- Single Pulse stress – Ambient temperature
  - Stress in current level: 5.2 mA and 73 mA (Gate voltages of 3.2 and 4 V respectively)
  - Negative V_{TH} shift in both cases. Recovery time in the range of seconds
  - V_{TH} shift increases with stress magnitude (-2.5% at low current and -4% at high current)
  - Stress time, minor impact at high current stress.



GATE STRESSES AND THRESHOLD VOLTAGE INSTABILITY

- Ohmic Gate HEMT
- Single Pulse stress - 150 °C
  - No apparent shift at high temperature stress. Stress current increases (constant voltage gate driver)



SUMMARY

- Gate characteristics in WBG devices remain a relevant and important reliability topic
- Different techniques are required for assessing gate characteristics in WBG devices
- We have introduced 2 novel techniques based on 3rd quadrant characteristics and cross-talk
- This is especially important when considering TSEPs for condition monitoring of WBG devices

ACKNOWLEDGEMENTS

- This work was supported by the UK Engineering and Physical Sciences Research Council (EPSRC) through the grant reference EP/R004366/1
- We would like to thank iMAPS UK for the opportunity to disseminate our research

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