IMAPS-UK
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Online Event

Research Showcase
Recent Advances on Reliability and Gate Driving of WBG Power Electronics

Testing Silicon Carbide Power MOSFETs under Normal and Abnormal Operations

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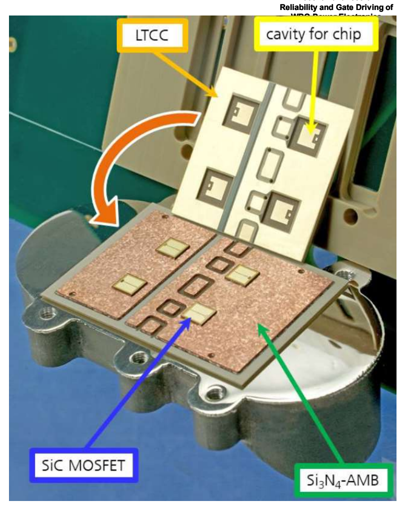
Outline

Research Showcase
Recent Advances on Reliability and Gate Driving of

Testing Silicon Carbide Power MOSFETs under Normal and Abnormal Operations

- ▶ Introduction
- ▶ Power-cycling testing of SiC MOSFETs
- ▶ Mission-profile-based reliability prediction
- ▶ Short-circuit testing of SiC MOSFETs
- ▶ Discussion
- ▶ Conclusion



Picture source: Kirill Klein, Olaf Rämer, Eckart Hoene, Yusuke Yasuda; Hiroyuki Ito, Fumi Kurita, Masato Enoki, Hideyuki Nakamura, Kenji Okishiro, "Low inductive full ceramic SiC power module for high-temperature automotive applications", PCIM 2019

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Introduction

- Why testing for reliability?

Silicon Carbide (SiC)

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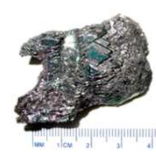
An old-new material

- Historically known for its mechanical properties (second hardest material after diamond)
- Outstanding properties as a semiconductor
- PE market is growing fast (40% forecast compound annual growth rate)



Source: Wikipedia

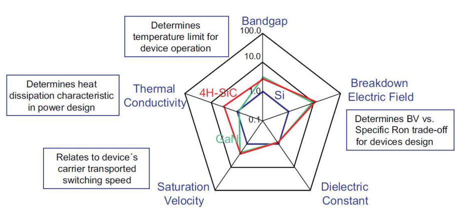
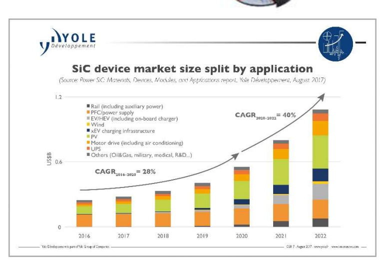


Figure 2.1.4 Impact of different physical parameters of semiconductor materials [3]



Sources: U. Nicolai, W. Tursky, T. Reimann, A. Wintrich, "Application Manual Power Semiconductors", Semikron, 2010
Majumdar, G.; Oomori, T.: "Some key researches on SiC device technologies and their predicted advantages", EPE 2009
H. Lin, A Villamor, "Power SiC 2018: Materials, Devices and Applications", Yole/Systemplus

Silicon Carbide MOSFETs

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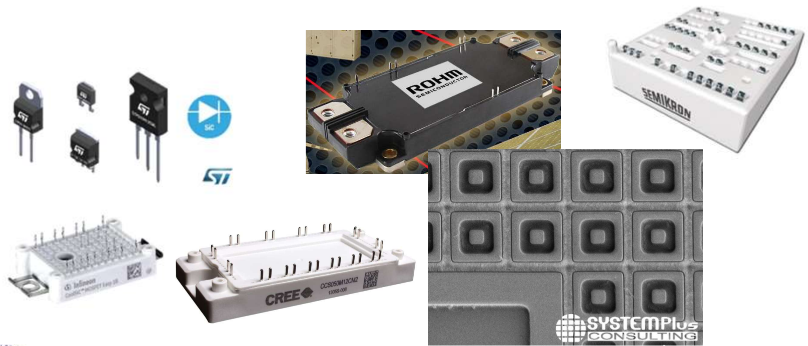
Scenario

- ▶ Many players in the field
- ▶ Both discrete and modules are available
- ▶ Technology is going fast: trench gate (3G) available since 2017
- ▶ In 2Q-2019 CREE has invested 1B$ in new SiC fab



Source: Systemplus (analysis on Rohm gen3 SiC MOSFETs)

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Driving applications

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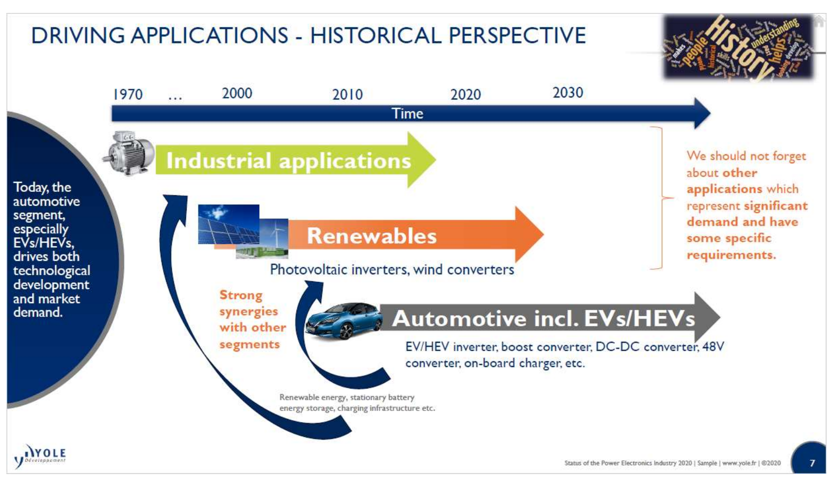
Automotive segment is expected to drive the next decade development in Power Electronics



Source: Status of the Power Electronics Industry 2020, Yole Développement

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Power-cycling testing of SiC MOSFETs

- Testing methods
- results

A look inside power devices

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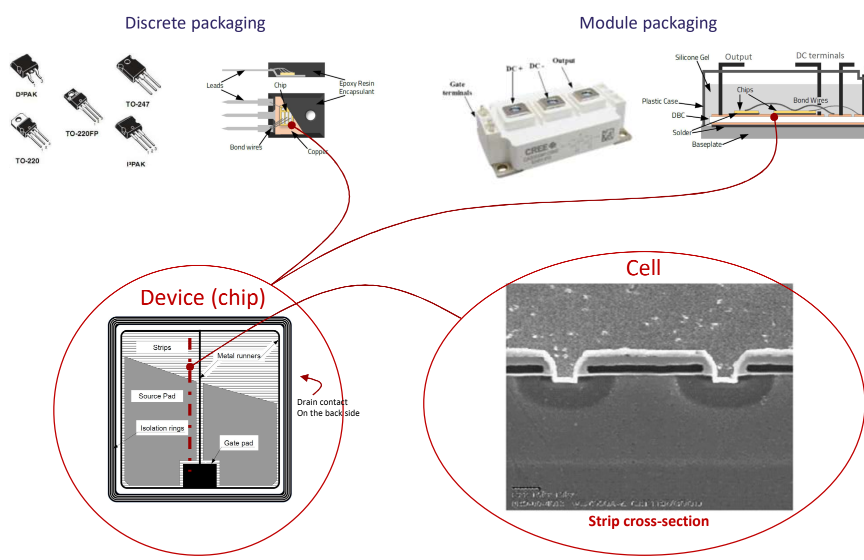
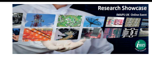


Packaging Wear Out Mechanisms



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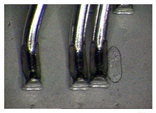
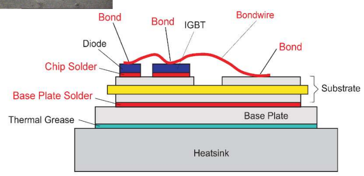
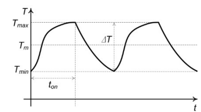
Bond wires

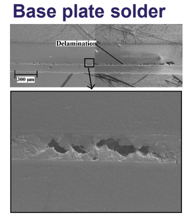


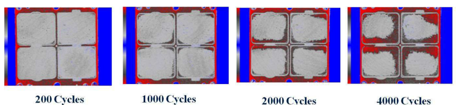




Cyclic temperature stress

Base plate solder





Chip solder

Thermal grease degradation

Sources

A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application manual power semiconductors*, SEMIKRON International, 2011, ISBN: 978-3- 938-84366-6.

T. Lhommeau, C. Martin, M. Karama, R. Meuret and M. Mermet-Guyennet, "Base-plate solder reliability study of IGBT modules for aeronautical application," Power Electronics and Applications, 2007 European Conference on, Aalborg, 2007, pp. 1-10.

M. Schulz, "Thermal management details and their influence on the aging of power semiconductors," *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, Lappeenranta, 2014, pp. 1-6.

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Accelerated Life Testing (ALT)

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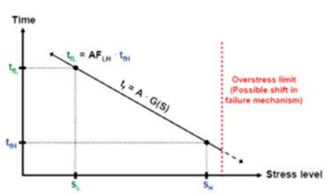
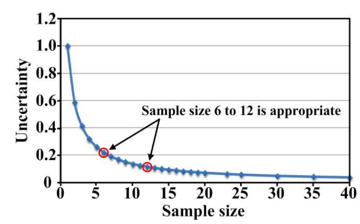
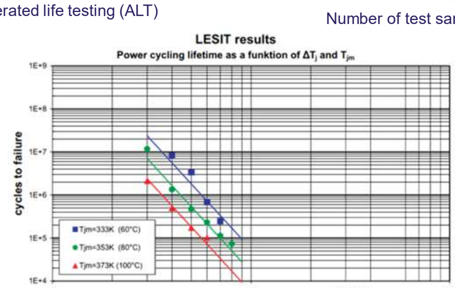


Principle of accelerated life testing (ALT)



Number of test sample per condition



Sources

SPM-179 "Acceleration factors and accelerated life testing"

LESIT project

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Transitioning to SiC-based Power Electronics

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Chip area is limited by cost

- ▶ Raw material is still dominating the cost breakdown

Packaging-related issues

- ▶ Smaller per-Ampere area with respect to Silicon counterparts
- ▶ Lesser area for bond-wire footprints → higher bond-wire current density
- ▶ Higher power density → higher junction temperature swing

36 A chip from ROHM BSM180D12P3C007 SiC MOSFET module (3.0mm x 4.3mm)

Semiconductor-related issues

- ▶ Larger bandgap → higher electric field → higher probability of instabilities taking place in the oxide region

Sources: " 6" and Below: Small Dimension Wafer Market Trends 2020", Yole Développement, 2020
Silicon carbide semiconductors in the Bosch wafer fab in Reutlingen, Bosch-Presse, 2019

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Degradation Mechanisms of SiC MOSFETs

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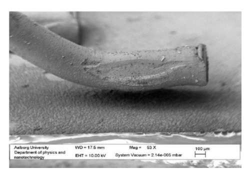
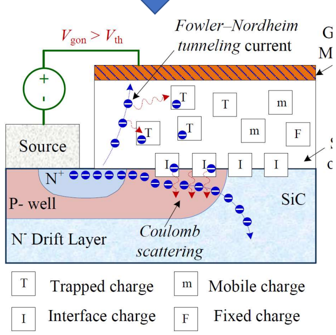
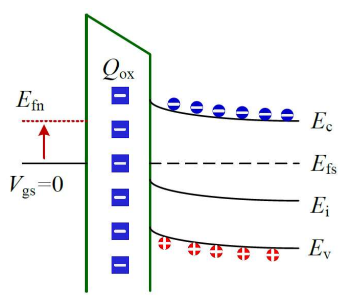
Two main levels of degradation

- ▶ Packaging degradation (bonding wires)
- ▶ Semiconductor degradation (Vth)





Fohler-Nordheim tunneling mechanism



Effect of trapped charges

Source: H. Luo, F. Iannuzzo, et al. "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules", JESTPE 2019

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Degradation of SiC MOSFETs - Testing

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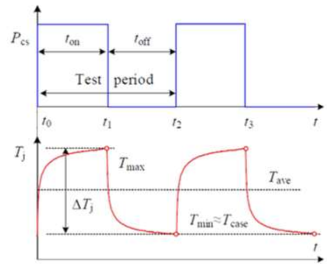
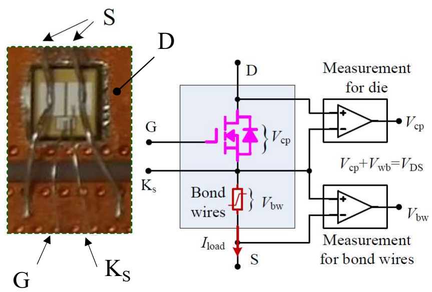
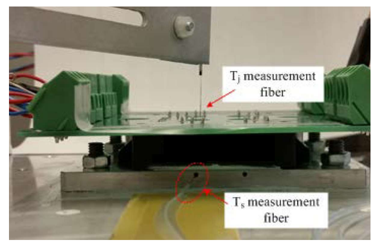
- ▶ Standard DC power cycling
- ▶ Separated voltage monitoring for die and bond wire
- ▶ Junction temperature monitored under test







Sources: H. Luo, F. Iannuzzo, et al. "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules", JESTPE 2019
H. Luo, F. Iannuzzo, et al., "Study of Current Density Influence on Bond Wire Degradation Rate in SiC MOSFET Modules," JESTPE 2019

Effect of current density on bond wires

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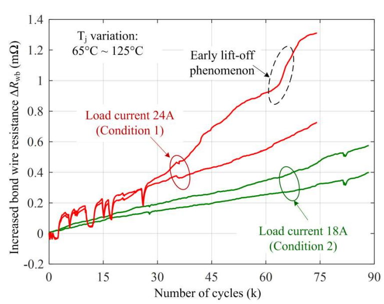
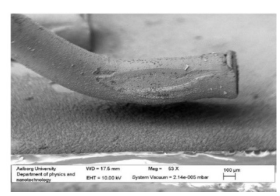
Bond-wire resistance increases during tests

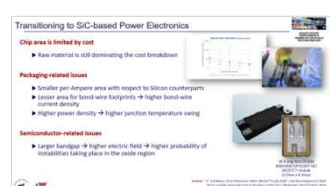
- ▶ Current density plays a major role in wear phenomena

Parameters	Condition 1	Condition 2
Maximum T_j	125 °C	125 °C
Minimum T_j	65 °C	65 °C
Delta T_j	60 °C	60 °C
Period/duration	2s / 4s	2s / 4s
Base plate temperature	≈ 45 °C	≈ 55 °C
Drain current I_{DS}	24 A	18 A



Bond wire resistances measurements





Source: Haoze Luo, Aalborg University, IECON 2017

Vth Shift in SiC MOSFETs

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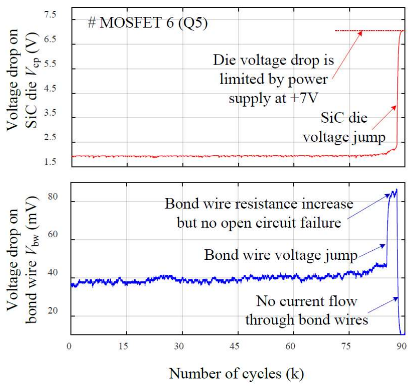
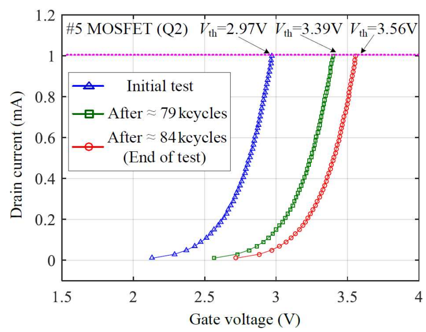
Dominated by Temperature

Parameters	Value	Parameters	Value
Initial maximum T_j	175 °C	Base plate temperature	105 °C
Initial minimum T_j	115 °C	Constant load current	21.5 A
Delta temperature	60 °C	t_{on} / t_{off}	2s / 2s





Source: H. Luo, F. Iannuzzo, and M. Turnaturi, "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules," IEEE J. Emerg. Sel. Top. Power Electron., vol. 8, no. 2, pp. 1657–1667, Jun. 2020

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Mission-profile-based reliability prediction

Reliability Prediction of Bond Wires in Real Mission Profiles

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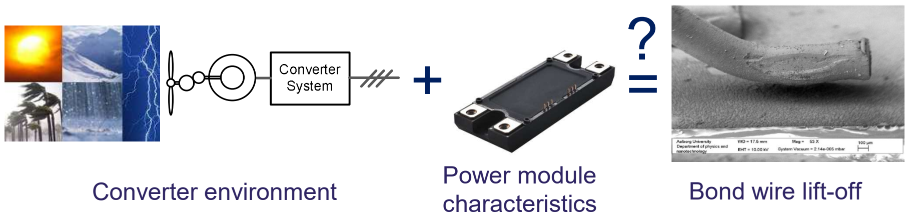
Background and motivation



Case study: Wind

- Wind speed (load) and ambient temperature (environment): mission profiles in wind turbines
- Combining such different time scales can be puzzling

A systematic approach is needed to confidently estimate thermal stress in bond-wires based on real mission profiles

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Proposed Analysis Method

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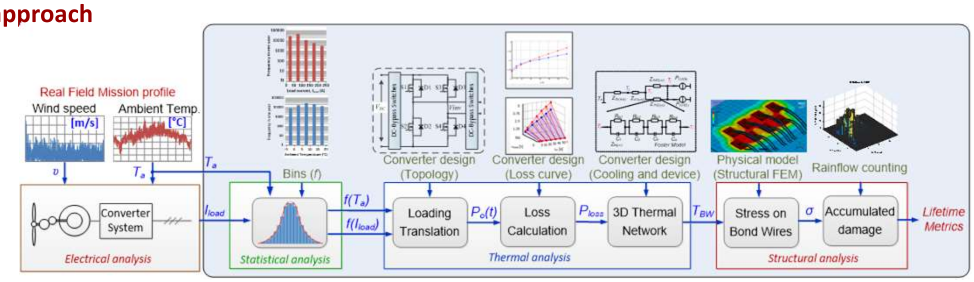
Discrete approach



- ▶ The real-field mission profile (wind speed and ambient temperature) is discretized in time and values and statistically analysed in a 2D space (Tamb, Iload)
- ▶ An accurate electro-thermal model is used to predict junction temperature at every condition (statistical bin)
- ▶ A thermo-mechanical FEM stress analysis is performed for every bin
- ▶ Rainflow analysis is performed to predict the accumulated damage function

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Mission Profile Model

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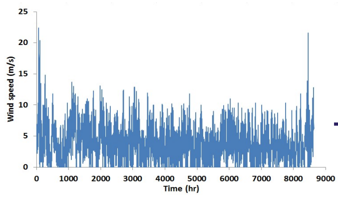
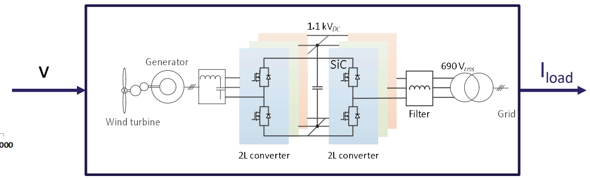


1-year mission profile



Rated output active power P_o	500 kW
Output power factor PF	1.0
DC bus voltage V_{dc}	1100 VDC
*Rated primary side voltage V_p	690 V rms
Rated load current I_{load}	209 A rms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	1.9 mH

Statistical Model

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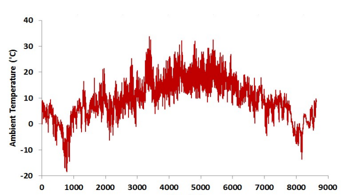
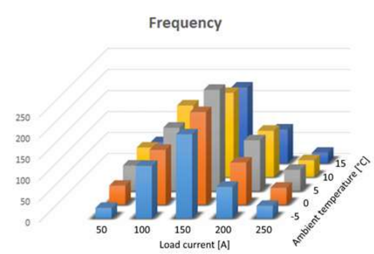
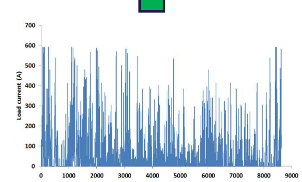


1-year ambient temperature profile



- ▶ The converter load current profile is extracted from the electrical model
- ▶ A two-dimensional distribution based on ambient temperature and load current is generated
- ▶ Generation of a compact spectrum of operating conditions (totally 5x5 bins)



1-year load current profile

Electro-Thermal Model

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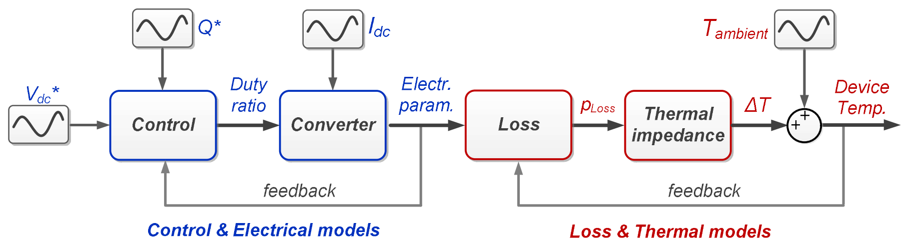
Electrical model



Flowchart of the thermal information of device

- Device temperature is calculated using the power losses and thermal impedance
- Power losses are identified experimentally and look-up tables are generated
- Look up tables are used to acquire losses in the electro-thermal model

Electro-Thermal Model

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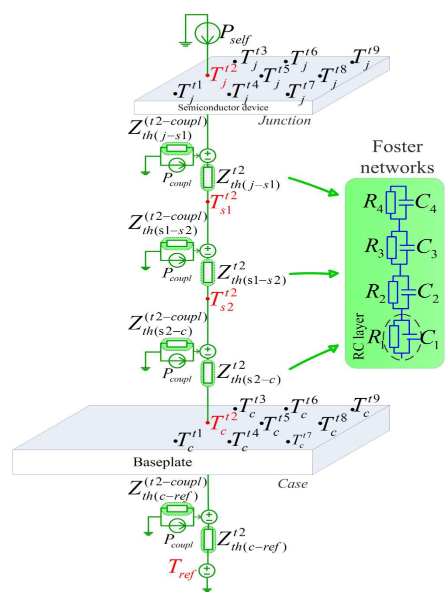
3D thermal impedance model

- A lumped thermal model based on the physical behavior of the device in different environmental and loading conditions
- Extracted from FEM
- Several Foster networks in series between layers to increase accuracy
- Accurate: RC elements variable with temperature
- Detailed temperature monitoring points in several critical locations



Thermo-Mechanical Model

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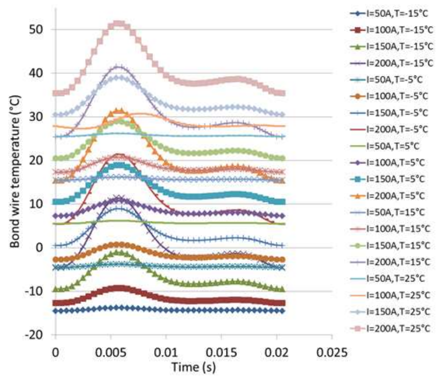
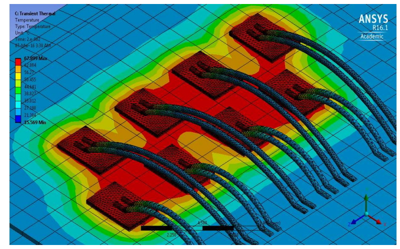


Half cycle of bond wire temp. profiles



FEM thermo-mechanical analysis

- Bond wire foot temperatures are given to FEM structural model
- The highest stresses in the interconnection of bond wires and dies are extracted for all mission profile bins
- 2 hours simulation time for the entire 5 x 5 operating condition matrix

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Thermo-Mechanical Model

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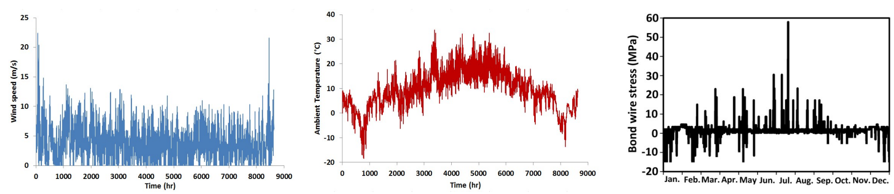
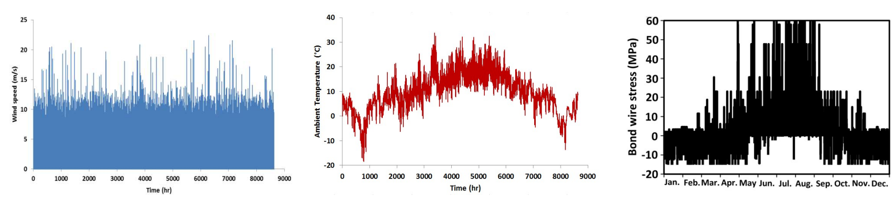


Mission profile A: wind speed, ambient temperature, bond wire stress profile



Mission profile B: wind speed, ambient temperature, bond wire stress profile

- In mission profile "B", bond wires are highly stressed with large stress fluctuations compared to mission profile "A" that will affect the lifetime in long-term operation.

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Lifetime Model

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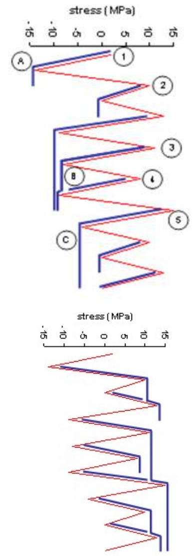
Rainflow counting

- ▶ Reduce the time history to a sequence of tensile peaks and compressive valleys.
- ▶ Each tensile peak or compressive valleys is imagined as a source of water that "drips" down the pagoda.
- ▶ Count the number of half-cycles by looking for terminations in the flow occurring when either:
  - It reaches the end of the time history
  - It merges with a flow that started at an earlier peak/valley; or
  - It flows when an opposite peak/valley has greater magnitude.
- ▶ Assign a magnitude to each half-cycle equal to the stress difference between its start and termination.
- ▶ Pair up half-cycles of identical magnitude (but opposite sense) to count the number of complete cycles. Typically, there are some residual half-cycles.



Images: Wikipedia

Lifetime Model

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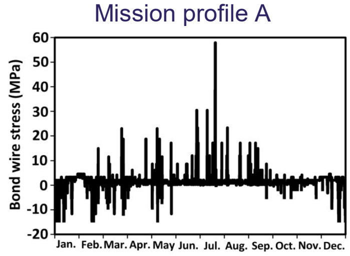
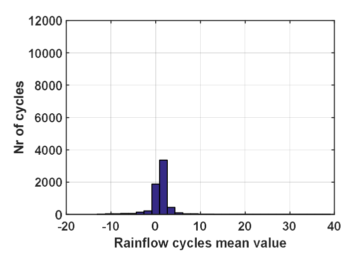
Rainflow counting is used for the cyclic accumulated damage in bond wires

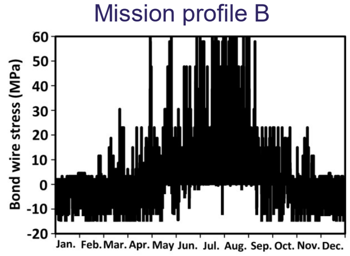
Mission profile A



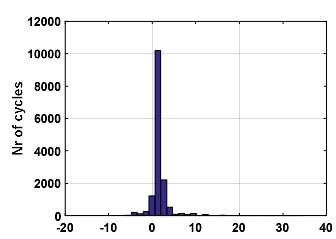
Rainflow counting



Mission profile B



Rainflow counting



Lifetime Model

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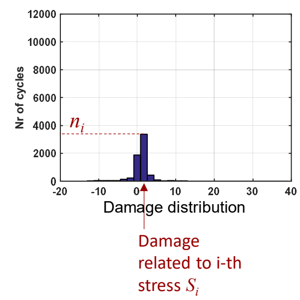
Miner's rule (Fatigue life of the component)

The entire lifetime of the module can be divided into fractions of damage for each bin of the simplified mission profile data. For various bins (load currents and ambient temperatures), the Miner's rule can give an estimation of the life consumption (LC) for the given mission profile, i.e. 1 year.

$$LC\Big|_{1year} = \sum_{i=1}^{k} \frac{n_i}{N_{fi}} \ [\%]$$

i: different applied bins from 1 to k
n_i: the number of cycles accumulated at stress S_i
N_{fi}: the number of cycles to failure at the stress S_i



The expected lifetime (end of life, EOL) can be finally calculated as:

$$EOL = \frac{1}{LC|_{1year}} \ [years]$$

Considering the number of cycles to failure in Aluminum wires – S-N curve – and the period of cycles in the mission profiles, lifetime of mission profile **A** is estimated in 18.2 years and mission profile **B** in 12.5 years.

Ref: A.S. Bahman, F. Iannuzzo, C. Uhrenfeldt, F. Blaabjerg and S. Munk-Nielsen, "Modeling of Short-Circuit-Related Thermal Stress in Aged IGBT Modules," IEEE Trans. Ind. Appl., vol. 53, no. 5, pp. 4788-4795, Sept.-Oct. 2017.

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Short-circuit testing of SiC MOSFETs

- **Testing methods**
- **Results**

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Abnormal conditions

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Why study the behavior of power devices at extreme conditions?

- Highly-reliable applications, such as energy production from renewables require 20 or more years expected life
- In the above time horizon, random failures cannot be neglected
- Random failures are basically related to abnormal events occurring during the component's life

Sources
http://www.windpowerengineering.com/
Wiser R., Bolinger M. "2014 wind technologies market report." – US Department of Energy (2015).
Wang, H.; Liserre, M.; Blaabjerg, F., "Toward Reliable Power Electronics: Challenges, Design Tools, and Opportunities," Industrial Electronics Magazine, IEEE , vol.7, no.2, pp.17,26, June 2013

Testing for Short circuit

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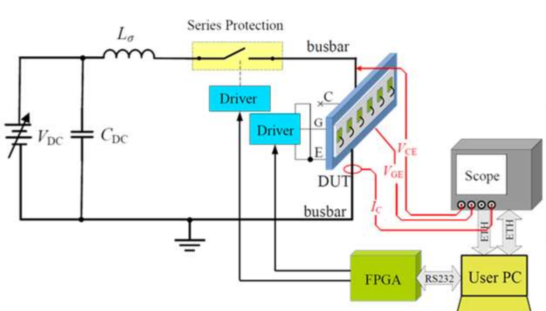
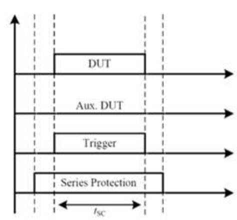
Non-Destructive Tester



Principle schematic



Timing

Photograph

Source: Smirnova, L.; Pyrhonen, J.; Iannuzzo, F.; Rui Wu; Blaabjerg, F., "Round busbar concept for 30 nH, 1.7 kV, 10 kA IGBT non-destructive short-circuit tester," Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on , vol., no., pp.1,9, 26-28 Aug. 2014.

Typical safe short-circuit sequence

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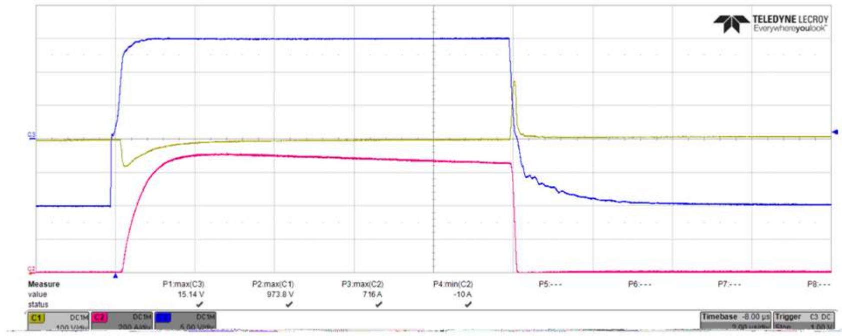
Silicon IGBT

- ▶ Conditions: VCE = 800 V; Pulse width = 10 us



Device under test: 1700 V, 150 A

Instabilities in Silicon Carbide MOSFETs (1/2)

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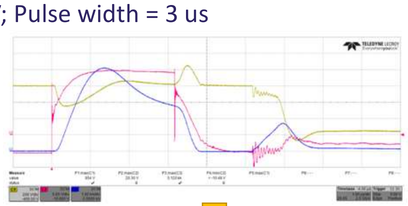
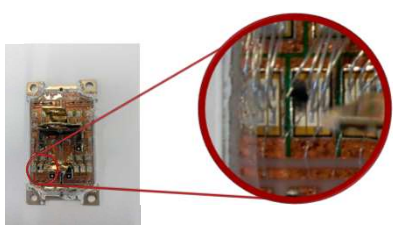
SC tests of 1.2k V, 300 A SiC MOSFET module

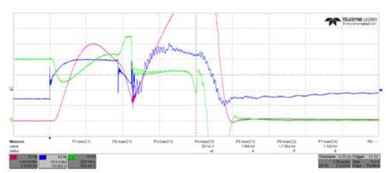
- ▶ VDS = 800 V; Pulse width = 3 us



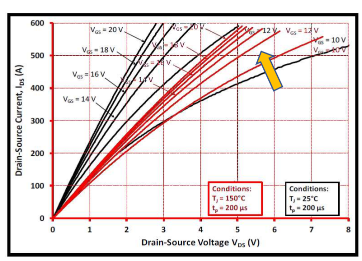
Post-failure analysis
Only one chip out of 6 is blown up



- ▶ VDS = 800 V; Pulse width = 2 us



Interpretation
SiC MOSFETs exhibit Negative Thermal Coefficient (NTC) at low gate voltages



Source: www.wolfspeed.com – CAS300M12BM2 datasheet

Instabilities in Silicon Carbide MOSFETs (2/2)

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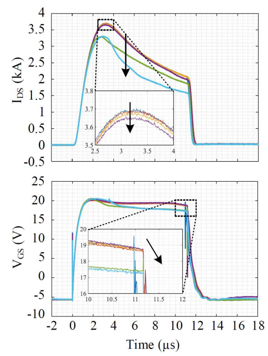
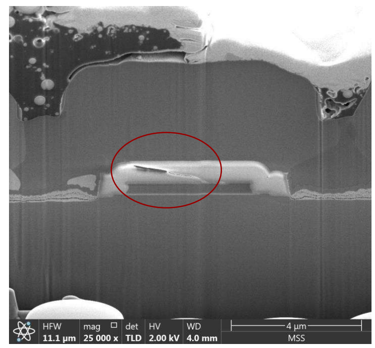
Repetitive short-circuit testing effects on the gate leakage

- ▶ Shorter pulse time has been used
- ▶ The gate oxide leakage increases
- ▶ FA has evidenced a crack in the field oxide, likely due to thermal stress





Source: Du, H., Reigosa, P.D., Iannuzzo, F., Ceccarelli, L., "Investigation on the degradation indicators of short-circuit tests in 1.2 kV SiC MOSFET power modules", (2018) Microelectronics Reliability, 88-90, pp. 661-665.

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Discussion

- ➢ **Status and prospects**

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Present challenges in SiC MOSFET reliability

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1. Cost, cost, cost, …

- Lower cost would mean gaining one more design degree of freedom. Chip area could be not a constraint anymore, and allow full exploitation of SiC potential – reliability included

2. Maximum operating temperature

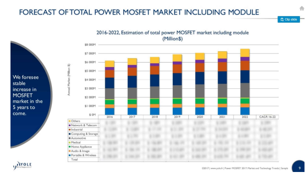
- No doubt: temperature is the second hurdle. In spite of high expectations, operations are limited to Tj,max = 150 °C. To conquer e.g. automotive market (worth 1.5 B$, CAGR 3,4% in 2017), 200 °C stable operation is demanded

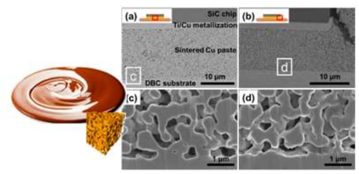
3. New interconnections

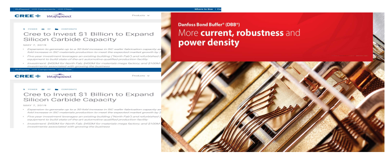
- Temperature swing has become a constraint at the solder layer, too. New (cheap) concepts are demanded

But scenario is very dynamic

- May 2019: Cree invested 1B$ in new wafer fab
- Danfoss to enlarge portfolio with DBB (copper wire bonding)
- Major changes to be expected in the coming 2-3 years







Sources: www.yole.fr, www.cree.com, www.danfoss.com

Y. Gao, S. Takata, C. Chen, S. Nagao, K. Suganuma, A. S. Bahman, F. Iannuzzo, "Reliability analysis of sintered Cu joints for SiC power devices under thermal shock condition", ESREF 2019 Conference, Toulouse, France

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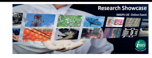
Conclusion

Summary



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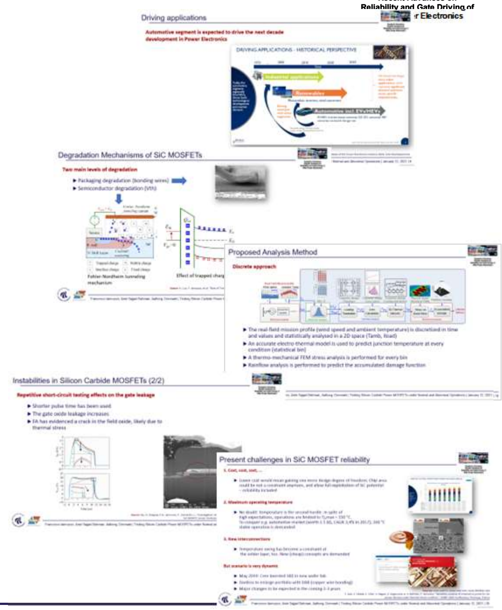
Testing Silicon Carbide Power MOSFETs under Normal and Abnormal Operations

- The power electronics scenario will be vey dynamic in the coming decade, and WBGs are a big part of it
- Wear testing in Silicon Carbide components evidences two distinct failure mechanisms, i.e. bond-wire lift off and threshold voltage shift
- Current density plays a major role in bond-wire lift off, whereas temperature mostly affects threshold voltage shift
- A mission-profile-based approach for life estimation has been presented, which helps coping with the new failure mechanisms
- Abnormal operations are as important as normal ones for SiC reliability assessment, and are currently the most limiting performance
- Present challenges in SiC MOSFET technology are cost, stable operating temperature, and new interconnections



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IMAPS-UK
11-12 January 2021
Online Event

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Thank you

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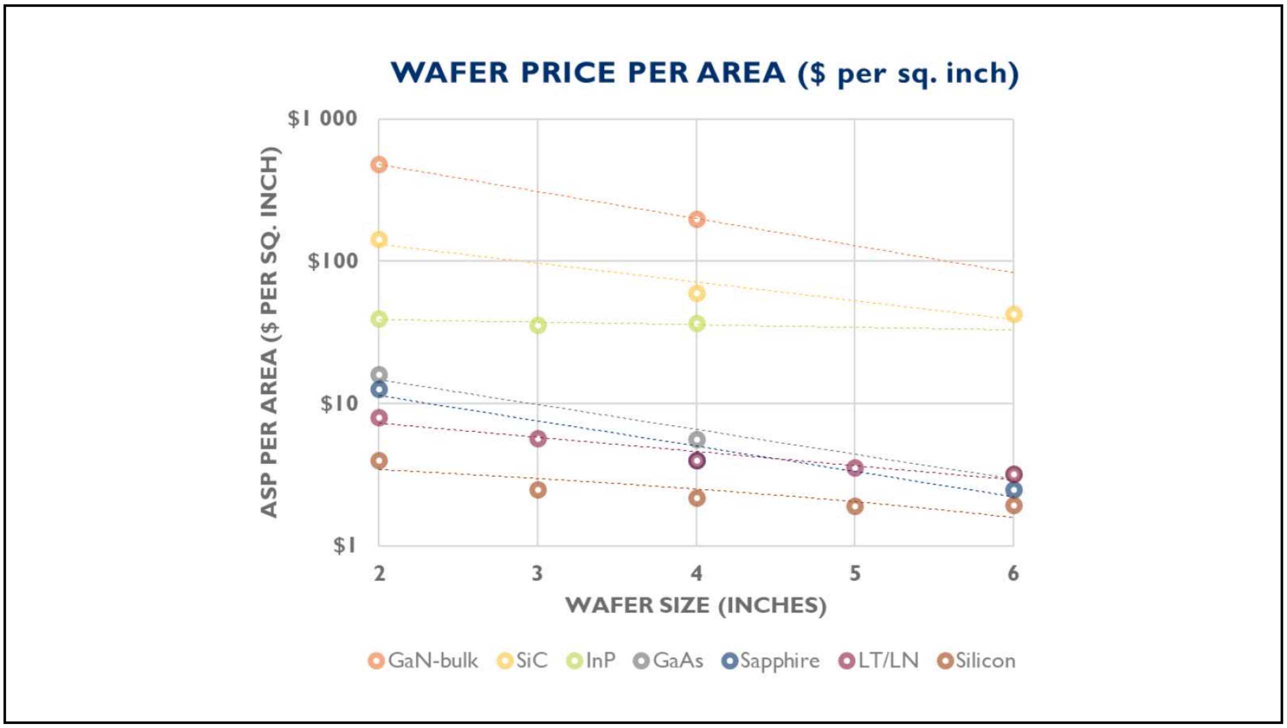
WAFER PRICE PER AREA ($ per sq. inch)
$1 000
$100
$10
$1
ASP PER AREA ($ PER SQ. INCH)
2
3
4
5
6
WAFER SIZE (INCHES)
GaN-bulk
SiC
InP
GaAs
Sapphire
LT/LN
Silicon

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