Newcastle University

iMAPS Research Showcase:
Recent Advances on Reliability and Gate Driving of WBG Power

Optimization of Switching Transients for SiC MOSFETs

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Newcastle University

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Content

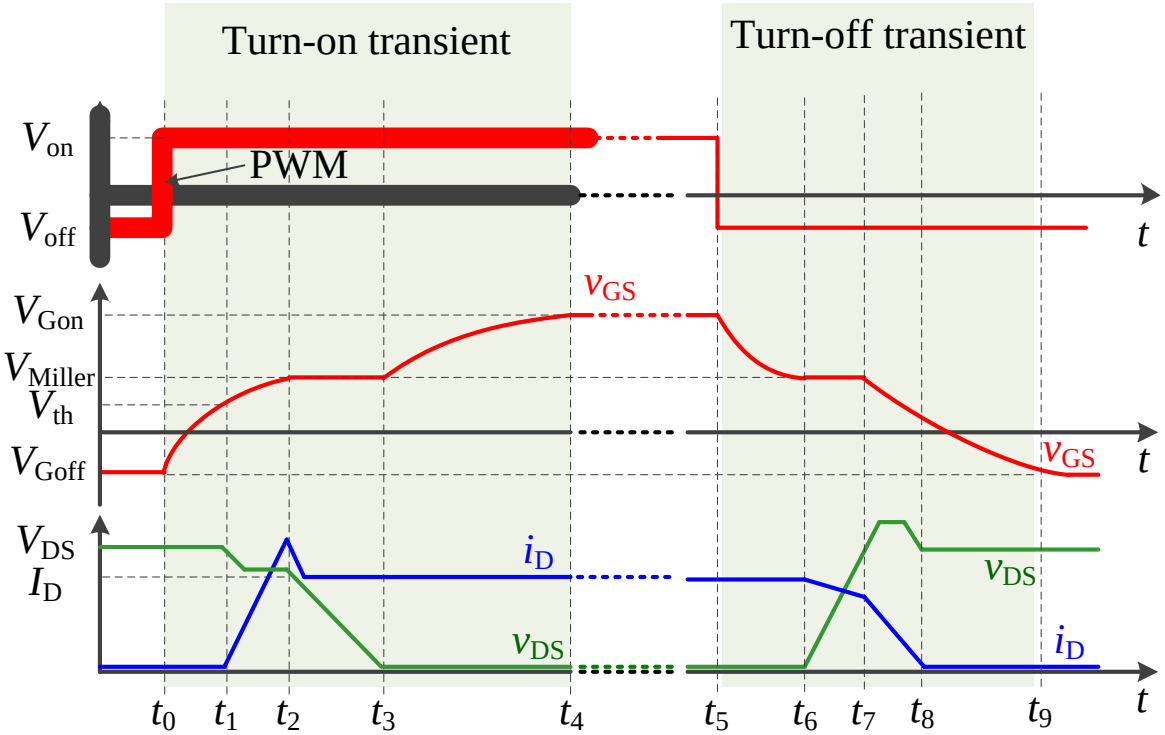
- Introduction
- Switching transient analysis
- Proposed gate driving signal
- Experimental verification
- Conclusion

Introduction

- SiC MOSFETs are ideal for high-efficient, high-frequency and high-power density applications due to their high switching capabilities.
- However, high switching speeds introduce large voltage/current overshoots and high oscillations, resulting in EMI, losses and reliability issues.
- Methods to reduce overshoots and oscillations are:
  - ☐ Oscillation damping snubber circuit — X additional components
  - ☐ Resonant circuit — X additional components
  - ☐ Gate driving signal optimization — ✓ no need to change power circuit
- This presentation proposes an optimized gate driving signal to reduce voltage/current overshoots and oscillations without increasing significantly switching losses.

Switching transient analysis

Structure of the presentation



Conceptual switching waveforms

- Turn-on di/dt (t1~t2)
- Turn-on dv/dt (t2~t3)
- Current overshoot (t2)
- Turn-on oscillation (t2 ~t3)

- Turn-off dv/dt (t6~t7)
- Turn-off di/dt (t7~t8)
- Voltage overshoot (t7~t8)
- Turn-off oscillation (t8 ~t9)

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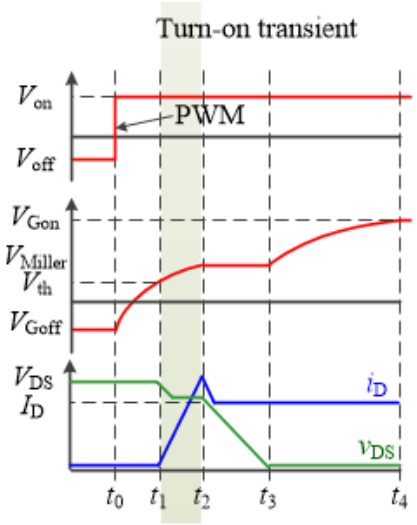
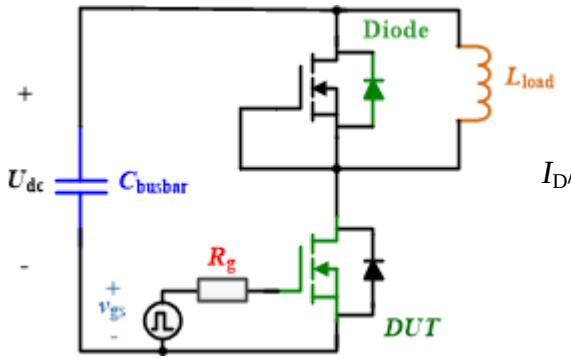
Switching transient analysis

Turn-on di/dt (t1~t2) varying Rg

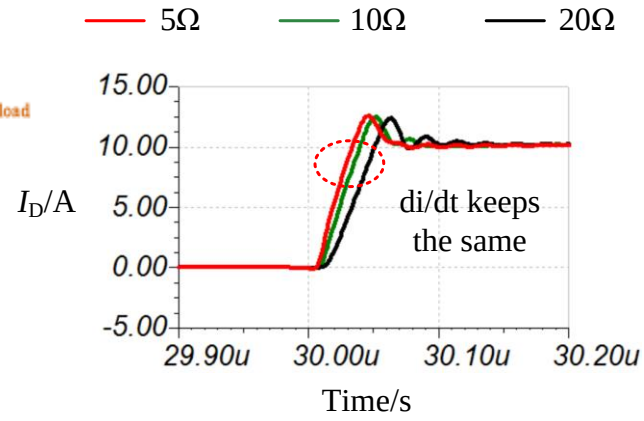
Test condition: 250V DC voltage 10A load current, +15V/0V gate voltage, SCT3060



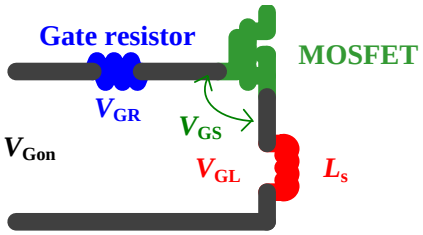
Turn-on conceptual waveform



Schematic of the simulation circuit



Turn-on di/dt simulation results



MOSFET equivalent circuit

$$\begin{cases} V_{Gon} = V_{GR} + V_{GS} + V_{GL} \\ V_{GR} = I_g \cdot R_g \\ V_{GL} = L_s \cdot \dfrac{di_D}{dt} \end{cases}$$

- Turn-on di/dt is dominated by the gate current
- Changes in the gate resistor makes only limited impact on di/dt due to the parasitic source inductance (Ls)

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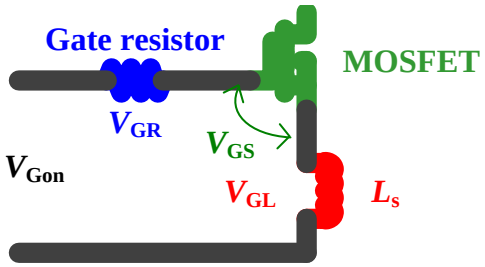
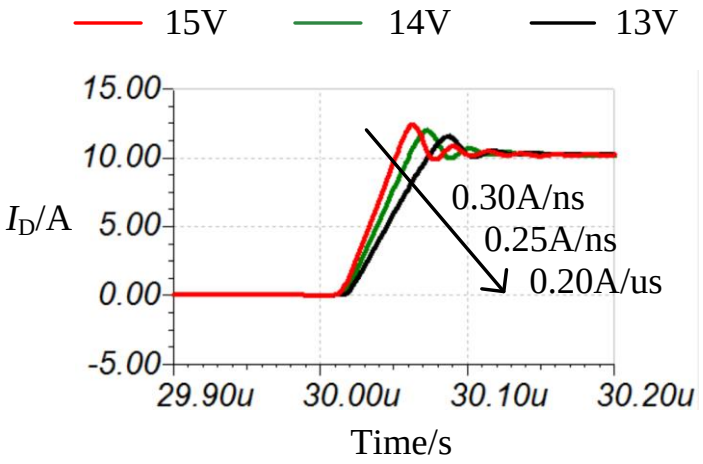
Switching transient analysis

Turn-on di/dt (t1~t2) varying VGon



MOSFET equivalent circuit

$$\begin{cases} V_{Gon} = V_{GR} + V_{GS} + V_{GL} \\ V_{GR} = I_g \cdot R_g \\ V_{GL} = L_s \cdot \dfrac{di_D}{dt} \end{cases}$$



Turn-on di/dt simulation results

Test condition:

250V DC voltage

10A load current

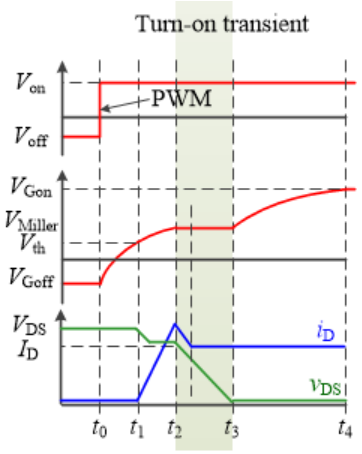
Rg = 20ohm

ROHM SCT3060

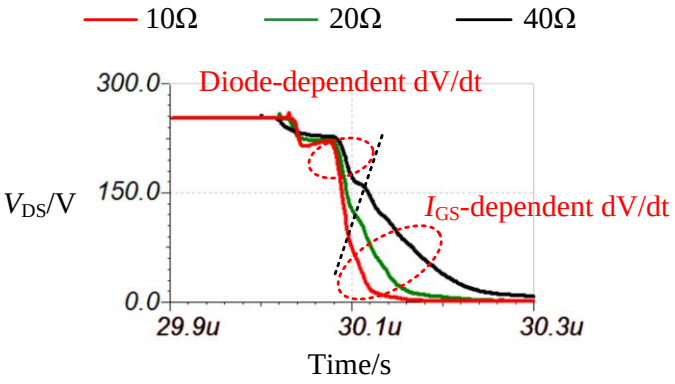
- The gate current can be changed by manipulating the turn-on gate voltage, instead of changing the gate resistor.
- However, the best way to control turn-on di/dt is to control the gate current directly.

Switching transient analysis

Turn-on dv/dt (t2~t3)



Turn-on conceptual waveform



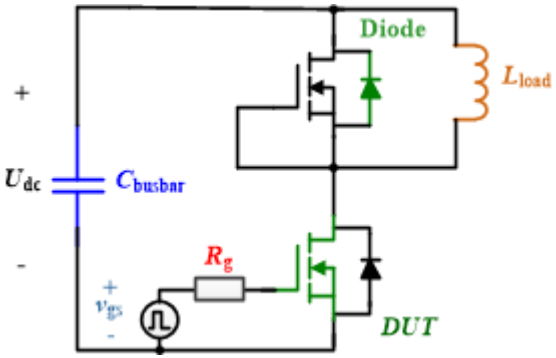
Turn-on dv/dt simulation results

Test condition:

250V DC voltage

10A load current

ROHM SCT3060

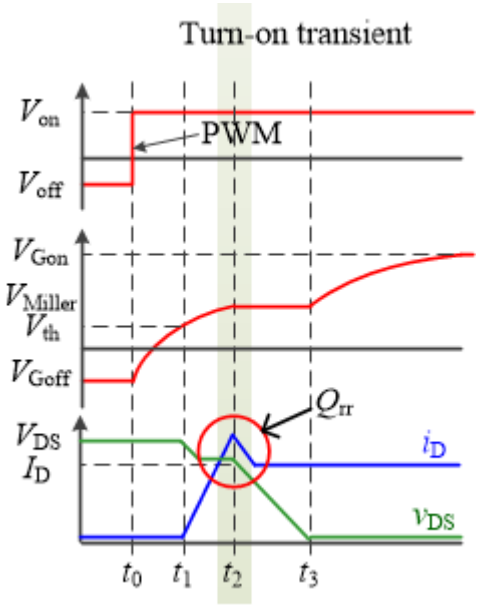


Schematic of the simulation circuit

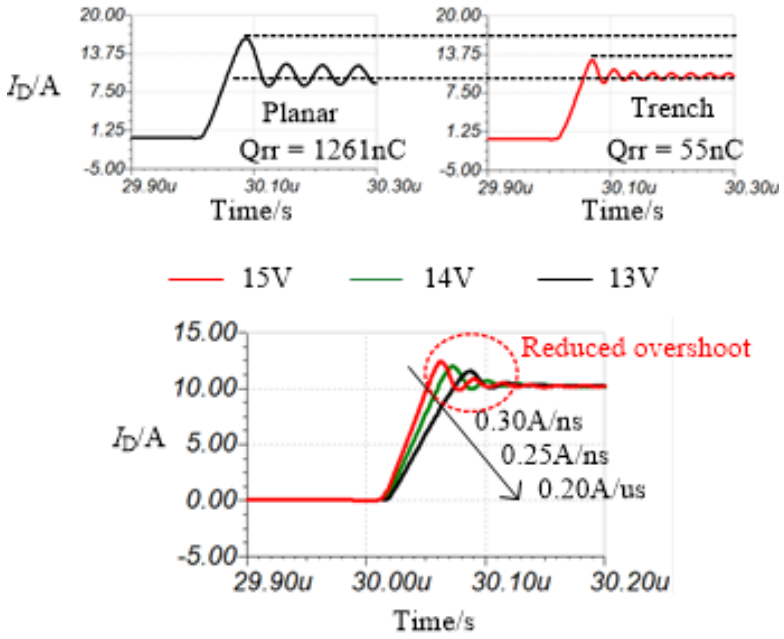
- Turn-on dv/dt consists of 2 processes. dv/dt is firstly dominated by the reverse recovery current of the diode, and then by the gate resistor which dictates the gate current.

Switching transient analysis

Turn-on current overshoot (t2)



Turn-on conceptual waveform



Turn-on current overshoot simulation results

- The turn-on current overshoot is dominated by the reverse recovery charges of the diode and the di_D/dt.

But which period di_D/dt is the most important?

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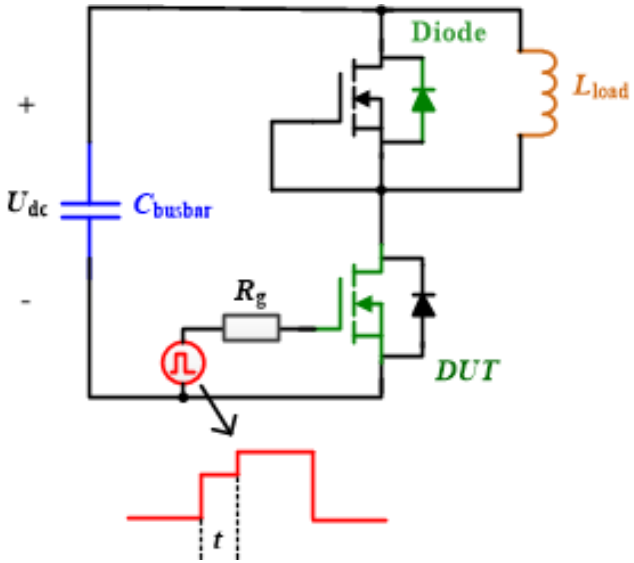
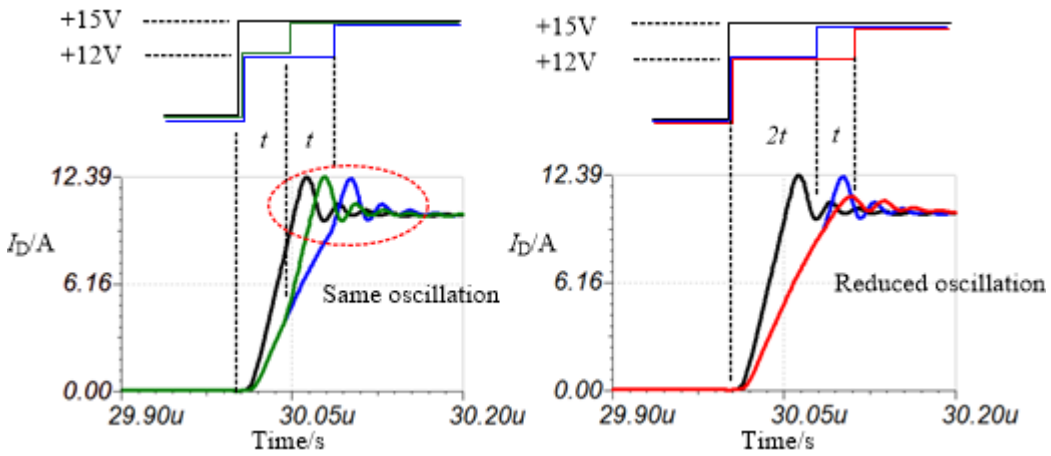
Switching transient analysis

Turn-on oscillation (t2 ~t3)



Schematic of the simulation circuit

Example of step gate driver: AgileSwitch

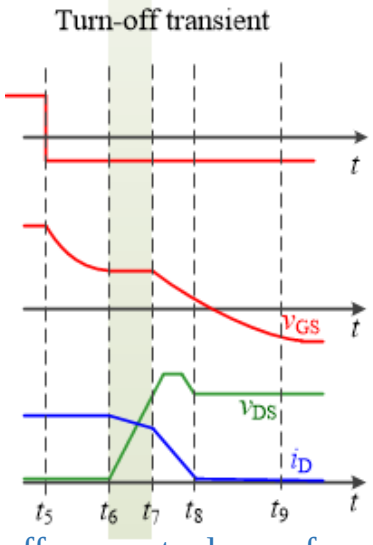


Turn-on oscillation simulation results

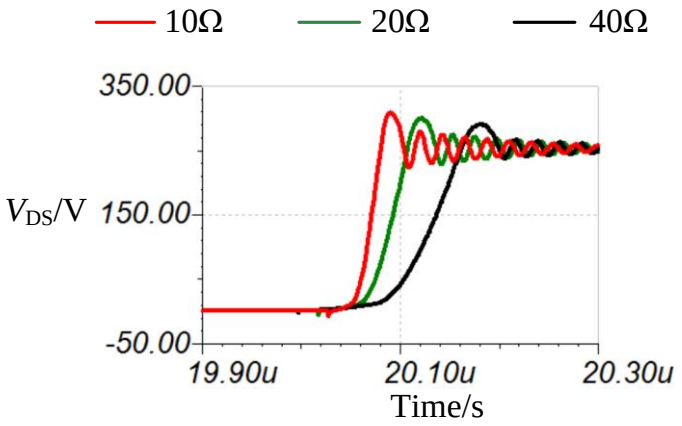
- di_D/dt has no influence on the oscillation or the overshoot, when the gate voltage step occurs before t2

Switching transient analysis

Turn-off dv/dt (t6~t7) varying Rg



Turn-off conceptual waveforms



Turn-off dv/dt simulation results

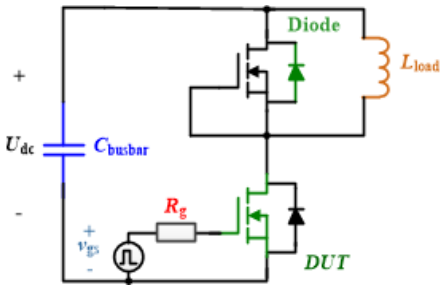
Test condition:

250V DC voltage

10A load current

+15V/0V gate voltage

ROHM SCT3060



Schematic of the simulation circuit

- As expected, the turn-off dv/dt is influenced by the gate resistor.

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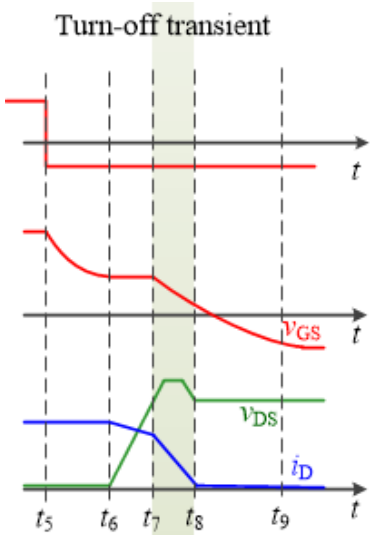
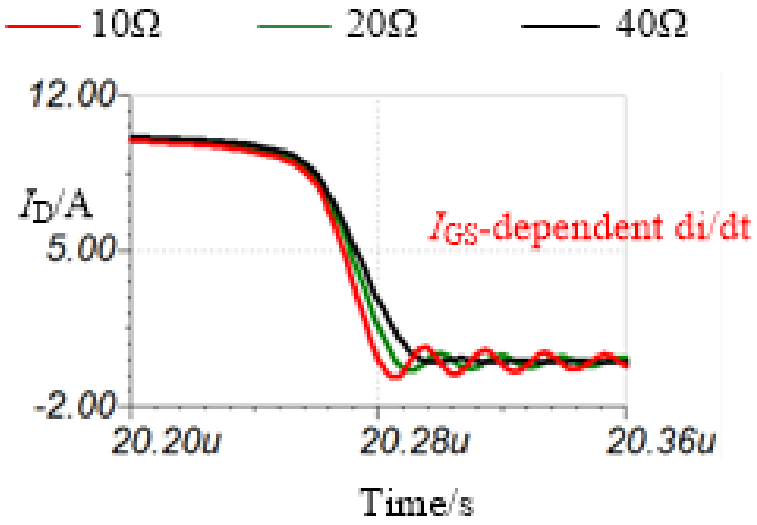
Switching transient analysis

Turn-off di/dt (t7~t8)



Turn-off conceptual waveforms



Turn-off di/dt simulation results

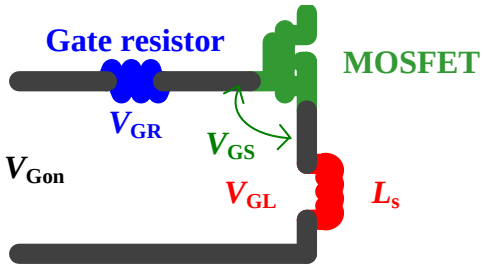
Test condition:

250V DC voltage

10A load current

+15V/0V gate voltage

ROHM SCT3060



MOSFET equivalent circuit

- Turn-off di_D/dt is influenced by the gate current (i_{GS});
- Another value that impact di_D/dt is Ls.

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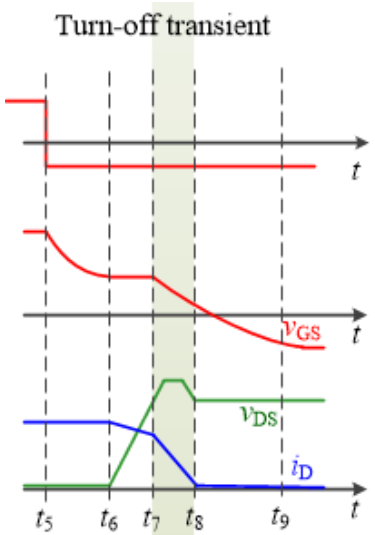
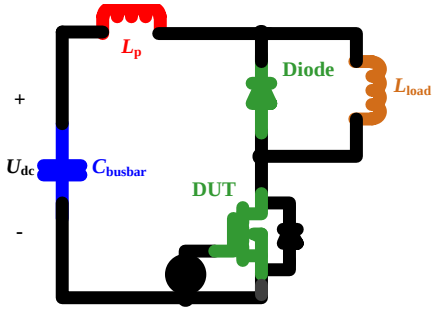
Switching transient analysis

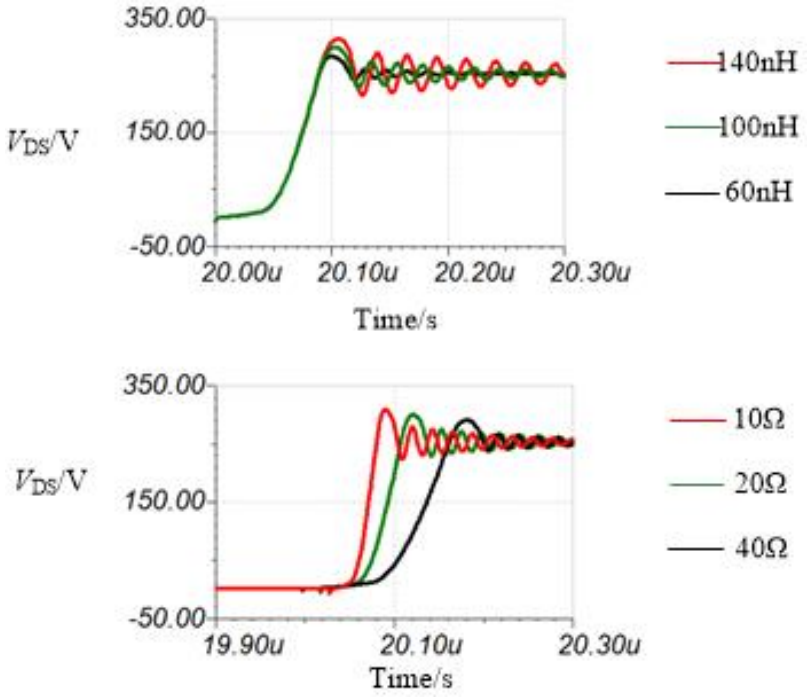
Turn-off voltage overshoot(t7~t8)



Turn-off conceptual waveforms



Schematic of the simulation circuit



Turn-off di/dt simulation results

- As expected, the turn-off voltage overshoot is influenced by the parasitic inductance of the bus bar and the gate resistor thus current (i_{GS}).

$$v_{DS} + v_D = U_{dc} + v_{Lp} = U_{dc} + L_p \cdot \frac{di_{DS}}{dt}$$

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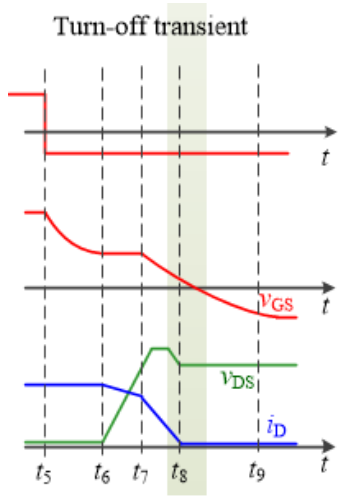
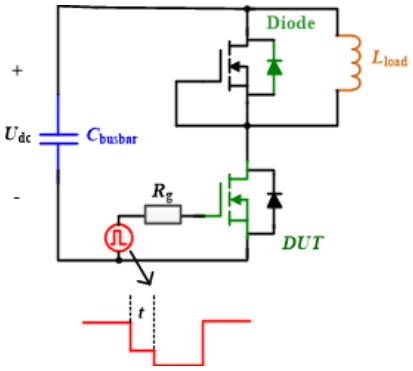
Switching transient analysis

Turn-off oscillation(t8 ~t9)

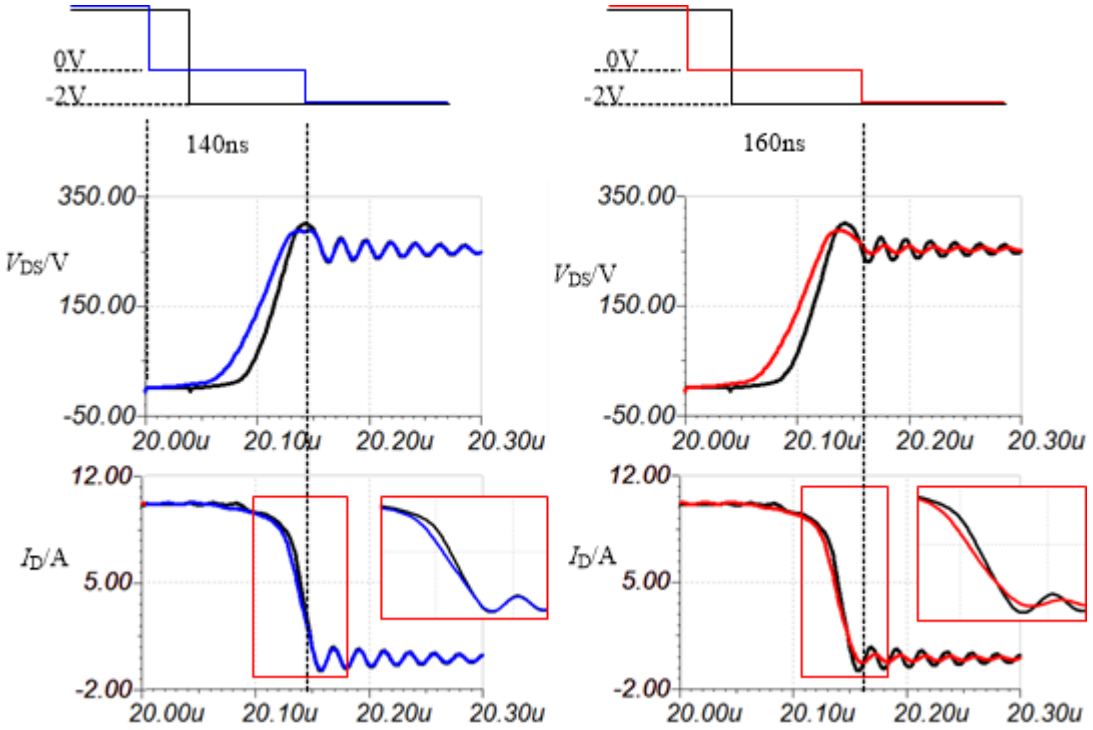


Turn-off conceptual waveforms



schematic of simulation circuit

Example of step gate driver: AgileSwitch



Turn-off oscillation simulation results

- Turn-off oscillations are not the result from di/dt or dv/dt so long the time step is before the voltage overshoot

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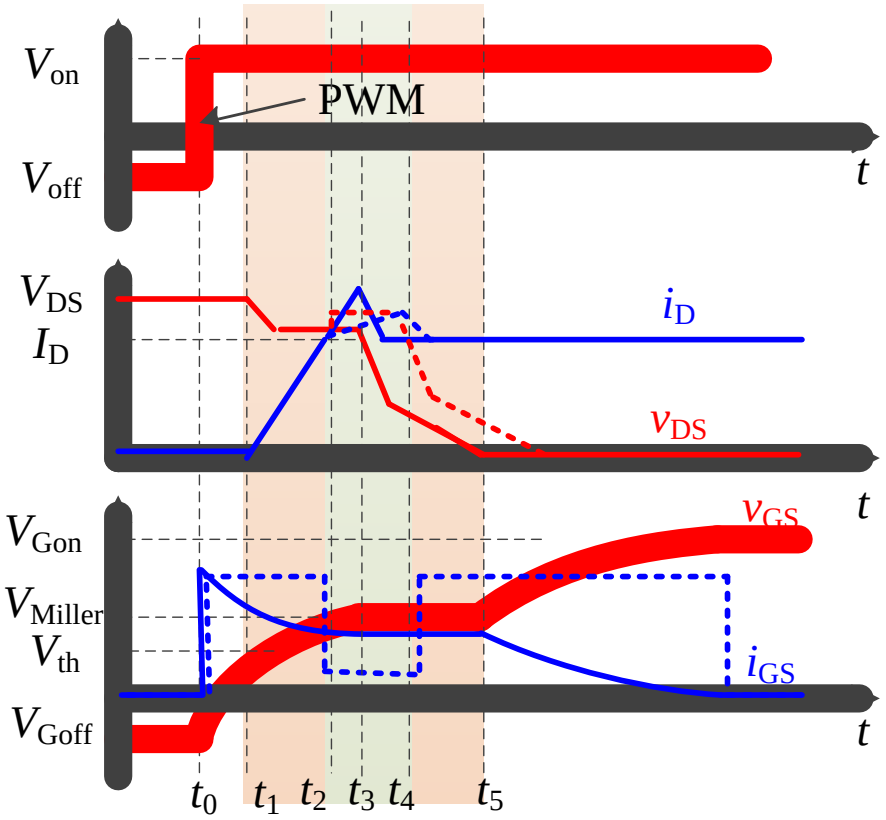
Switching transient analysis

Summary

- There are some parameters gate drivers cannot control, e.g. the impact caused by the reverse recovery effect of the diode and inductance L_s and L_{stray};
- Most of the switching performances are determined by the gate current, therefore, gate drivers should be current-controlled not voltage-controlled.

Proposed gate driving signal

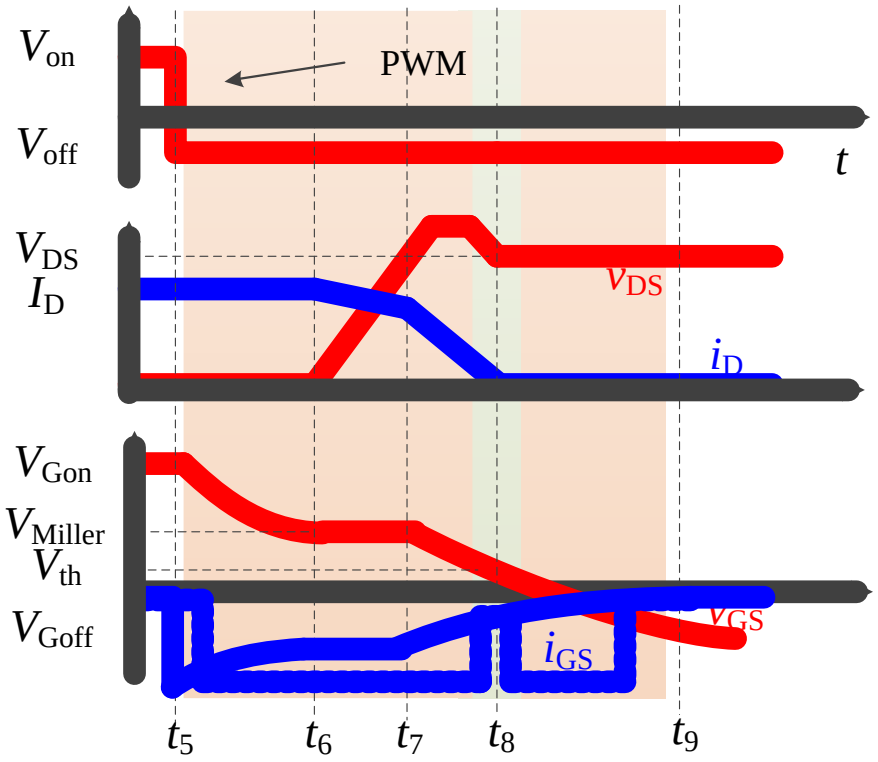
U-shape gate driving signal for turn-on transient optimization



- High gate current in the periods t0~t2, t4~t5 keeps di/dt and dv/dt at high level to reduce losses
- Low current in the period t2~t4 to reduce the oscillation and the current overshoot
- The increase of switching losses is less compared to traditional methods to reduce di/dt and dv/dt

Proposed gate driving signal

n-shape at t8 gate driving signal for turn-off transient optimization

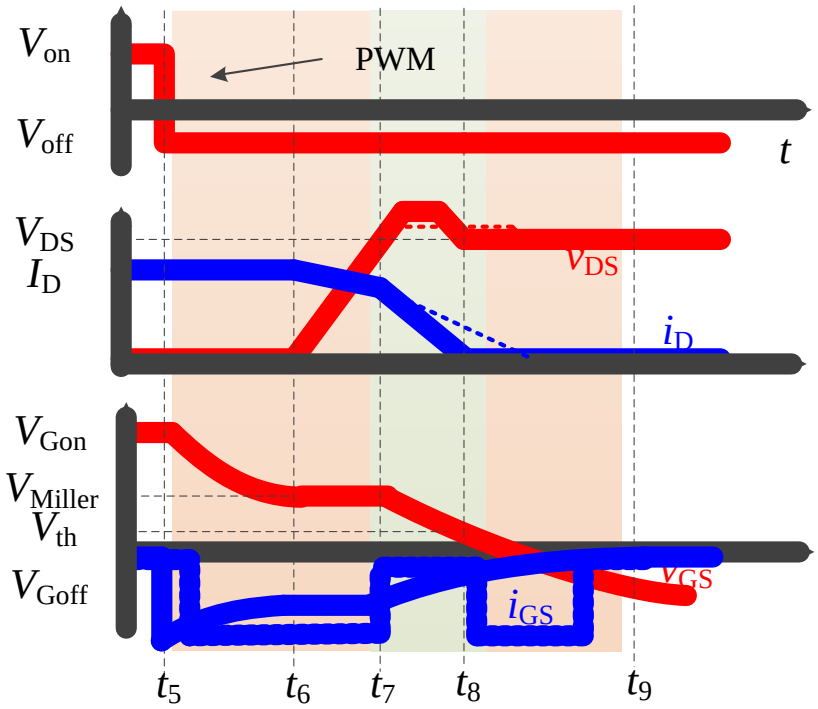


For oscillation only:

- High gate current in the period t5~t8 keeps di/dt and dv/dt at high level to reduce losses.
- The di/dt has highest change at t8, resulting in high oscillation. Low current at t8 reduces the change, therefore reduces the oscillation.
- Oscillation is reduced with no additional switching loss, but voltage overshoot remains unchanged.

Proposed gate driving signal

n-shape (t7-t8) gate driving signal for turn-off transient optimization

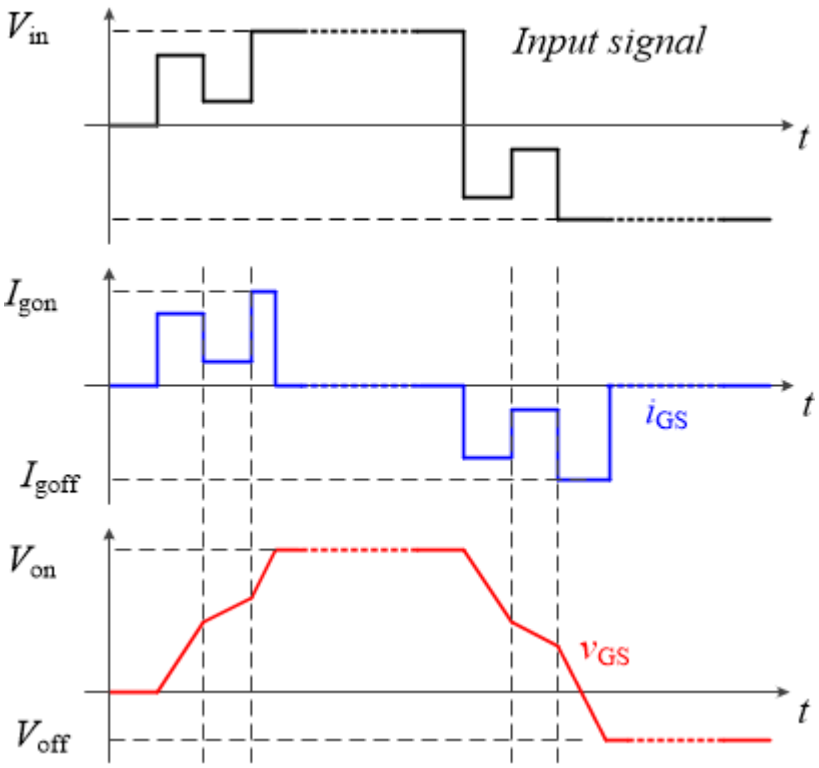


For both oscillation and overshoot:

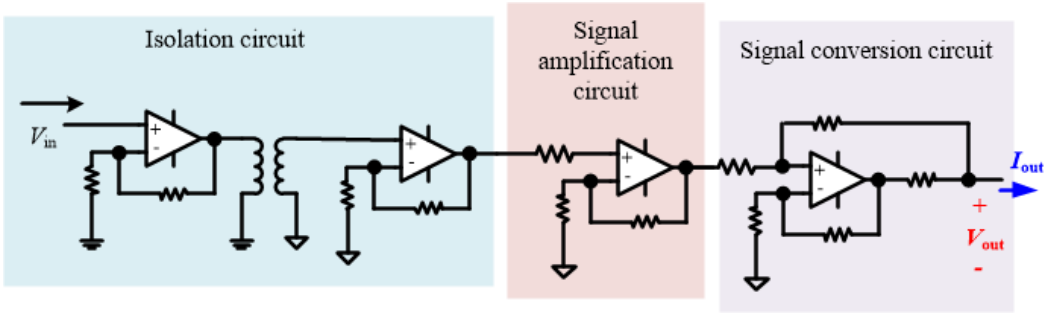
- High gate current in the period t5~t7 keeps dv/dt at high level to reduce losses.
- Low gate current in the period t7~t8 keeps di/dt low to reduce the overshoot and oscillation.

Experimental verification

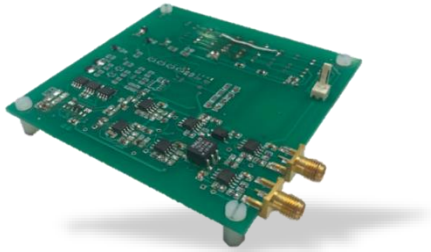
Design of an active gate driver



Conceptual gate waveforms



Schematic of the gate driver circuit



Picture of the gate driver circuit

Performance of the gate driver

Voltage range	15V/-5V
Current range	0 – 200mA
Time step	13.3ns – 10us

- The input signal is pre-programmed

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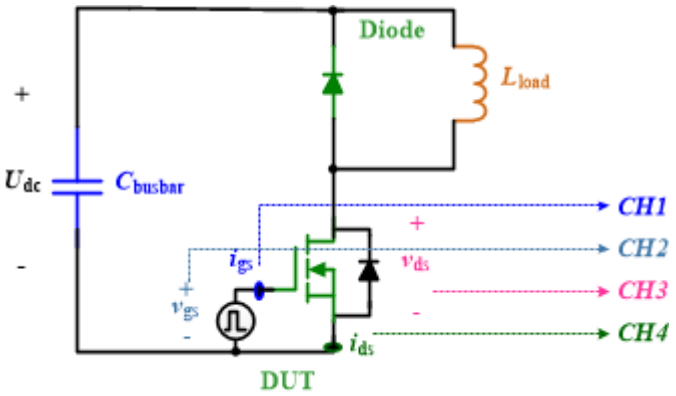
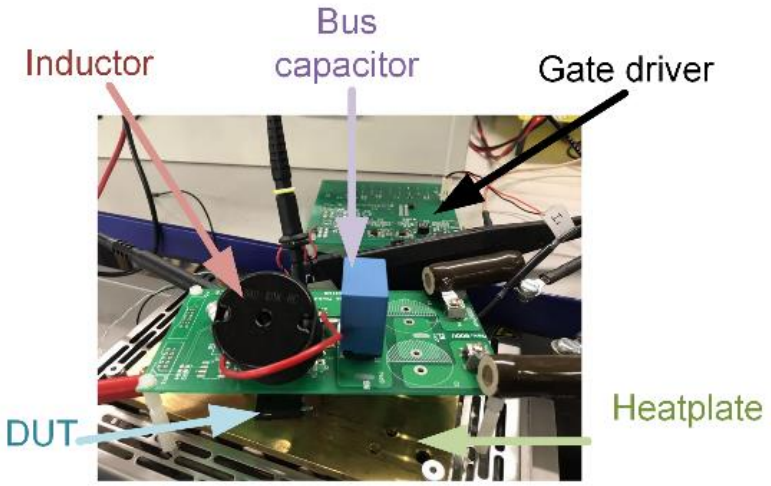
Experimental verification

Design of double pulse test platform



Schematic of the test platform



Picture of the test platform

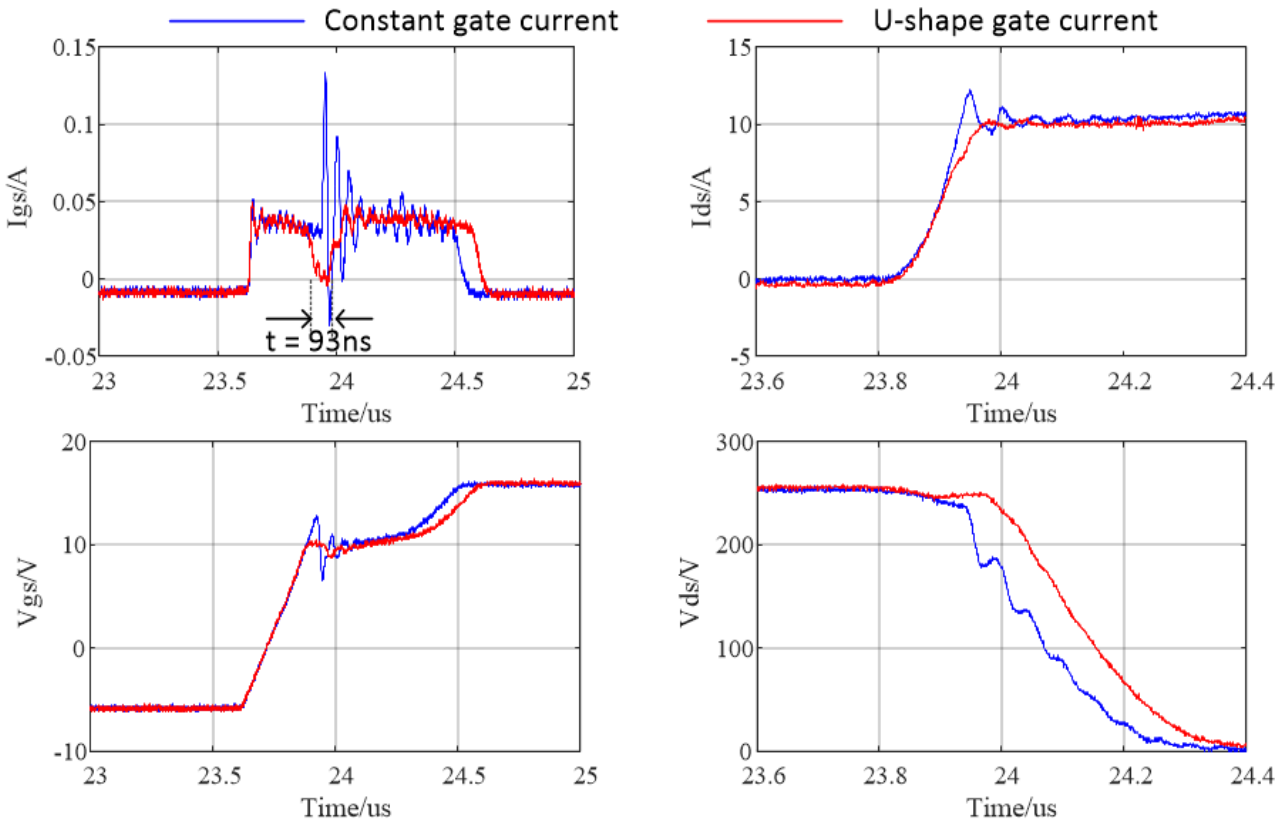
Test condition:

- DC voltage: 250V Load current: 10A
- Diode: CREE C3M0065090D (900V 36A)
- MOSFET: ROHM SCT3060AL (650V 39A)

Experimental verification

U-shape gate current signal for turn-on transient optimization

Oscillation and overshoot are reduced; di/dt and dv/dt remains unchanged.

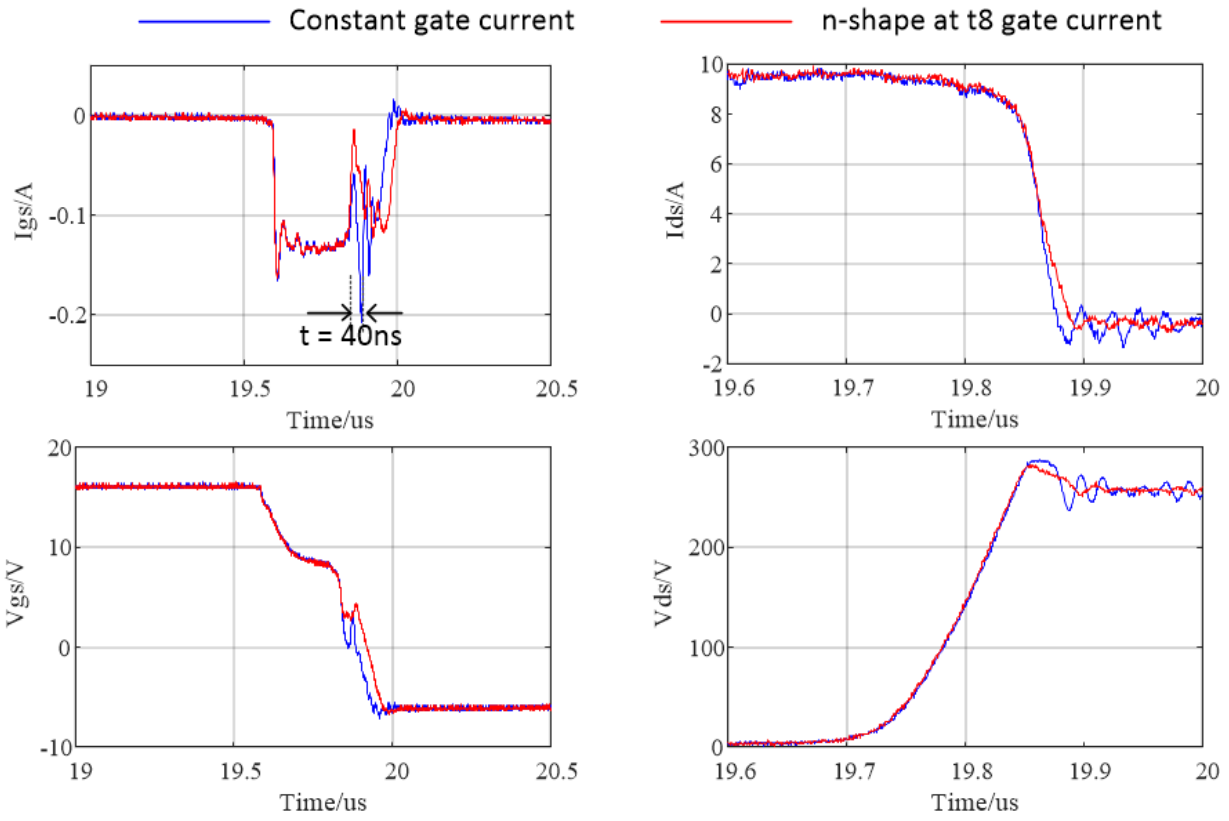


Experimental results

Experimental verification

n-shape gate current signal for turn-off transient optimization

Oscillation is reduced; di/dt and dv/dt remains unchanged.

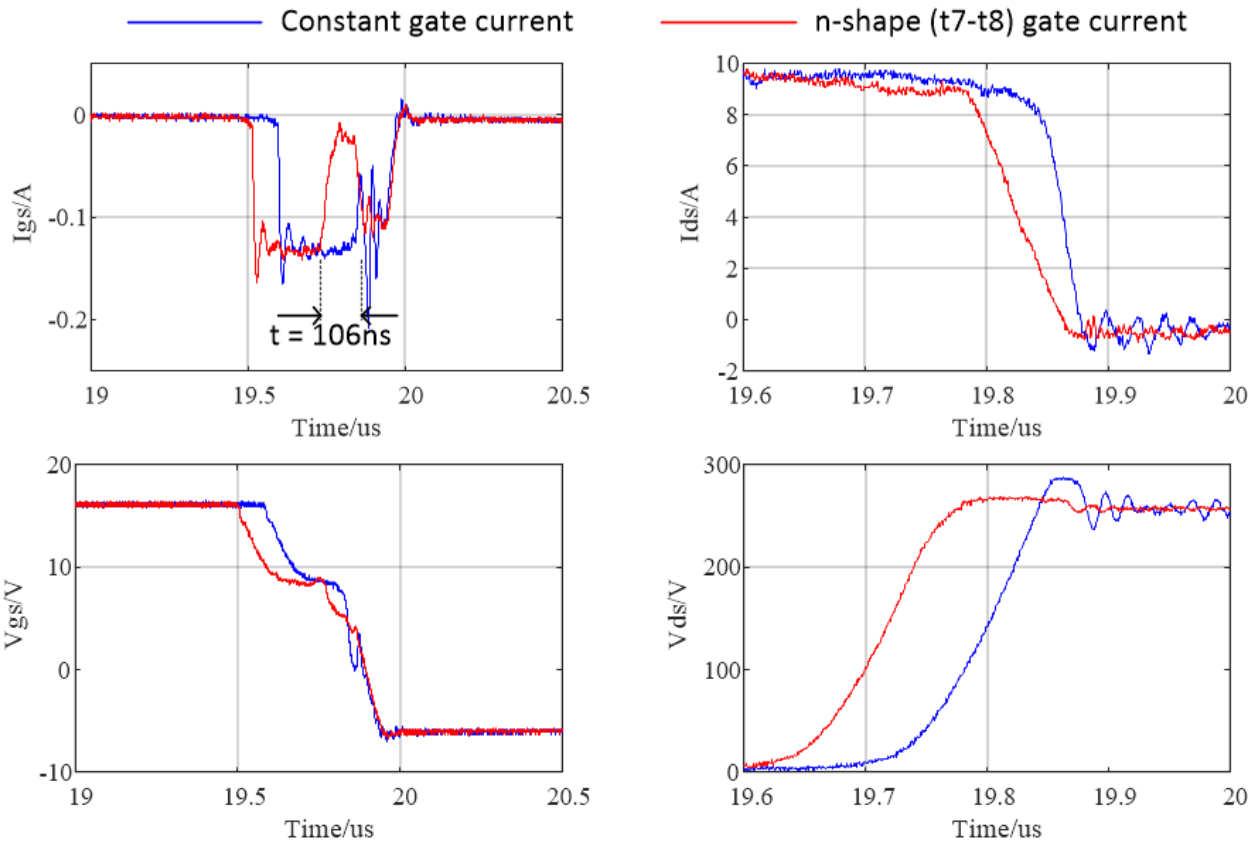


Experimental results

Experimental verification

n-shape gate current signal for turn-off transient optimization

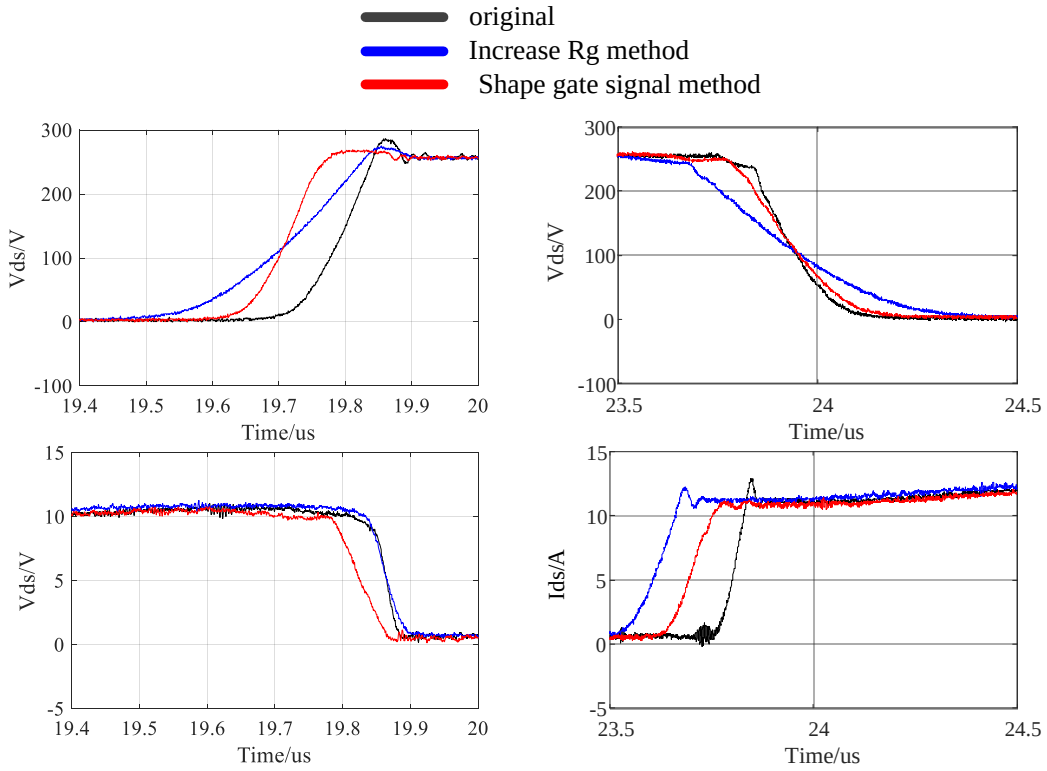
Oscillation and overshoot are reduced; dv/dt remains unchanged.



Experimental results

Experimental verification

Comparison with the traditional method to reduce voltage/current overshoots



Experimental results

Performance comparison

Methods	Original	Rg	Shape
Eoff	0.24mJ	0.40mJ	0.30mJ
Eon	0.36mJ	0.86mJ	0.62mJ
I_{over}	1.92A	1.12A	0.40A
V_{over}	28V	19V	11V

Next Steps

1. Optimize the U-shape / n-shape signal;
2. Produce gate driver version 3 with higher output current and FPGA control to achieve higher bandwidth;
3. Design the concept of feedback control using load current.

Conclusion

- The factors impacting switching transients have been investigated;
- A driving signal is proposed to improve the switching performance in terms of voltage/current overshoots and oscillations;
- A gate driver was designed to evaluate the effectiveness of the proposed gate driving signal.

Acknowledgement

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC), UK, under the project of Reliability, Condition Monitoring and Health Management Technologies for WBG Power Modules (EP/R004366/1).

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Mr. Xiang Wang
Prof. Volker Pickert
Dr. Haimeng Wu
Mr. Bowen Gu
Dr. Weichi Zhang
Mr. Joel Holland

Newcastle University

Thank you!

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