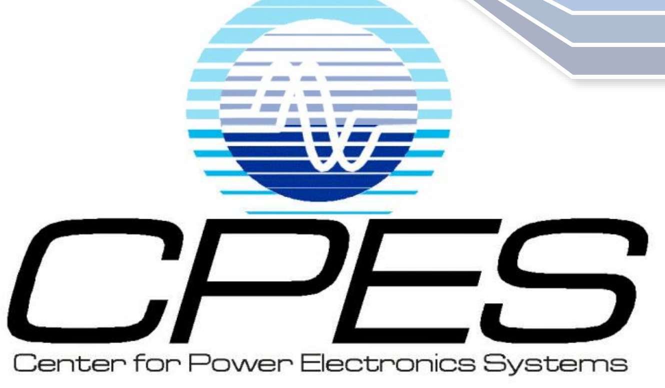

Medium-Voltage SiC Power MOSFET Packaging: An International Collaboration

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Dushan Boroyevich, Rolando Burgos

July 5, 2018

Background

- **High-voltage (≥ 10 kV) silicon carbide (SiC)** devices increase the **power density** and reduce the **complexity** of high-power systems.
- <u>Applications</u>: urban distribution, wind turbines, more-electric ships
- <u>Objective</u>: develop an **optimized package for 10 kV SiC MOSFETs**

1st-Gen. 10 kV, 120 A SiC MOSFET Module Testing

PEBB 6000

$I = C(dv/dt)$

10 kV, 120 A SiC MOSFET/JBS Module

I_{ground} (A) vs. Time [ms] (0–50), range -200 to 200

I_L (A) vs. Time (µs) (0–500), range 90 to 115

Objective:

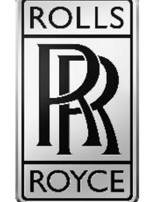
To develop a high-density, high-speed, 10 kV SiC MOSFET power module.

Challenges:

I. **High Density + High Voltage = High Electric Field**

II. **Fast Switching = Voltage Overshoot, Current Imbalance, EMI**

III. **High Density + High Power = High Heat Flux Density**



Substrate Design: Electric Field Reduction

Simulated Electric Field

6 kV
Triple point
0 V
Substrate1
Heat Sink

6 kV
0 V
Substrate1
Floating
Substrate2
Heat Sink

6 kV
0 V
Substrate1
3 kV
Substrate2
Heat Sink

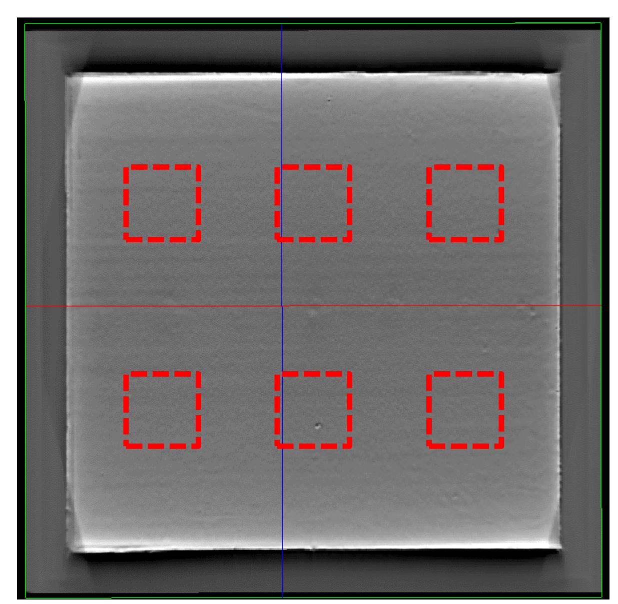
D1
S1D2
DBA1
DBA2
Stacked Substrates
0
20
40 (mm)

D1
G1
S1
S1D2
G2
S2
S2

➢ ***>50 % decrease in peak electric field***

Substrate Attach: Large-area Ag Sintering (250 °C, 5 MPa)

XCT scan of
DBA-DBA attach
(50 x 50 mm)



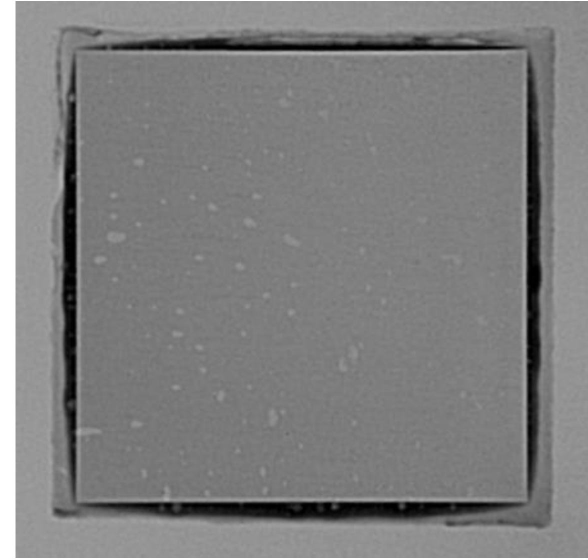
D1
S1D2
DBA1
DBA2
Stacked Substrates
0
20
40 (mm)

G1
S1
S1D2
G2
S2
S2
D1

➢ ***0.11–0.14 K/W thermal resistance***

Die Attach: Pressure-less Ag Sintering (230 °C for 90 min)

X-ray image of die attach layer



10 kV, 350 mΩ SiC MOSFET

D1

S1D2

DBA1

DBA2

Stacked Substrates

D1

G1

S1

S1D2

G2

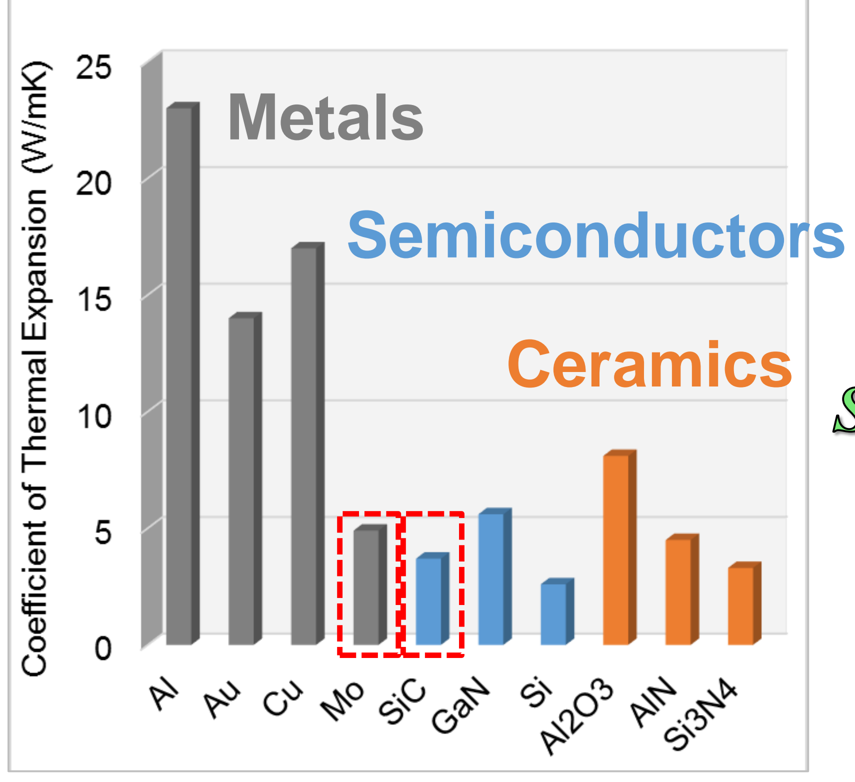
S2

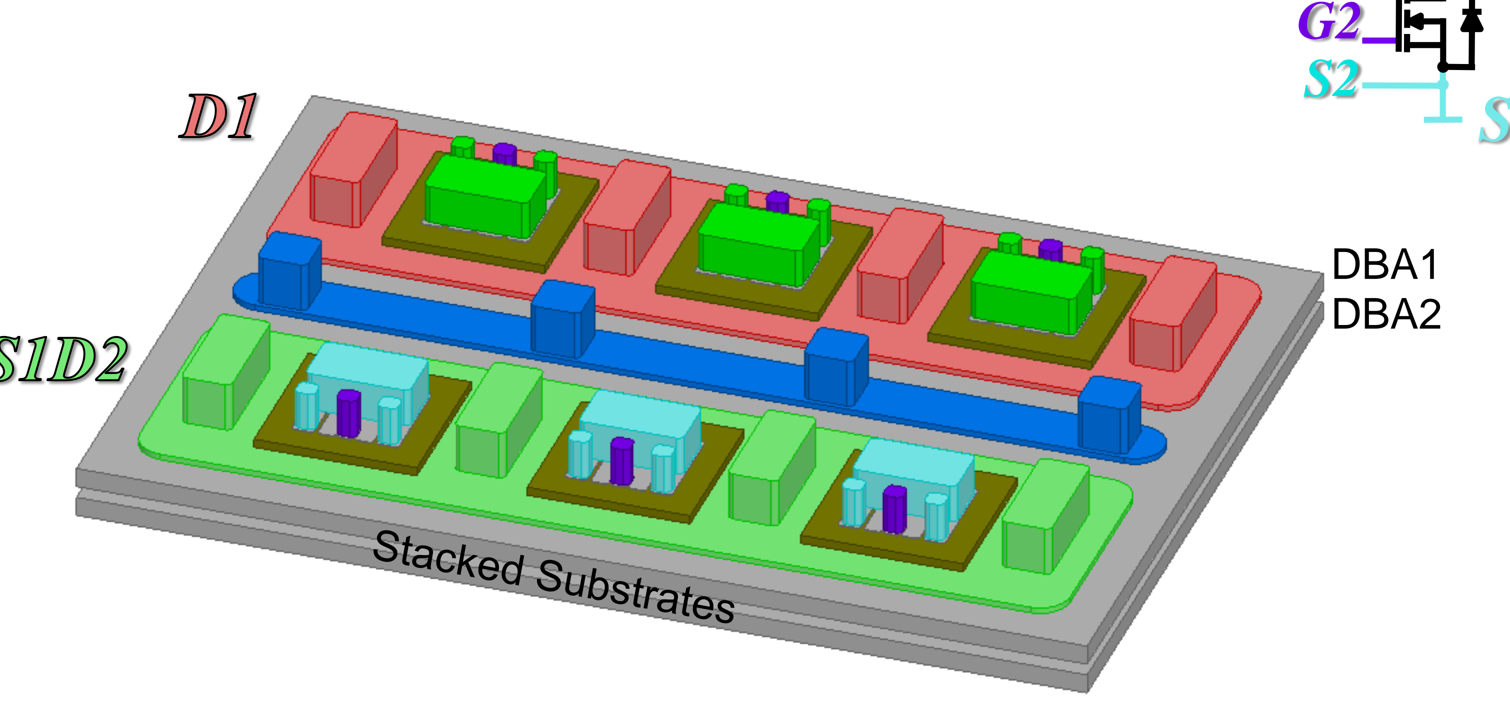
S2

0 20 40 (mm)

- ***Low voiding content and 18.4 MPa bonding strength***

Interconnect: Molybdenum Posts Instead of Wire Bonds

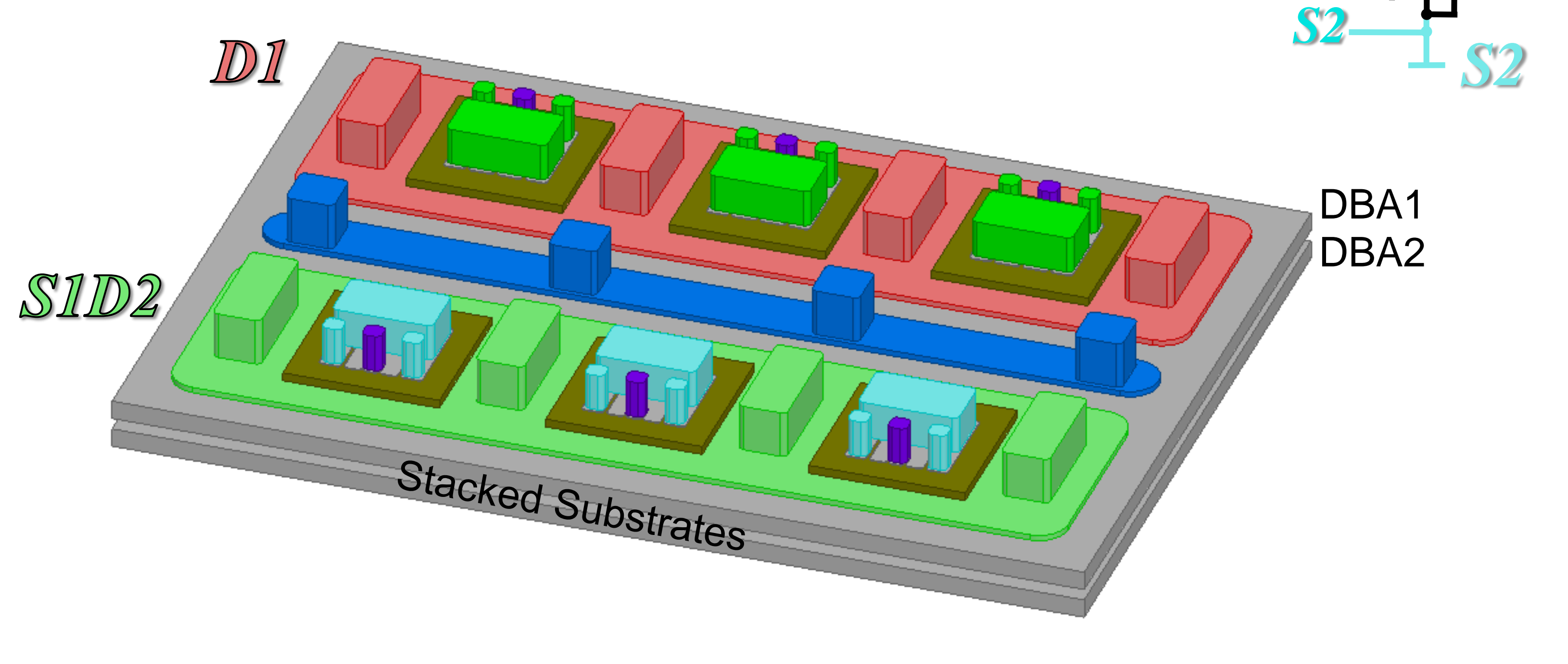




➢ ***Molybdenum increases reliability***

Post Attach: Ag Sintering

Sintered molybdenum posts to 10 kV MOSFET



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Top DBA Attach: Sn10/Pb88/Ag2 Solder Paste

X-ray image of die, posts, and DBA in assembled module

S1 G1 S1

S1D2

D1

S1D2

S2

S1 G1 S1

D1

S1D2

S2 G2 S2

S2

Stacked Substrates

Stacked Substrates

D1

G1

S1

S1D2

G2

S2

S2

0 20 40 (mm)

➢ ***Good alignment** is achieved during assembly*

Wire-bond-less 10 kV SiC MOSFET Power Module

L_{power}= 4 nH*

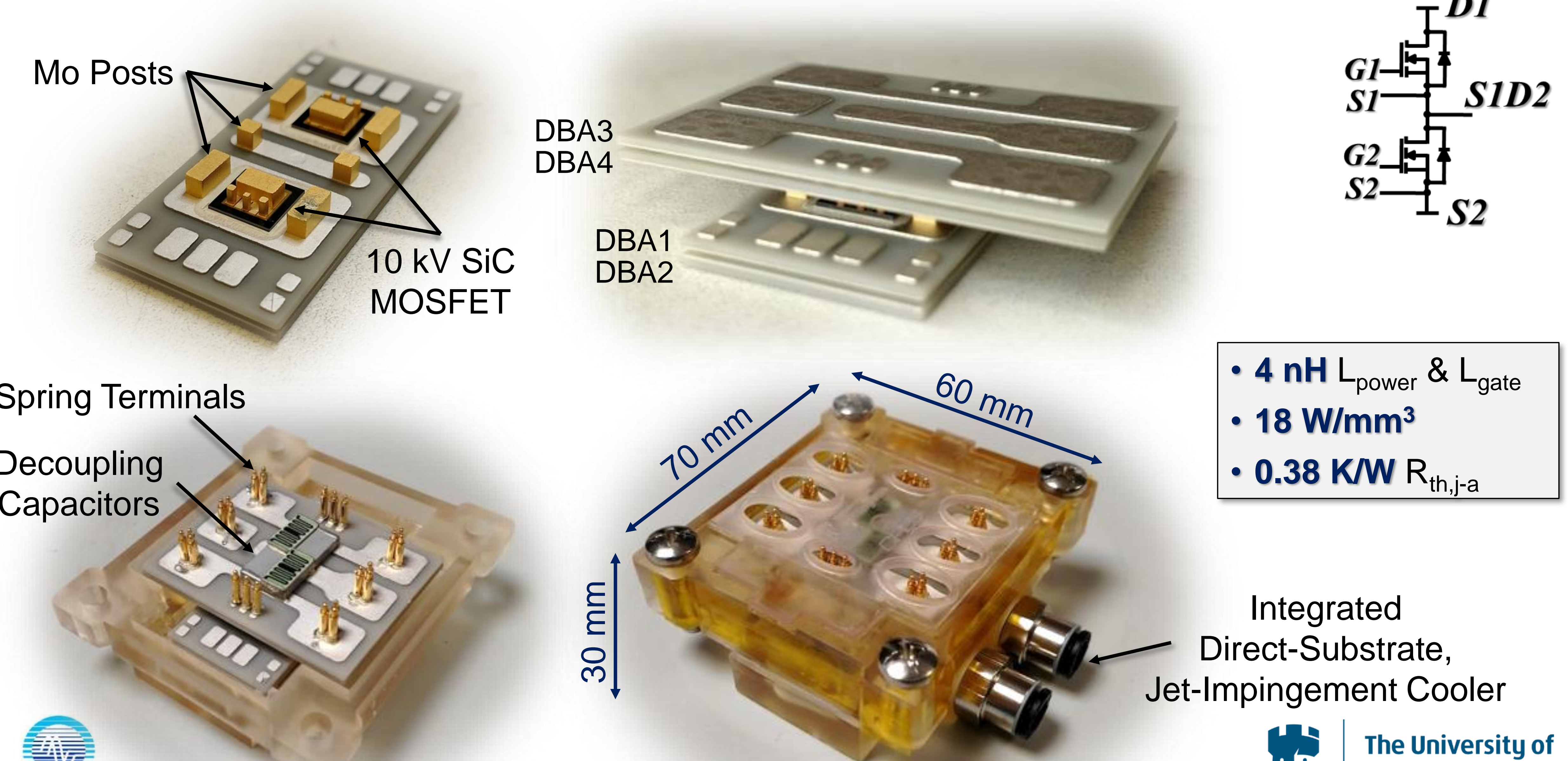
L_{gate}= 4 nH*

***for each MOSFET**

18 W/mm³ power density

➢ ***Low, symmetrical inductance and 4x higher density***

10 kV, 350 mΩ SiC MOSFET Module Prototype



- **4 nH** L_{power} & L_{gate}
- **18 W/mm³**
- **0.38 K/W** $R_{th,j\text{-}a}$

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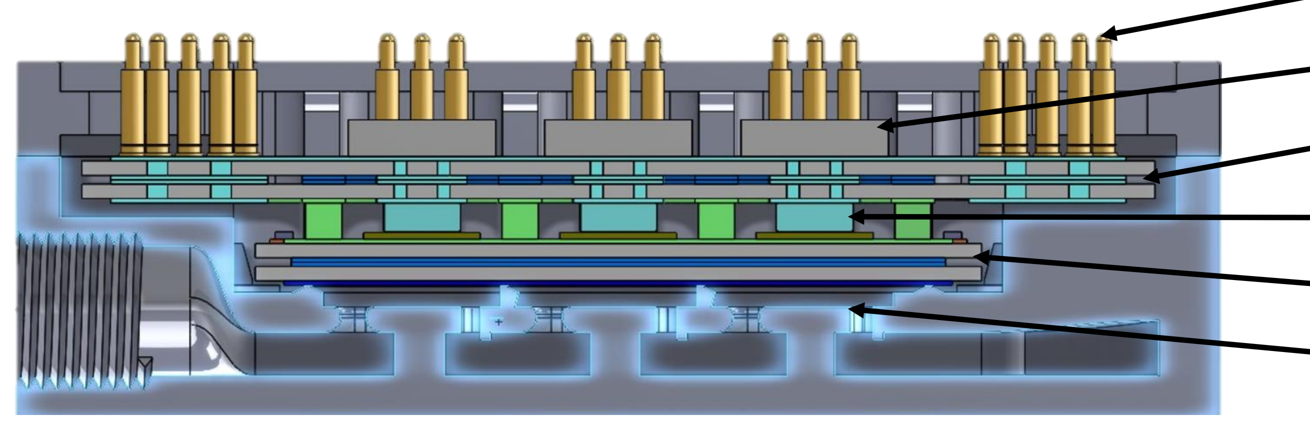
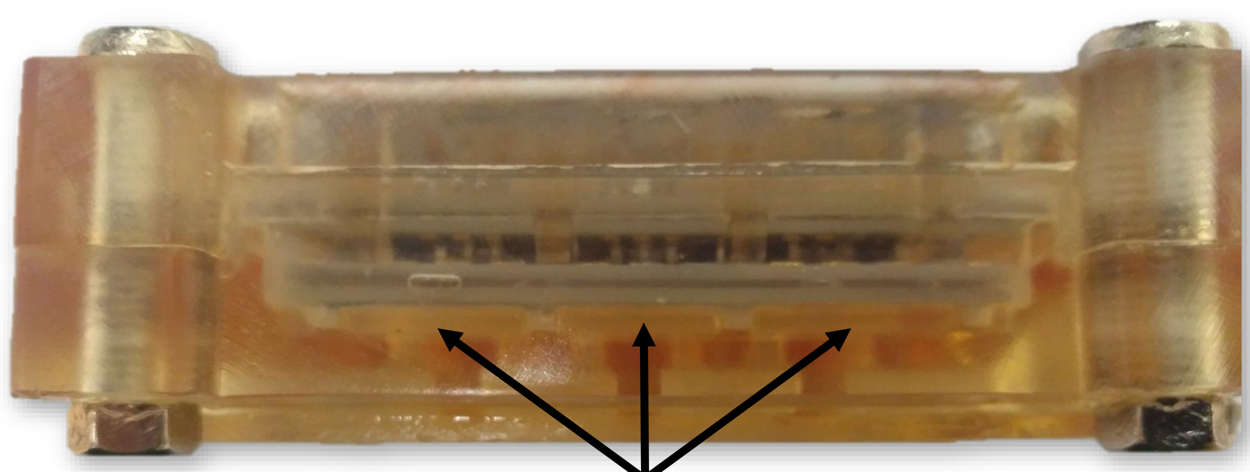
Thermal Management



Spring connectors
Decoupling capacitors
Upper stacked substrate with vias
Sintered interconnect with Mo posts
Lower stacked substrate with screen and vias
Integrated jet-impingement cooler



➢ ***0.38 K/W junction-to-ambient thermal resistance***

Double-Pulse Test Setup

Oscilloscope

20 kV Passive Probe (75 MHz)

Inductor

Decoupling Capacitors (1.2 µF, 6.6 kV)

Gate Driver

30 kV Power Supply

C_{D1} C_{D2} L V_{GS} V_{DS}

Double-Pulse Test Setup

C_{D1}

C_{D2}

L

V_{GS}

V_{DS}

20 kV Passive Probe (75 MHz)

300 V Passive Probe (1 GHz)

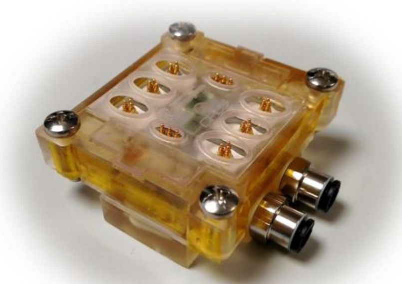
Decoupling Capacitors (1.2 μF, 6.6 kV)

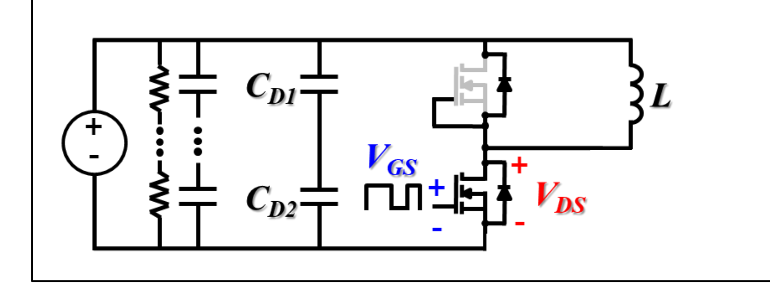
Gate Driver

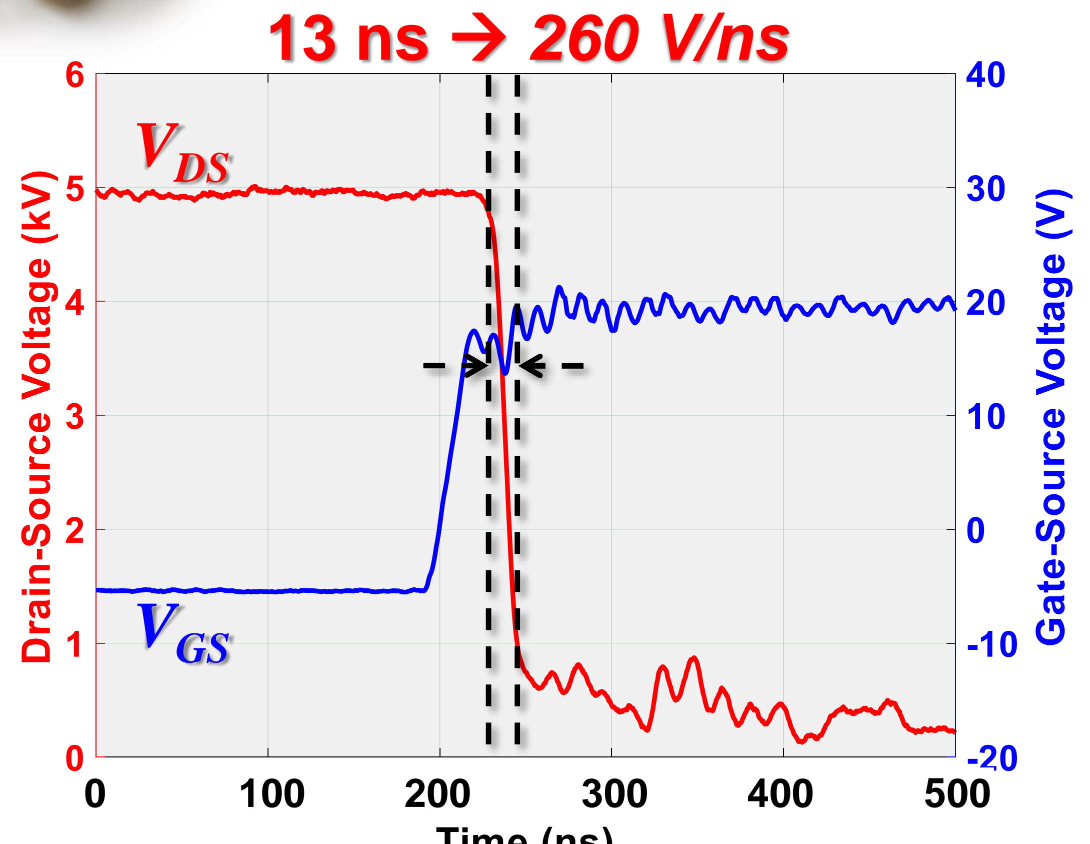
Module

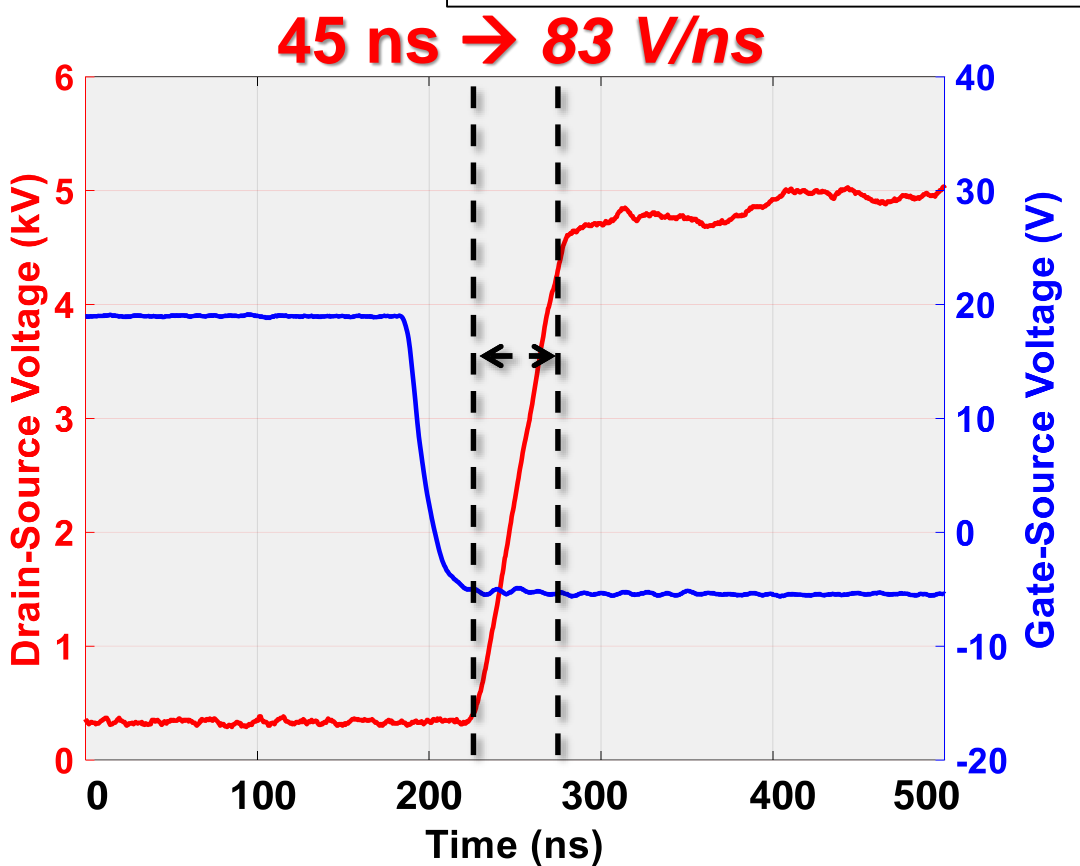
Inductor

10 kV Prototype DPT









$R_{G,ON}$= 0.33 Ω, $R_{G,OFF}$= 0.17 Ω, I_D= 20 A

➤ ***13 ns switching at 5 kV***

Embedded Common-Mode Screen

C_{D1}
C_{D2}

D1
C_{D1}
G_1
S_1
S1D2
$1/2V_{DC}$
C_{P1}
C_{D2}
G_2
S_2
C_{P2}
S2
Middle Metal Layer

$1/2V_{DC}$
S2
C_{D2}
C_{D1}
D1
C_{P1}
C_{P2}

$I = C(dv/dt)$

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Common-Mode Screen Analysis

1/2V_{DC} S2 C_{D2} C_{D1} D1 C_{P1} C_{P2}

I= C(dv/dt)

D1 C_{D1} G_1 S_1 S1D2 1/2V_{DC} C_{D2} G_2 S_2 C_{P1} C_{P2} S2

Middle Metal Layer

$$Z_{screen} \ll Z_{gnd}$$

$$Z_{screen} = \omega L_{screen} + \frac{1}{j\omega C_D} + R_s \qquad Z_{gnd} = \omega L_g + \frac{1}{j\omega C_{P2}} + R_g$$

- Low L_{screen}
- High C_D
- Low C_{P2}

$$\omega L_{screen} + \frac{1}{j\omega C_D} + R_s \ll \omega L_{gnd} + \frac{1}{j\omega C_{P2}} + R_g$$

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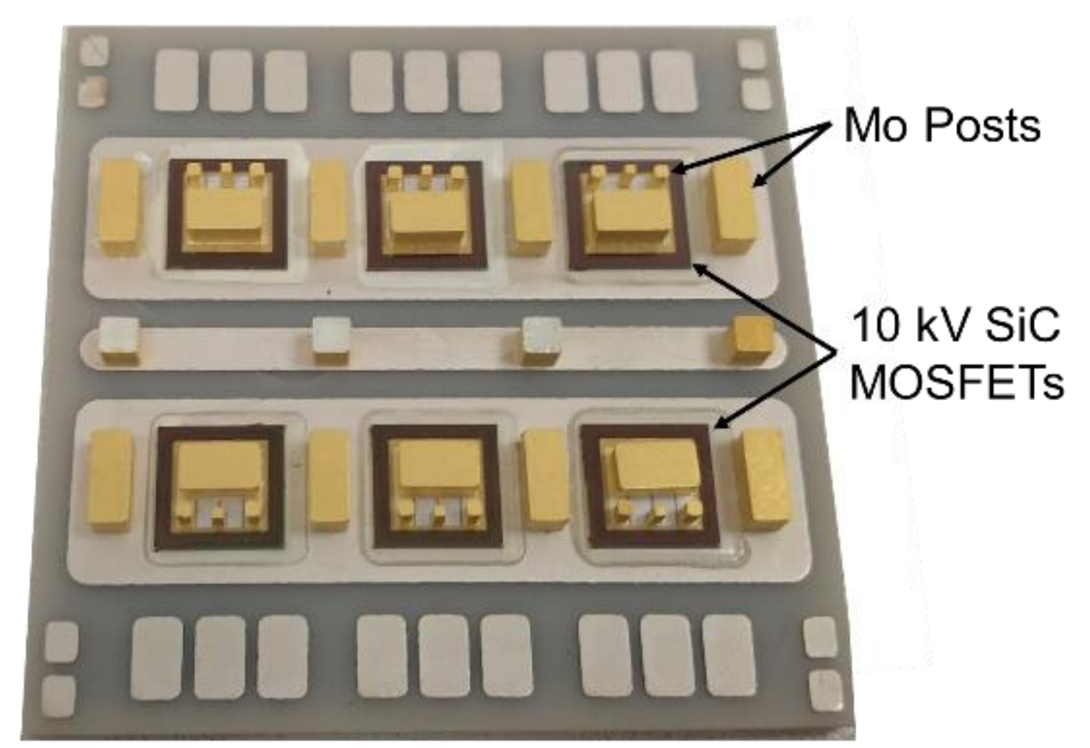
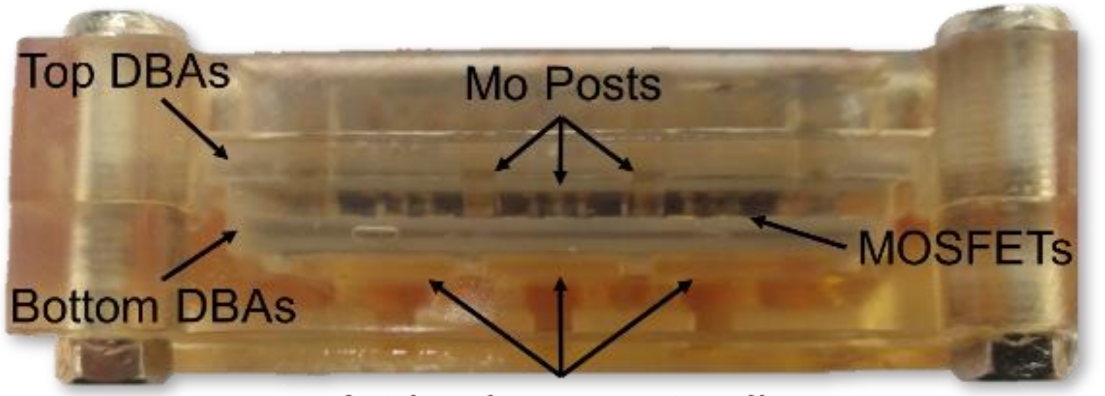
10 kV, 117 mΩ SiC MOSFET Module Prototype

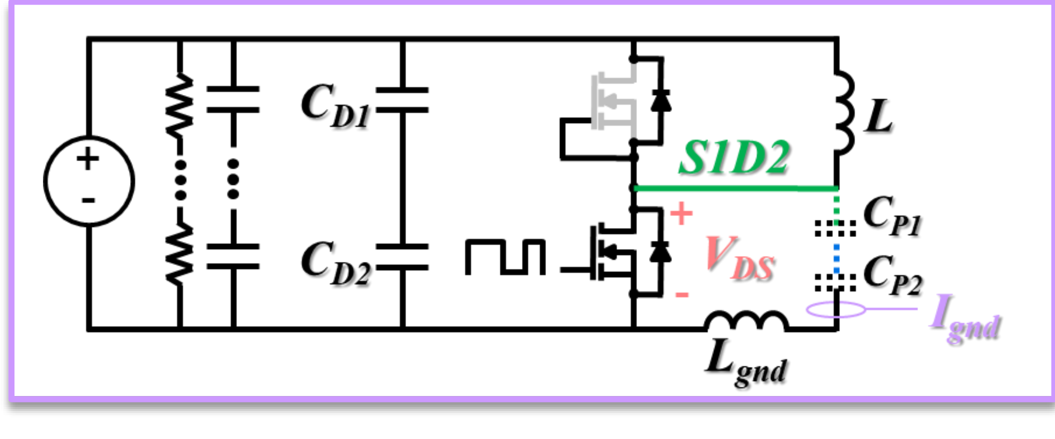


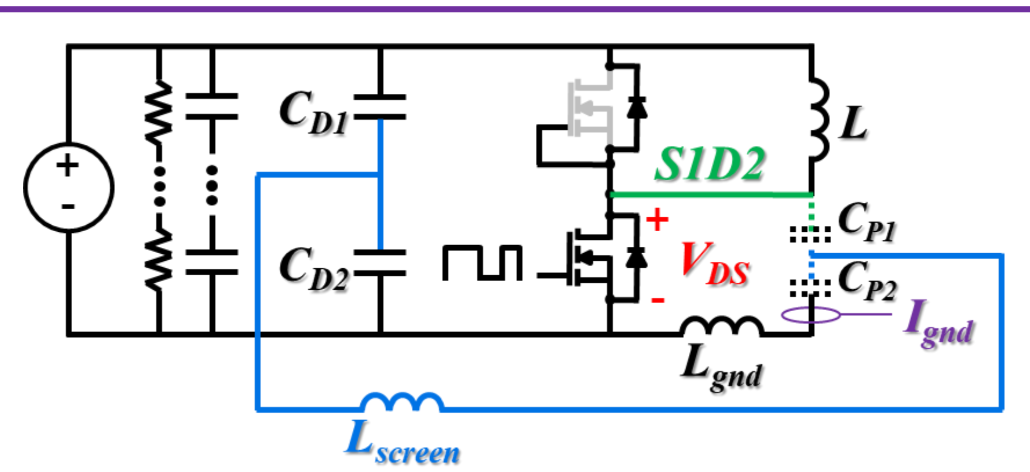


$$\omega L_{screen} + \frac{1}{j\omega C_D} + R_s \ll \omega L_{gnd} + \frac{1}{j\omega C_{P2}} + R_g$$

$L_{screen} = 2\ nH;\ C_D = 680\ pF;\ C_{P2} = 160\ pF$

Common-Mode Screen Waveforms

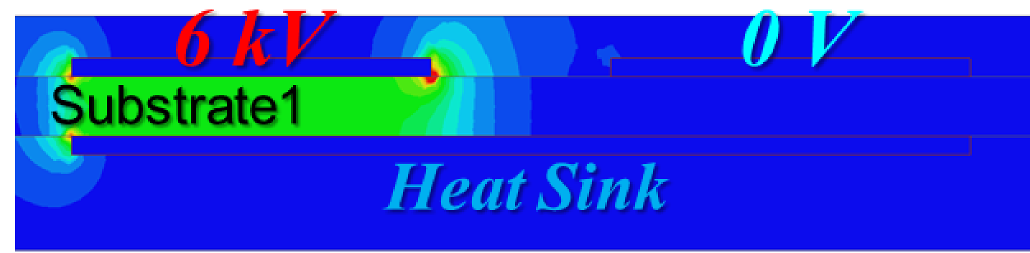


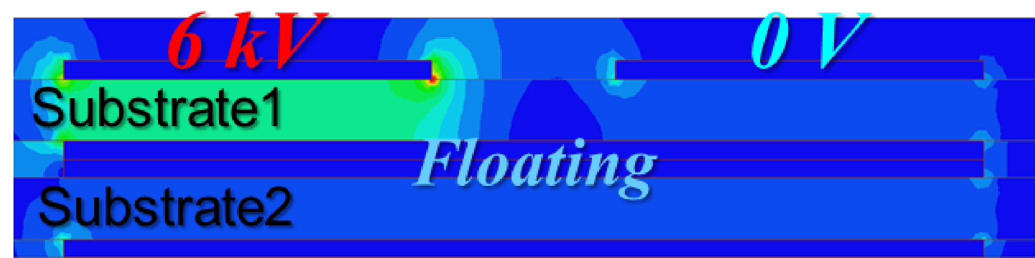


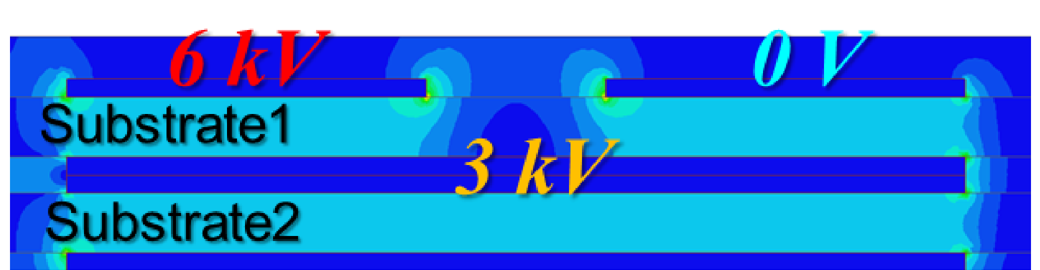
Vds
Vds_Screen
Ignd
Ignd_Screen
~2 A
~0.2 A
Drain-Source Voltage (V)
2500
2000
1500
1000
500
0
-500
Ground Current (A)
6
4
2
0
-2
-4
-6
0
0.1
0.2
0.3
0.4
0.5
Time (µs)

R_G= 0 Ω, I_D= 20 A

Electric Field Reduction







	Partial Discharge Inception Voltage (rms)	
Case	Air	Silicone Gel
Single DBA	1.7 kV	7.4 kV
Stacked DBAs (middle floating)	1.7 kV	7.6 kV
Stacked DBAs (middle at half the applied voltage)	2.6 kV	>10.5 kV

➢ ***>50 % higher partial discharge inception voltage***

Electric Field Reduction at the Module Terminals

Cu Trace

PCB

Air

Housing

Encapsulation

Ellipse

Springs

Ceramic

E [V/m]

3.0000E+006
2.8000E+006
2.6000E+006
2.4000E+006
2.2000E+006
2.0000E+006
1.8000E+006
1.6000E+006
1.4000E+006
1.2000E+006
1.0000E+006
8.0000E+005
6.0000E+005
4.0000E+005
2.0000E+005
0.0000E+000

PCB

Air

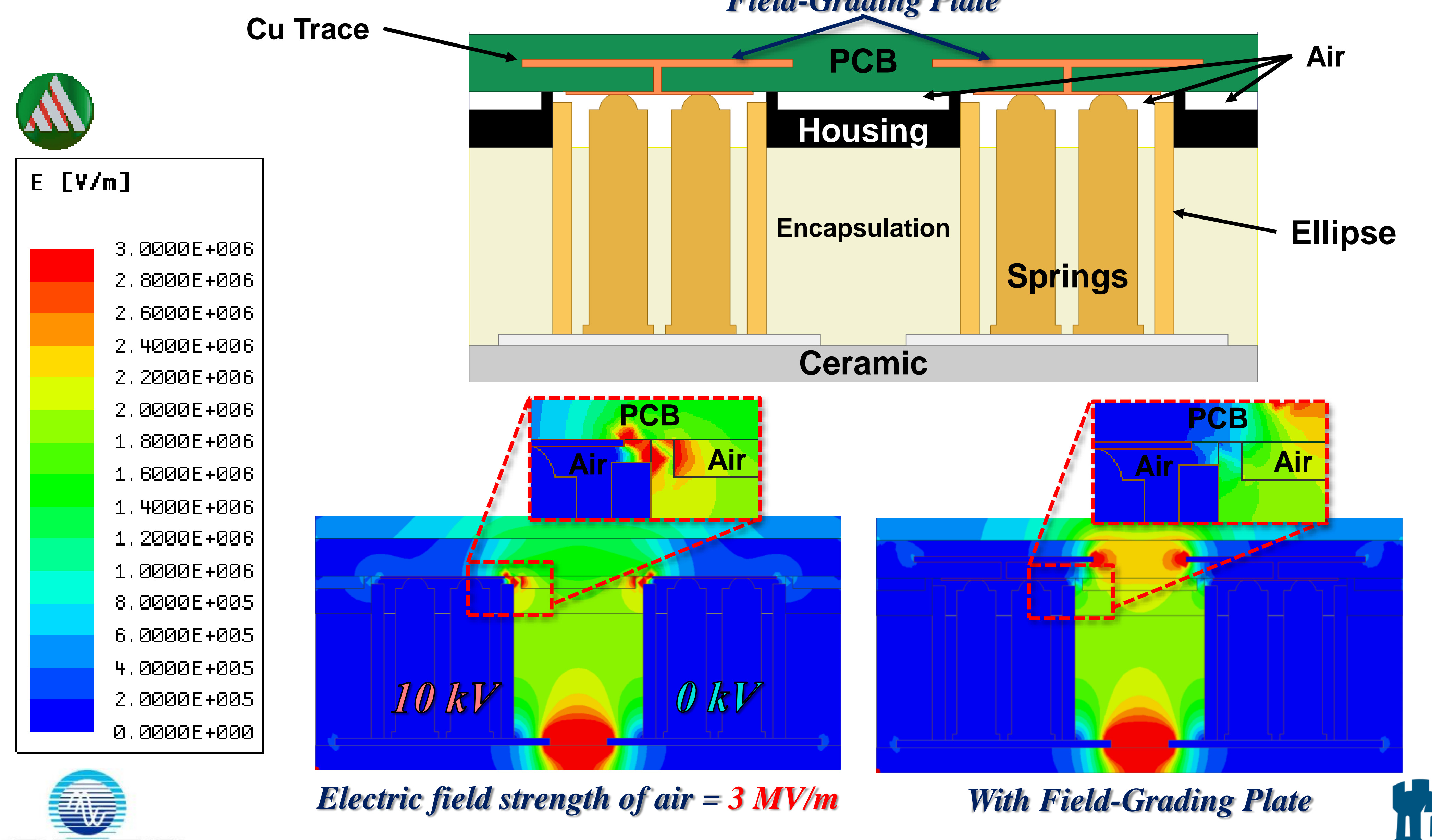
Air

10 kV

0 kV

Electric field strength of air = 3 MV/m

Electric Field Reduction at the Module Terminals



Electric field strength of air = 3 MV/m

With Field-Grading Plate

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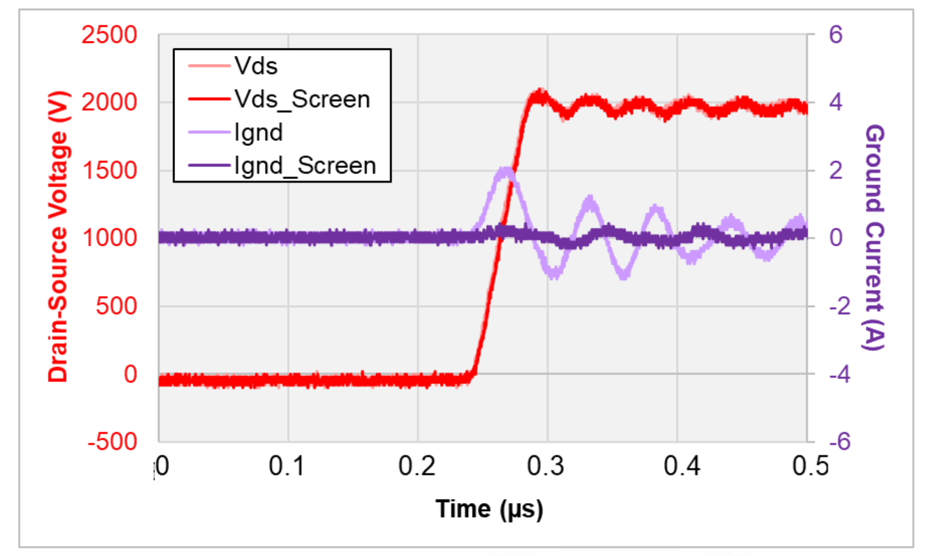
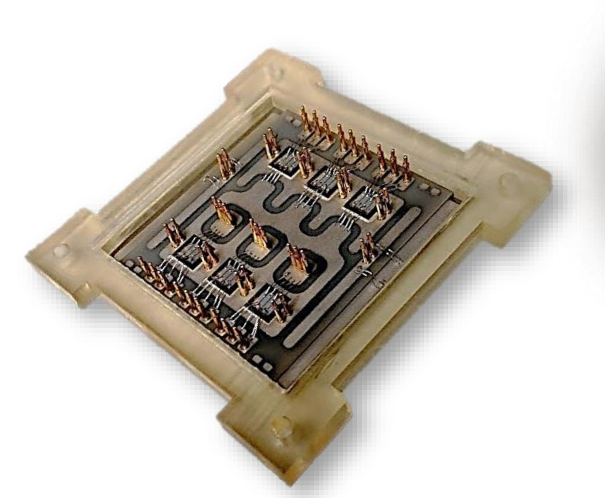
Summary and Future Work

- **Summary**
  - **4 nH** power- and gate-loop inductances
  - **18 W/mm³** power density (4 W/mm³ with cooler)
  - **0.38 K/W** (26 mm²•K/W) junction-to-ambient R_{th}
  - **13 ns** switching at 5 kV
  - **10x** reduction in common-mode current
  - **>50 %** higher partial discharge inception voltage



- **Future Work**
  - Electromagnetic interference evaluation
  - Wire bond module switching tests



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Comparison of *Multi-chip* 10 kV SiC MOSFET Modules

	10 kV, 120 A POWEREX *2011* 12 MOSFETs, 6 JBS	*10 kV, 240 A* Wolfspeed *2016* 18 MOSFETs	*10 kV, 60 A* CPES / The University of Nottingham *2017/2018* 3 MOSFETs	*10 kV, 60 A* CPES / The University of Nottingham *2017/2018* 3 MOSFETs
L_{power}	29 nH	15.8 nH	8.6 nH	4.4 nH → *4x lower* ✓
L_{gate}	3.6 nH	--	8.7 nH	3.8 nH → *2x lower* ✓
C_{hs}	370 pF	--	65 pF	45 pF → *2x lower* ✓
Power Density	0.99 W/mm³	4.2 W/mm³	7.0 W/mm³	18.1 W/mm³ → *4x higher* ✓

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