Advanced 3-Φ SiC/GaN PWM Inverter & Rectifier Systems

J.W. Kolar et al.

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

July 03, 2019

Advanced 3-Φ SiC/GaN PWM Inverter & Rectifier Systems

J.W. Kolar, J. Azurza, M. Guacci, M. Antivachis, D. Bortis

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

July 03, 2019

ETH Zurich

21 Nobel Prizes
509 Professors
5800 T&R Staff

2 Campuses
136 Labs
35% Int. Students
90 Nationalities
36 Languages

150th Anniv. in 2005

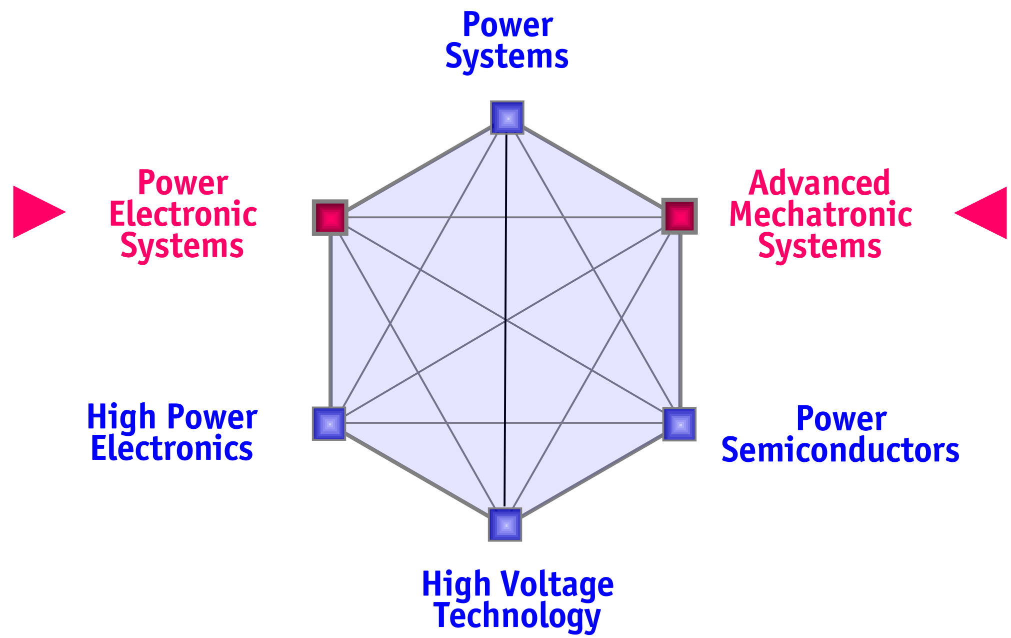
Departments

ARCH	Architecture
BAUG	Civil, Environmental and Geomatics Eng.
BIOL	Biology
BSSE	Biosystems
CHAB	Chemistry and Applied Biosciences
ERDW	Earth Sciences
GESS	Humanities, Social and Political Sciences
HEST	Health Sciences, Technology
INFK	Computer Science
ITET	Information Technology and Electrical Eng.
MATH	Mathematics
MATL	Materials Science
MAVT	Mechanical and Process Engineering
MTEC	Management, Technology and Economy
PHYS	Physics
USYS	Environmental Systems Sciences

Students ETH in total

14’500	B.Sc.+M.Sc.-Students
4’500	Doctoral Students

ITET – Research in E-Energy



Systems

Technologies

- Balance of Fundamental and Application Oriented Research

Power Electronic Systems Laboratory

Industry Relations
R. Coccia / B. Seiler

Johann W. Kolar

Adv. Mechatronic Systems
D. Bortis

AC-DC Converter	AC-AC Converter	DC-DC Converter	DC-AC Converter	Multi-Domain Modeling	Measurement Technology	Advanced Mechatronics	Magnetic Levitation
		F. Krismer	**D. Bortis**	**F. Krismer**		**D. Bortis**	**D. Bortis**
M. Heller Y. Li D. Menzi D. Neumayr	J. Azurza P. Czyz M. Haider	P. Bezerra T. Guillod G. Knabben J. Schäfer	M. Antivachis J. Böhler M. Guacci	P. Papamanolis	P. Niklaus	E. Hubmann	Th. Holenstein P. Püntener S. Miric

Secretariat
M. Kohn / Y. Schnyder

Administration
P. Maurantonio

Computer Systems
M. Eisenstat

Electronics Laboratory
P. Seitz

20 Ph.D. Students
2 Sen. Researchers

ECPE Competence Centre

EPSMA

Leading Univ. in Europe

Outline

- Introduction
- SiC/GaN VSD Application Challenges
- Adv. PWM Inverter Topologies
- Adv. PWM Rectifier Topologies
- Conclusions

Acknowledgement: T. Guillod, F. Krismer, D. Menzi, J. Miniböck, P. Niklaus

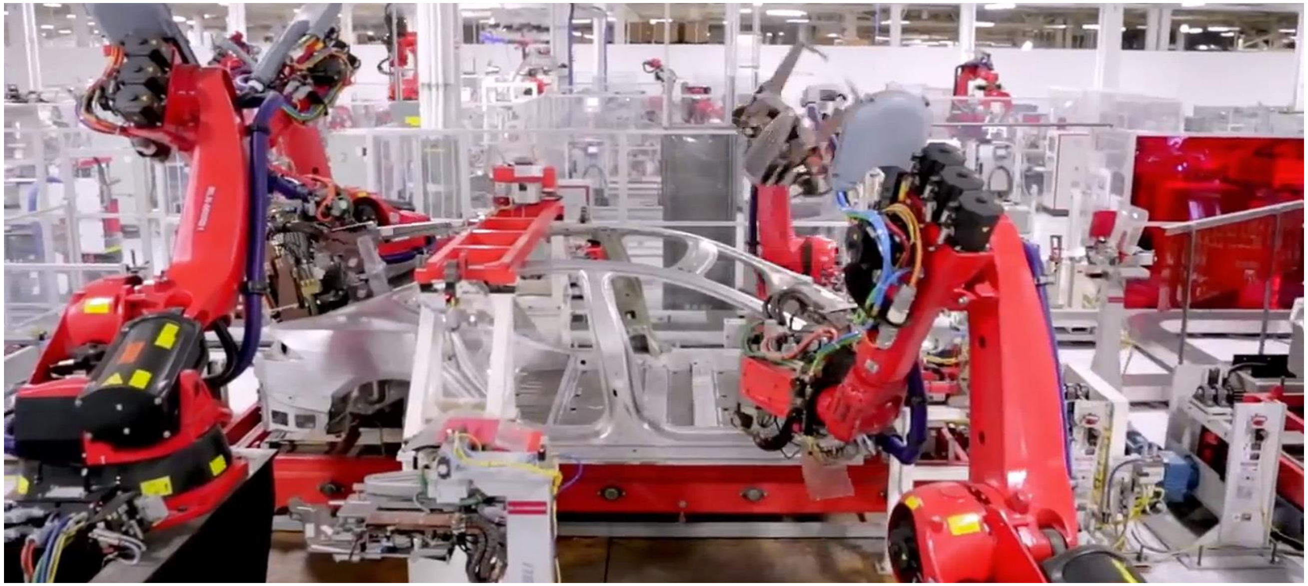
3-Φ Variable Speed Drive Inverter Systems

State-of-the-Art
Future Requirements

Applications of Drive Systems

- Industry Automation / Robotics
- Material Machining / Processing – Drilling, Milling, etc.
- Pumps / Fans / Compressors
- Transportation
- etc., etc. .... Everywhere !

Source: TESLA MOTORS

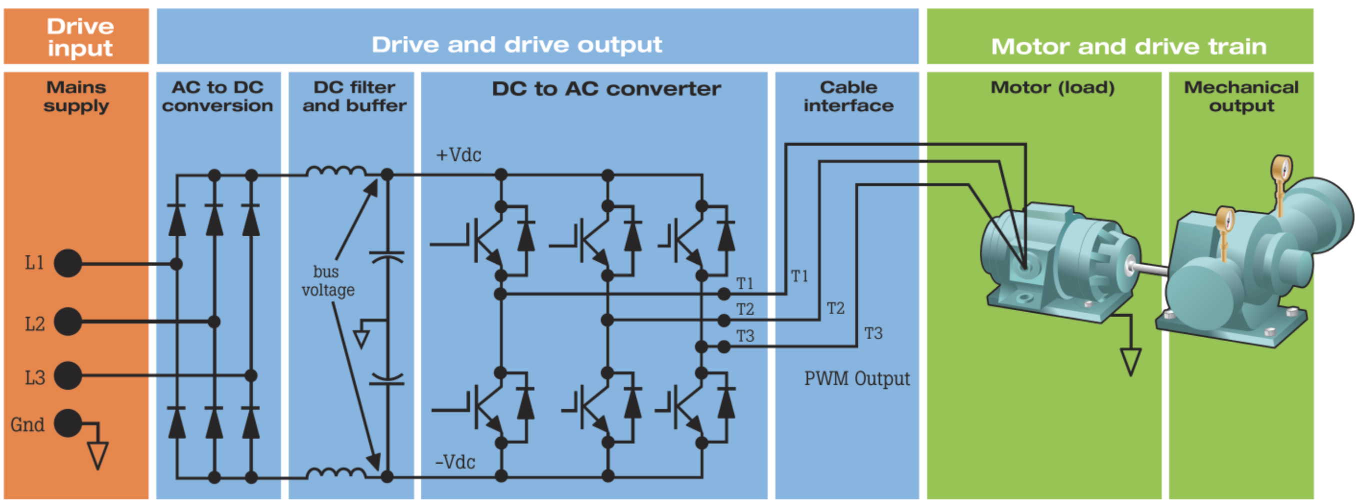


- *60% of El. Energy Used in Industry Consumed by VSDs*

▶ VSD State-of-the-Art

- Mains Interface / 3-Φ PWM Inverter / Motor — All Separated
  - → Large Installation Space / $$$
  - → Complicated / Expert Installation / $$$
- Conducted EMI / Radiated EMI / Bearing Currents / Reflections on Long Motor Cables
  - → Shielded Motor Cables / $$$
  - → Inverter Output Filters (Add. Vol.) / $$$

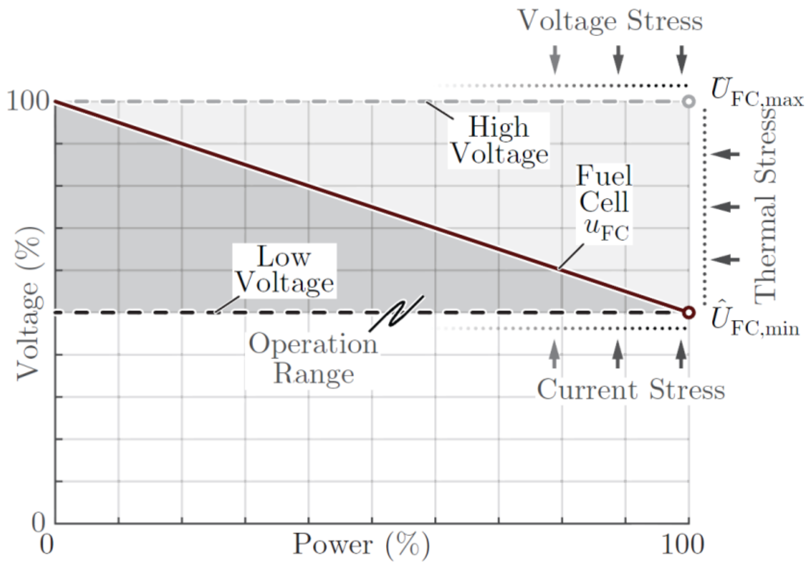
Source: FLUKE



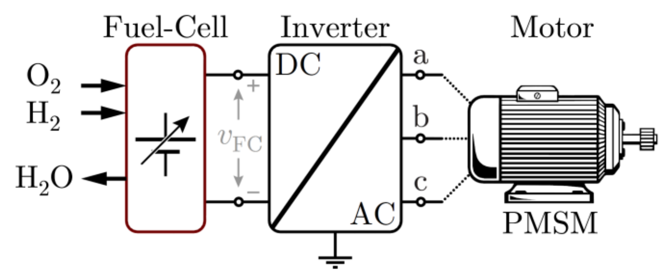
- High Performance @ High Level of Complexity / High Costs (!)

▶ Future Requirements (1)

- "Non-Expert" Install. / Low-Cost Motors → "Sinus-Inverter"
- Wide Applicability / Wide Voltage & Speed Range → Matching of Supply & Motor Voltage
- High Availability



Source: magazine.fev.com

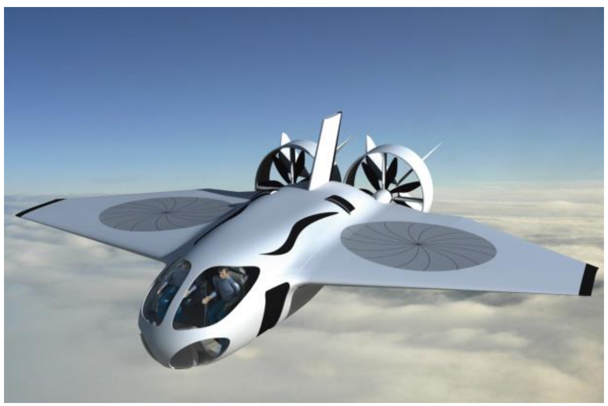


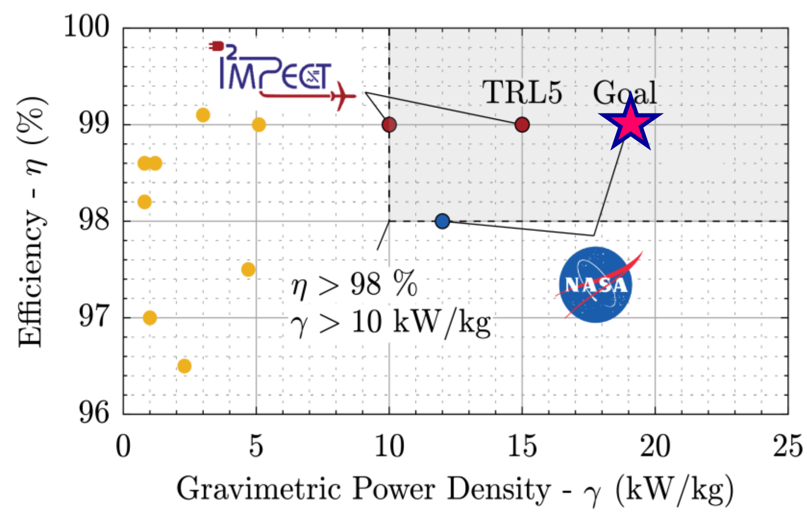
- Single-Stage Energy Conversion → No Add. Converter for Voltage Adaption

▶ Future Requirements (2)

- *Red. Inverter Volume / Weight* → *Matching of Low High-Speed Motor Volume*
- *Lower Cooling Requirement* → *Low Inverter Losses & HF Motor Losses*
- *High Speed Machines* → *High Output Frequency Range*

Source: Georgia Tech





→ *Main "Enablers" — SiC/GaN Power Semiconductors & Adv. Inverter Topologies*

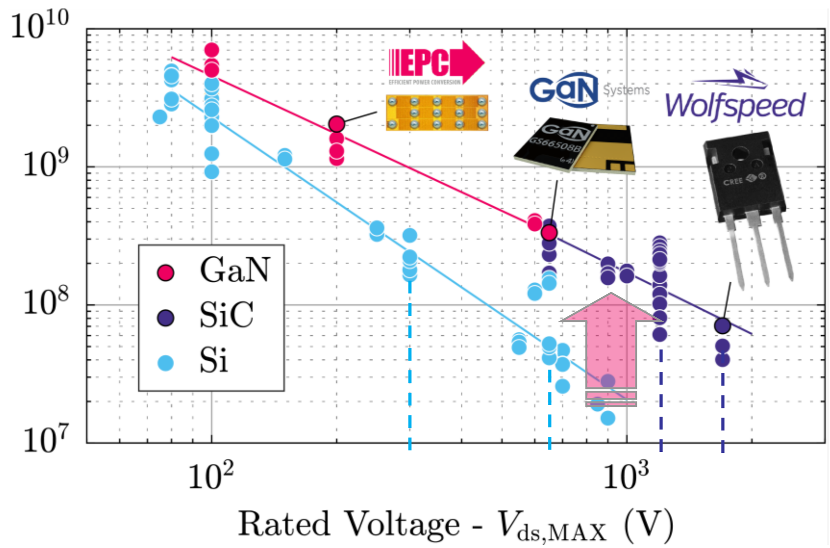
Enabling Technologies & Challenges

WBG Semiconductors
Advanced Inverter Topologies

▶ SiC/GaN

- *Very Low On-State Resistance* → *Low (Partial Load) Conduction Losses*
- *Very Low Switching Losses* → *High Switching Frequencies*
- *Small Chip Area* → *Compact Realization*

$$\mathrm{FOM} = \frac{1}{R_{\mathrm{ds,on}} Q_{\mathrm{oss}}}$$



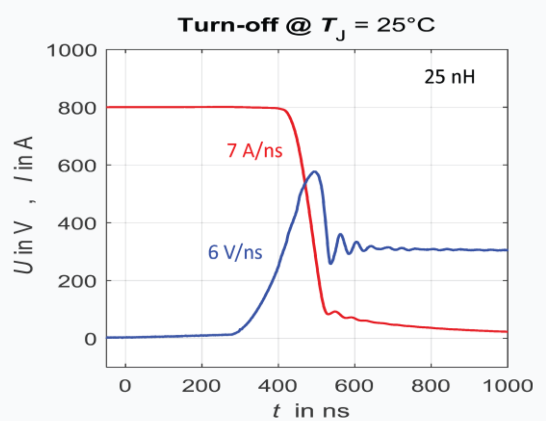
→ *Challenges in Packaging / Thermal Management / Gate Drive / PCB Layout*
→ *Extremely High Sw. Speed (dv/dt)* → *Motor Isol. Stress / Reflections / Bearing Curr. / EMI*

▶ Si vs. SiC

- **Si-IGBT** → dv/dt = 2...6 kV/us (Inverter for Var. Speed Drives / IEC 61800-3)
- **SiC** → dv/dt = 20...60 kV/us

Source: M. Bakran / ECPE 2019

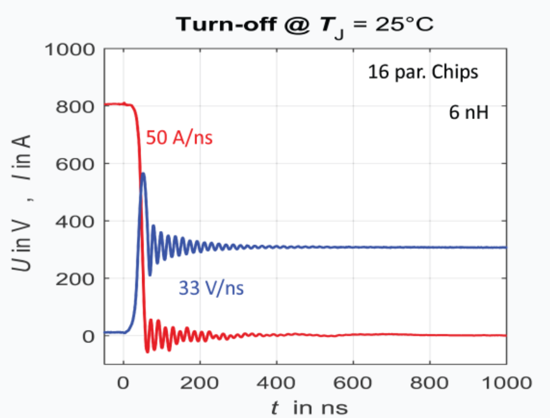
Si-IGBT / Hybrid-Pack 2



E_{off} = 45900 µJ

-> 8 kV/µs at 400V

SiC-MOSFET / (scaled for low inductance)



E_{off} = 4672 µJ

-> 44 kV/µs at 400 V

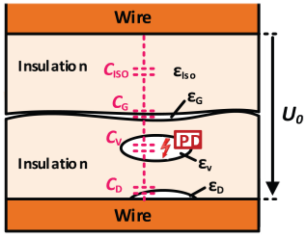
→ Extremely High dv/dt → Motor Isol. Stress / Reflections / Bearing Curr. / EMI

dv/dt - Challenges

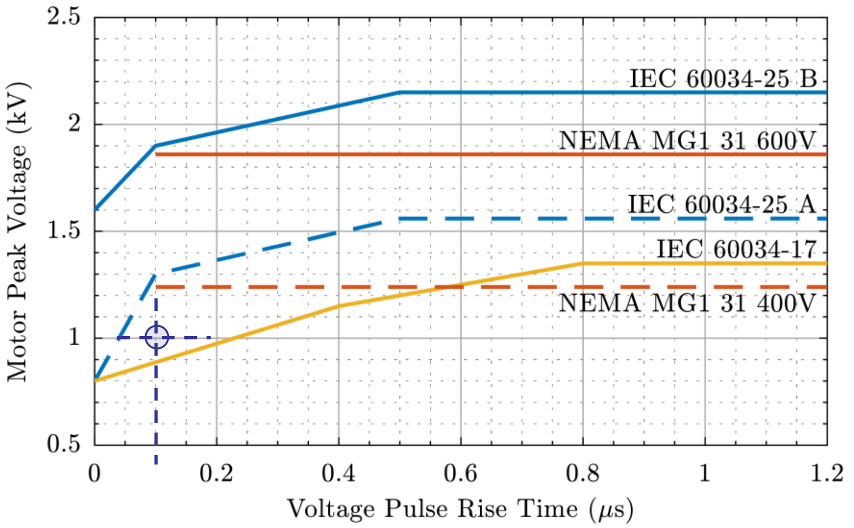
▶ Motor Insulation Destruction

- *Partial Discharge Due to Insul. Imperfections (Ionisation & Transient Space Charge Distrib.)*
- *Partial Discharge Inception Voltage (PDIV) Dependent on dv/dt*

Basic design of a wire insulation



Source: Bakran / ECPE 2019

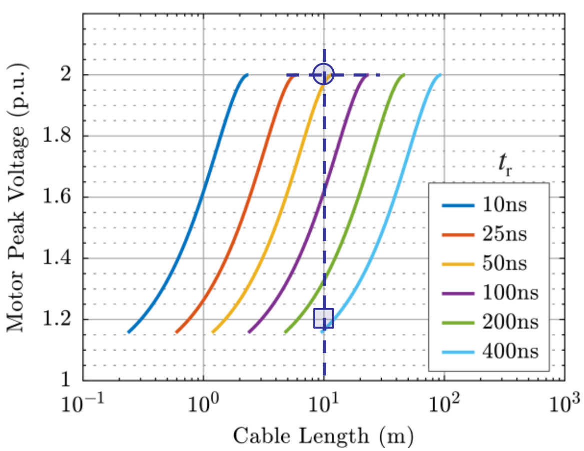


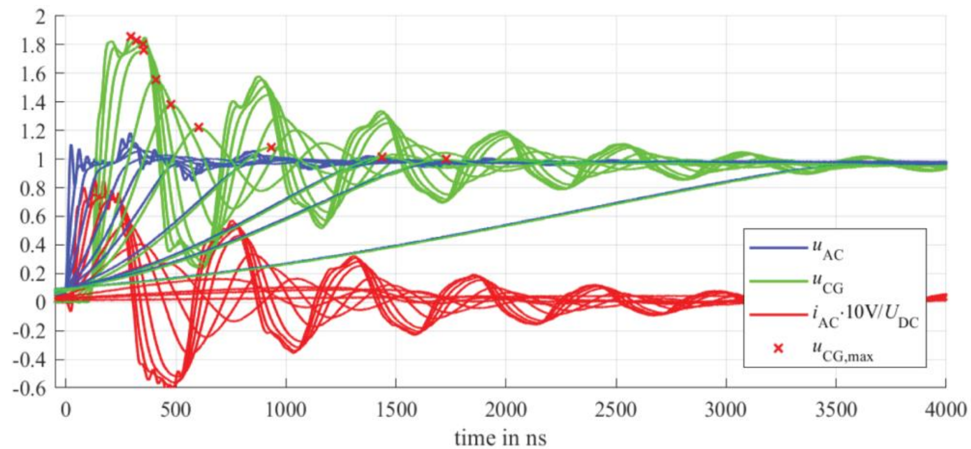
→ *dv/dt-Limits Specified by Standards*
→ *dv/dt-Filtering or Full Sinewave Filtering*

▶ *Surge Voltage Reflections*

- *Short Rise Time of Inv. Output Voltage*
- *Impedance Mismatch of Cable & Motor* → *Reflect. @ Motor Terminals / High Insul. Stress*
- *Long Motor Cable $l_c \geq \frac{1}{2}\, t_r v$*

Source: Bakran / ECPE 2019

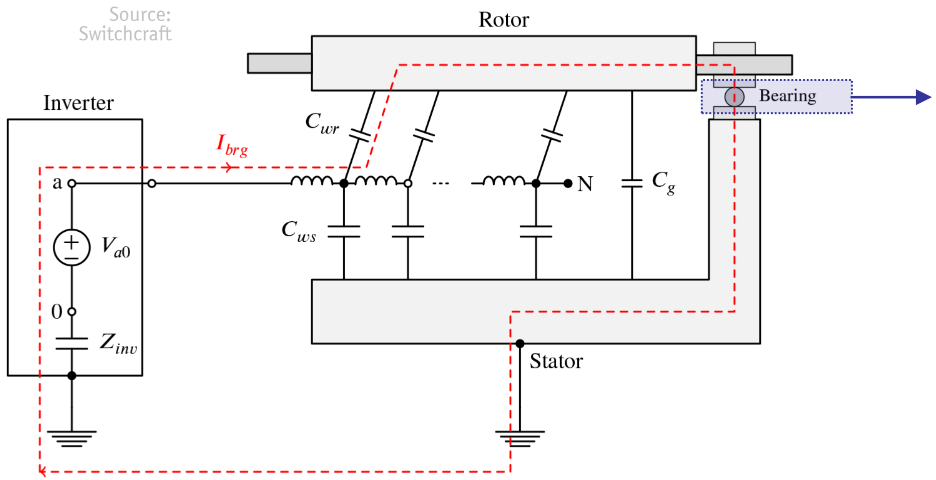


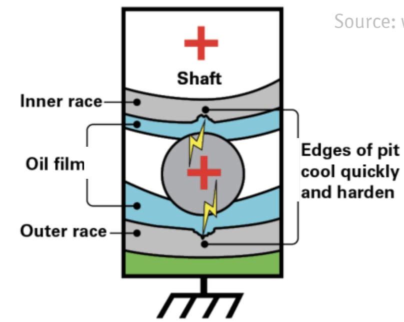


→ *dv/dt-Filtering or Full Sinewave Filtering / Termination & Matching Networks etc.*

▶ Motor Bearing Currents

- Switching Frequency CM Inverter Output Voltage → Motor Shaft Voltage
- Electrical Discharge in Bearing ("EDM")





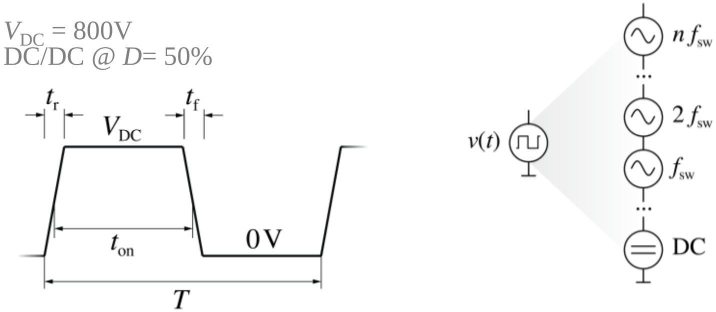
→ Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt- OR Sine Wave Filters

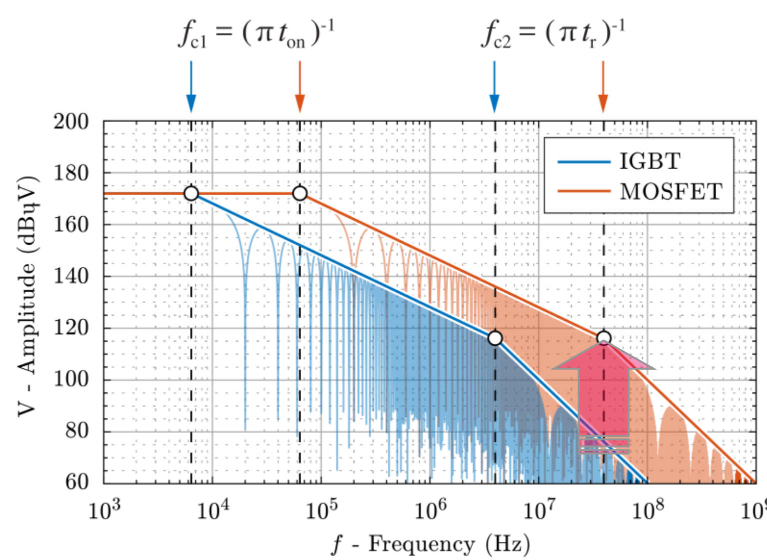
▶ SiC vs. Si Inverter EMI Spectrum

- *SiC Enables Higher dv/dt* → *Factor 10*
- *SiC Enables Higher Switching Frequencies* → *Factor 10*
- *EMI Envelope Shifted to Higher Frequencies*

Source/Idea: M. Schutten / GE

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)



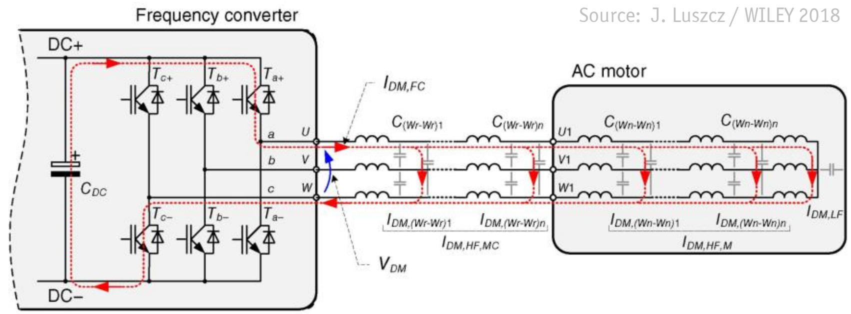


→ *Higher Influence of Filter Component Parasitics and Couplings*
→ *dv/dt-Filtering or Full Sinewave Filtering, Shielded Motor Cables*

▶ DM & CM Conducted / Radiated EMI

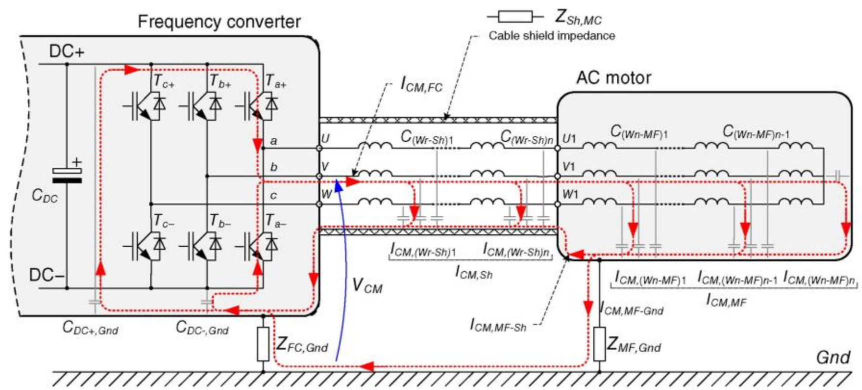
- *DM Conducted EMI Pathway*

Source: J. Luszcz / WILEY 2018



- *CM Conducted EMI Pathway (Motor Side)*

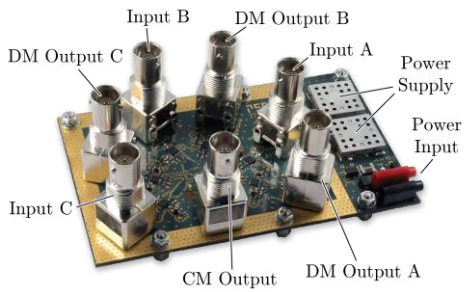
Source: J. Luszcz / WILEY 2018

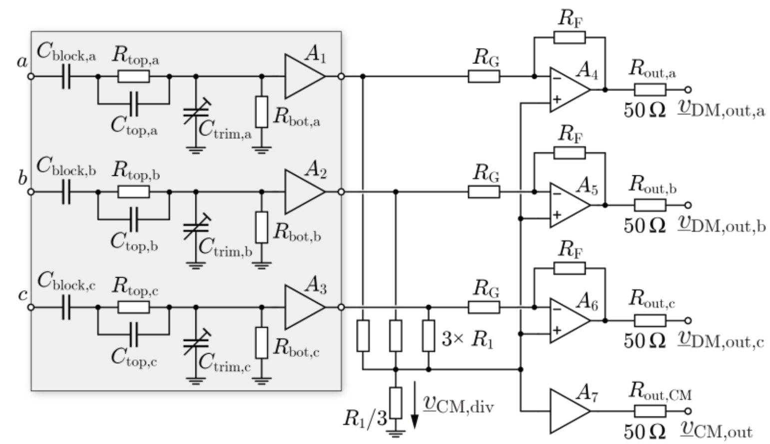


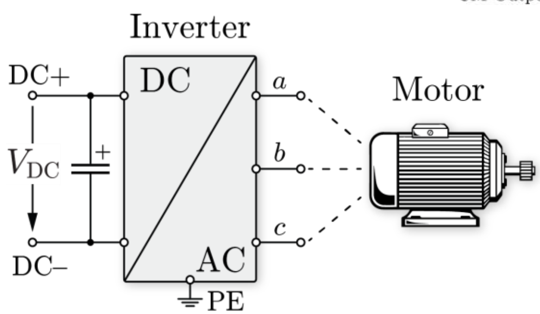
- *EMI Standards (Cond. & Rad.) → Shielded Motor Cables OR Full Sinewave Filtering*

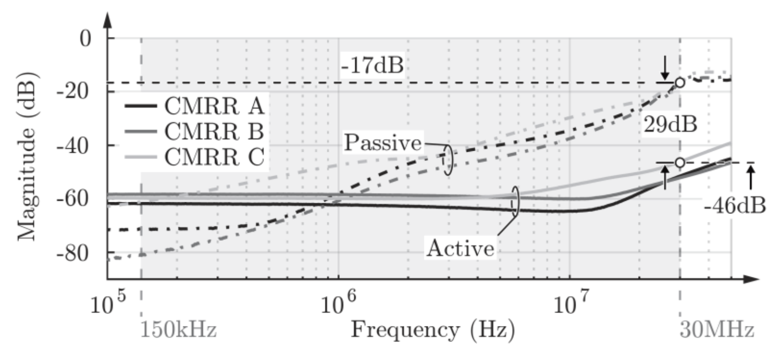
▶ 3-Φ DM/CM EMI Measurement & Separation

- ***EMI Measurement @ Inverter Output***
- ***DM/CM Splitting for Specific Filter Design***









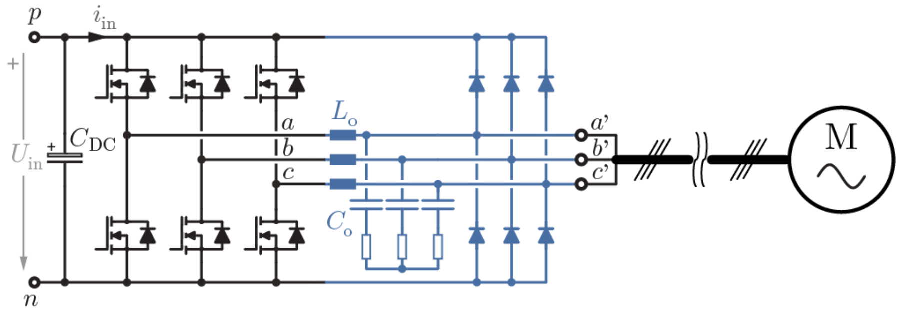
- ***Cap. Coupled Interface Circuit as Replacement for LISN (Var. Output Frequ.)***

Inverter Output Filters

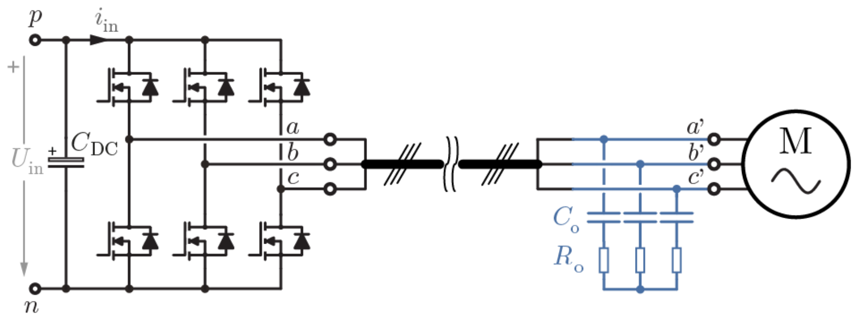
dv/dt-Filters
Motor Cable Termination
Staggered Switching
Active CM Filtering

▶ Passive dv/dt-Filter & Cable Termination

- $f_C > f_S$ → Reduction of High dv/dt of Inverter Output Voltage to 3...5kV/us



- Termination of Cable with Characteristic Impedance & Damping (No dv/dt-Limit)

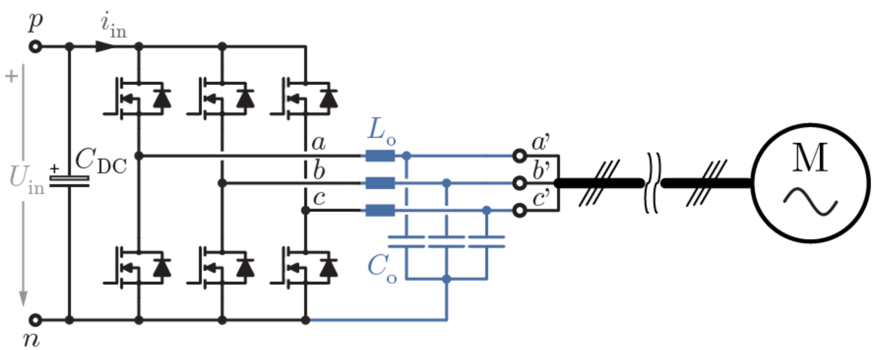


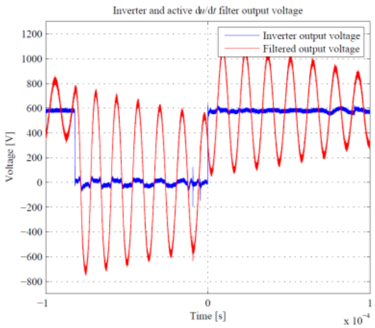
- Limited Applicability @ High Output / Sw. Frequencies (Losses) → Full Sinewave Filter

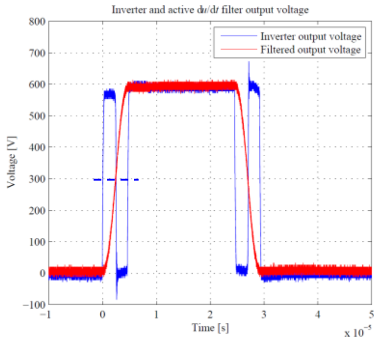
▶ Active dv/dt-Filtering

- Active Control of the dv/dt-Filter Transient Behavior → 2-Step Transition
- Influence of Motor Current → Adaption of Sw. Scheme
- DC- Connection Optional

Source: PhD Thesis, J.P. Ström
Lappeenranta Univ., 2009 / VACON



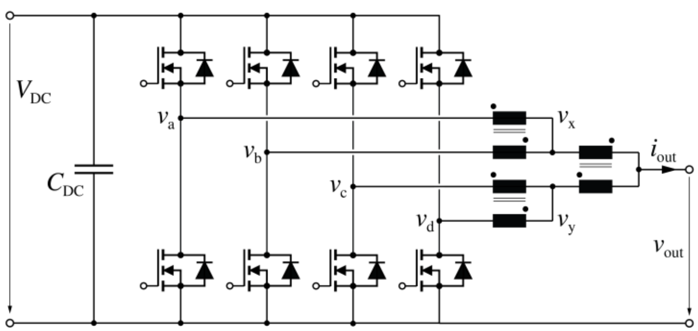


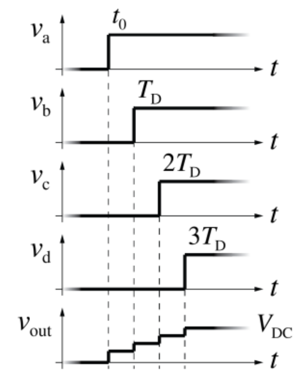


- *Ideally No Damping Resistors*
- *Increase of Sw. Losses → Low Sw. Frequ. OR High Sw. Speed Semiconductors*

► Staggered/Resonant Switching

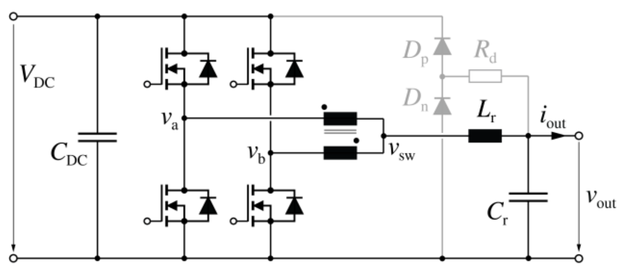
■ *Staggered Sw. Parallel Bridge Legs → Non-Resonant Multi-Step Transistion*

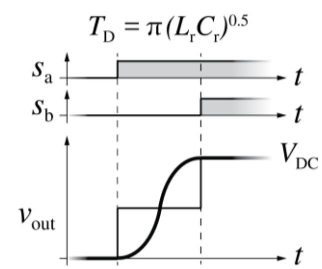




Source: J. Ertl et al. PCIM Europe 2017

■ *2-Step Switching / Resonant Transition (cf. Active dv/dt-Filter)*





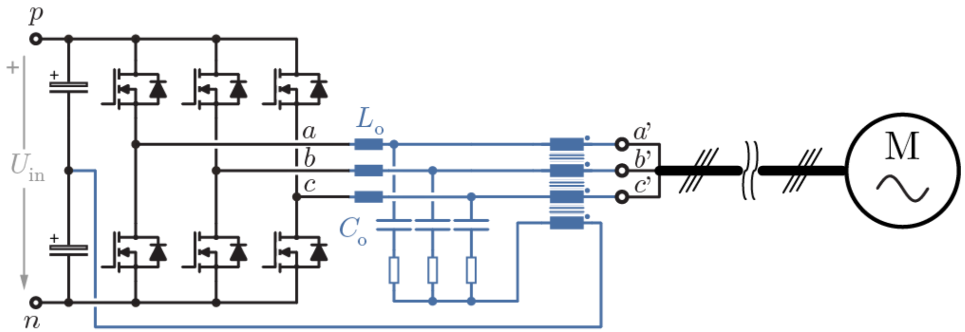
Source: J. Ertl et al. PCIM Europe 2018

● *Adv. for High Power / Output Curr. Syst. Employing Parallel Bridge Legs & Local Comm. Cap.*

Active CM Voltage Filters

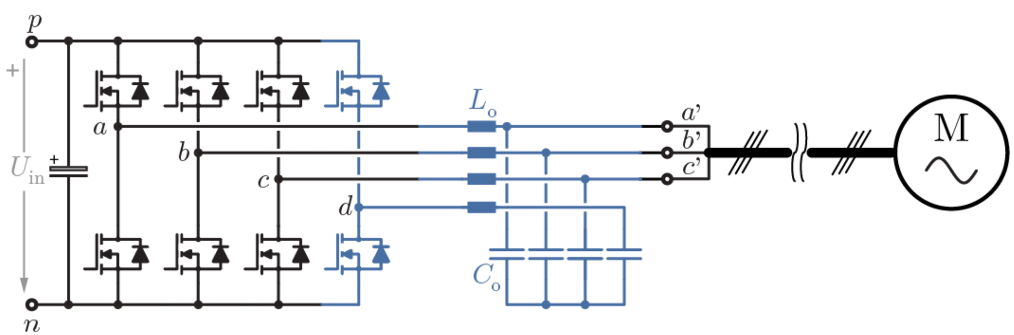
- *Series Compensation of CM Voltage & DM dv/dt-Filtering*

Source: X. Chen et al., 2007



- *Aux. Bridge Leg → Zero CM Voltage for Active Inv. Sw. States & DM dv/dt-Filtering*

Source: T.A. Lipo et al., 1999



- *Residual CM Voltage Due to Transf. & Sw. Imperfections / Complexity & Missing Zero State*

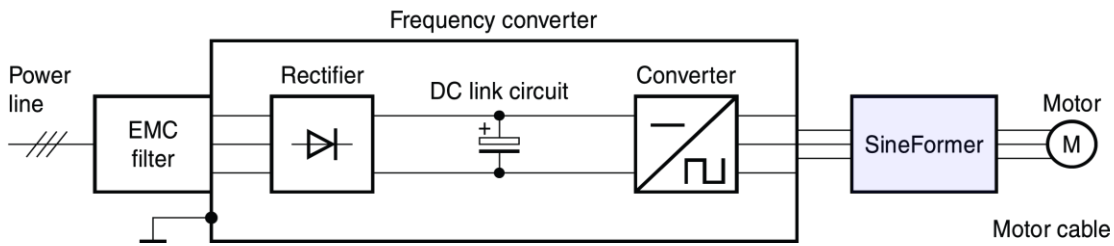
Inverter Output Filters

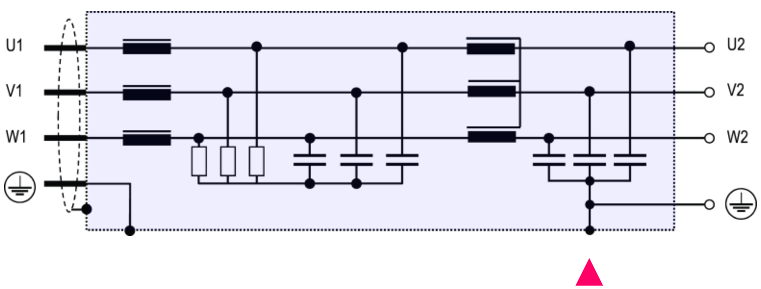
Sinewave Filters

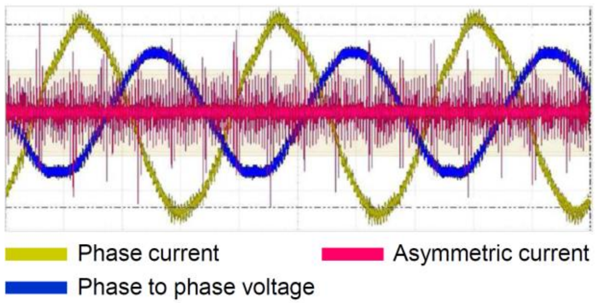
► "SineFormer" Output Filter

- $f_C << f_S$ DM and CM (!) Output Filter Stage → Sin. Output Voltage / No Sw. Frequ. CM Voltage
- No Shielded Motor Cables Required
- Reduction of Mains-Side EMI

Source: TDK



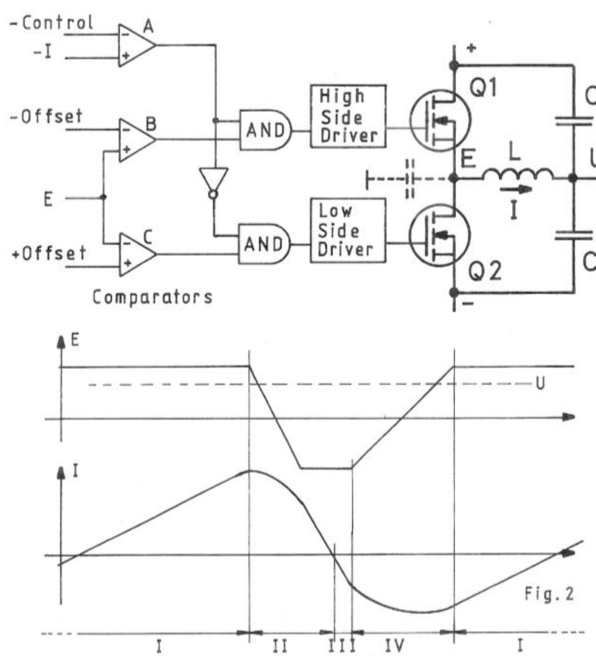




- Large Weight & Volume → ≈2 kVA/dm³ (f_S= 4...8 kHz, f_0= 0...100 Hz)
- Filter Cap. Starpoint Connected to PE Not DC- (Allows Retrofitting)

► Full Sinewave Filtering @ ZVS/TCM Operation

- *ZVS of Inverter Bridge Legs (No Use of the Intrinsic Diodes of Si MOSFETs)*
- *High Sw. Frequency & TCM → Low Filter Inductor Volume*

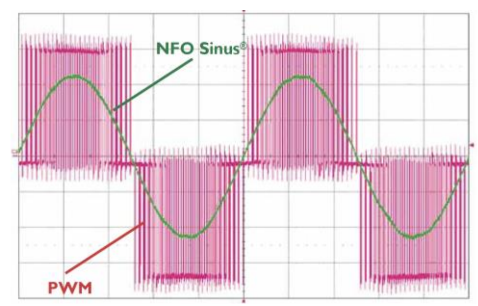


Source: Joensson

PCIM'88
(POWER CONVERSION)
CONFERENCE
DECEMBER 8-10, 1988
TOKYO, JAPAN

Source: NFO Sinus

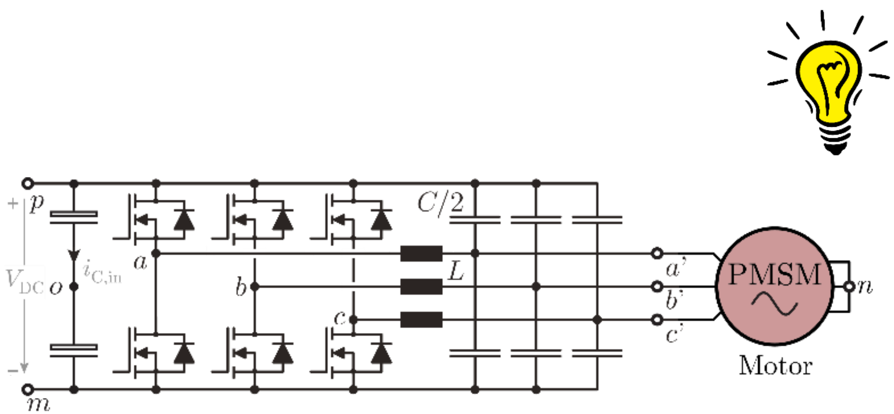
NFO Sinus® is available in size 0,37 kW up to 22 kW

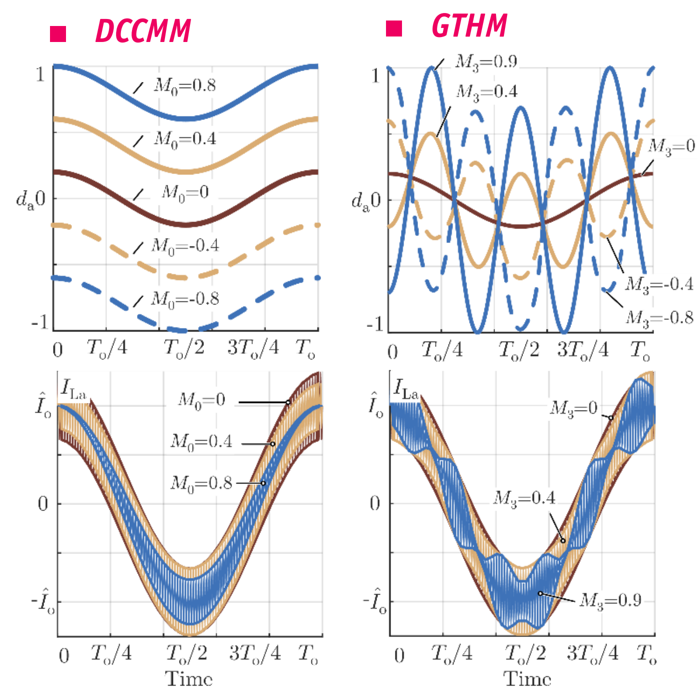


- *Widely Varying Switching Frequency → Voltage Headroom and/or Multiple Bridge-Legs*
- *Rel. High Current Stress on the Power Transistors*

▶ Full Sinewave Filtering @ CCM Operation (1)

- DC- Ref. LC-Filter → Max. Ind. Current Ripple @ d=0.5
- DCCMM — Max. DC-Offset M_0 Shifting Phase Voltages Towards d=0 OR d=1
- GTHM — Max. 3rd Harm. M_3 for Red. of Sw. Frequ. Harmonic Power

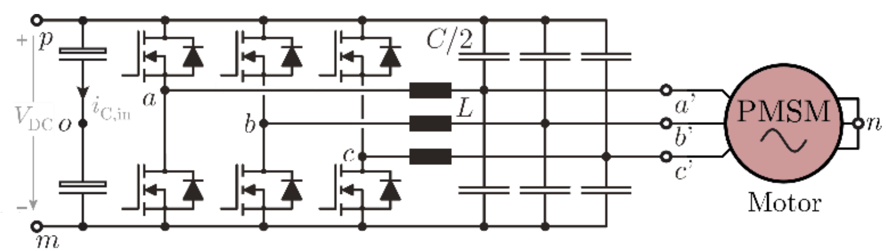


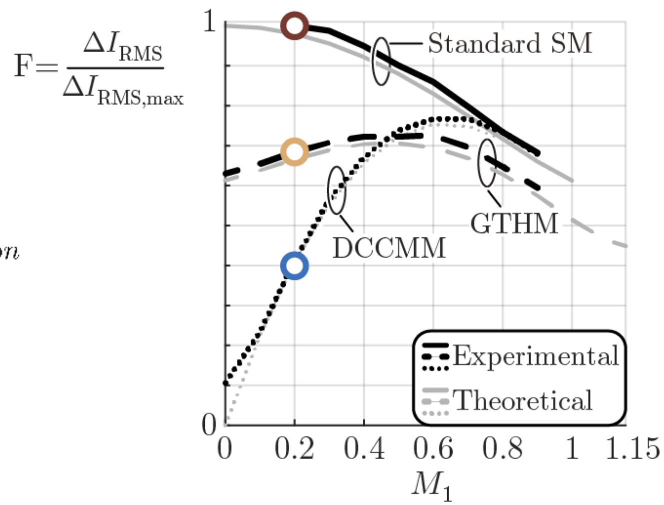


- GTHM — Results in Add. Cap. Reactive Power → Limited for Higher Frequencies

▶ Full Sinewave Filtering @ CCM Operation (2)

- *Massive Red. of Current Ripple @ Lower Modulation Index*
- *DCCMM — Adv. for M = 0...0.5*
- *GTHM — Adv. for M = 0.5...1.0*





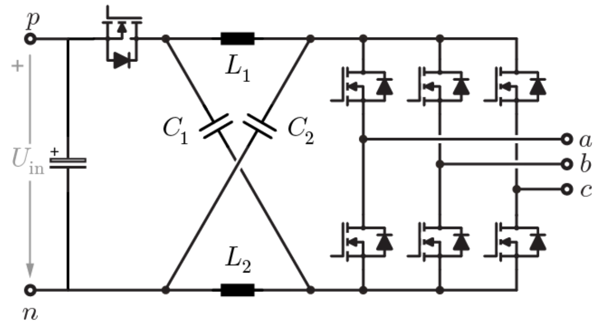
- *GTHM — Results in Add. Cap. Reactive Power → Limited for Higher Frequencies*

Buck+Boost Inverter

Z-Source Inverter etc.
VSI & DC/DC Front-End
Double-Bridge VSI
Phase-Modular Buck+Boost Inverter
CSI & DC/DC Front-End

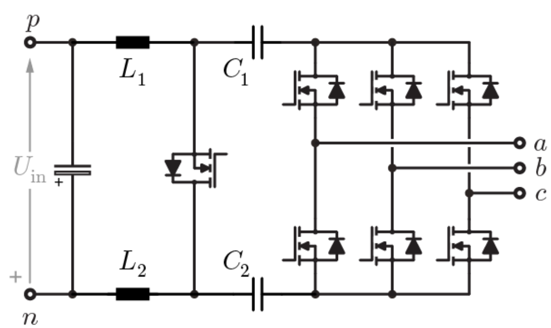
► "Outside-the-Box" Topologies

- *Z-Source Inverter → Shoot-Through States Utilized for Boost Function*
- *Higher Component Stress Eff. Limits Boost Operation to ≈120% U_{in}*



Source: F.Z. Peng / 2003
J. Rabkowski / 2007

- *3-Φ Back-End DC/AC Cuk-Converter*

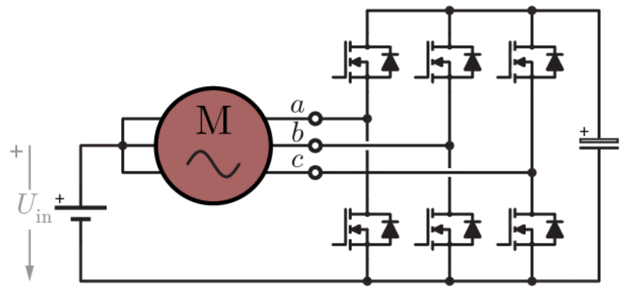


Source: T.A. Lipo et al. /2002 & K.D.T Ngo / 1984

- *Integration Typ. Results in Higher Comp. Stresses & Complexity / Lower Performance*

▶ Boost Converter DC-Link Voltage Adaption

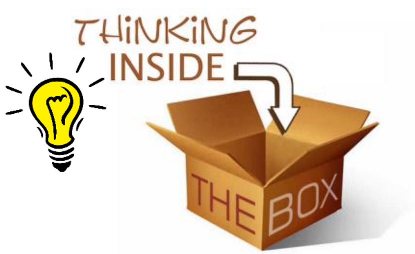
- Inverter-Integr. DC/DC Boost Conv. → Higher DC-Link Voltage / Lower Motor Current
- Access to Motor Star Point & Specific Motor Design Required
- No Add. Components

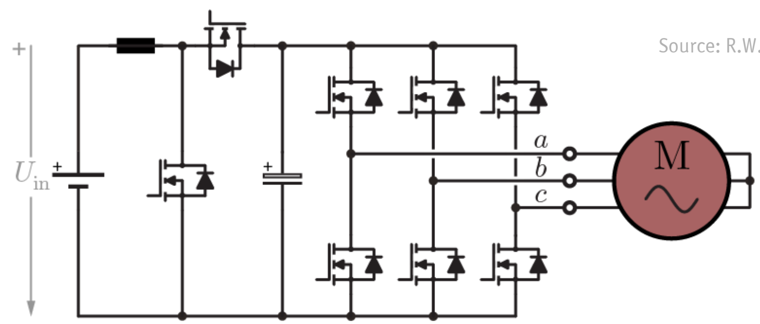


Source: J. Pforr et al. / 2009

- Explicit Front-End DC/DC Boost Stage

Source: www.rick-gerber.com



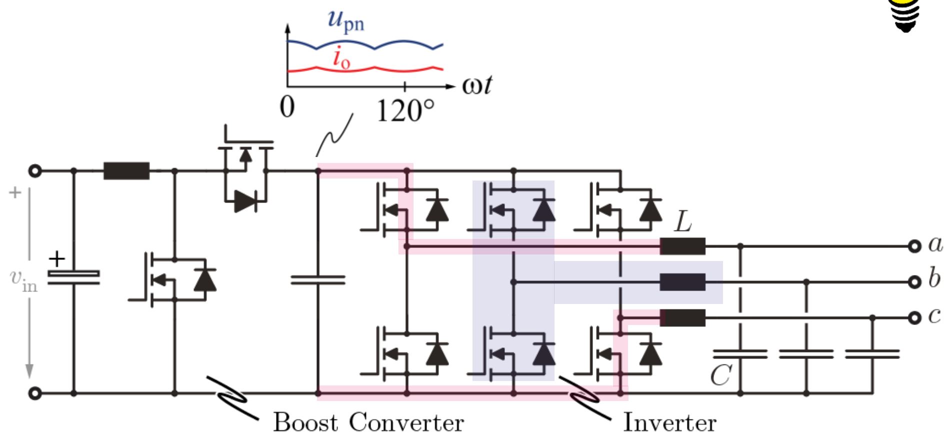


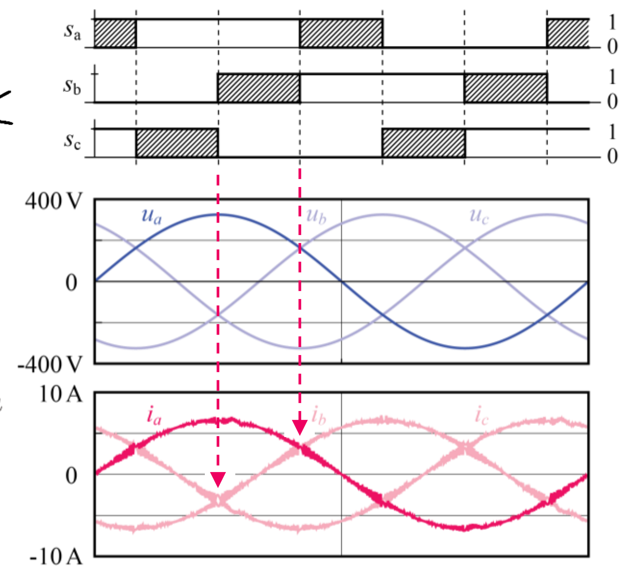
Source: R.W. Erickson et al. / 1986

→ Analyze Coupling of the Control of Both Converter Stages → "Synergetic Control"

▶ Front-End DC/DC Boost Converter

- "Synergetic Control" @ High Output Voltage
- 2 (!) Inverter Phases Clamped → Low Switching Losses / High Efficiency
- Conv. PWM Inverter / Clamped Boost-Stage Operation @ Low Output Voltage

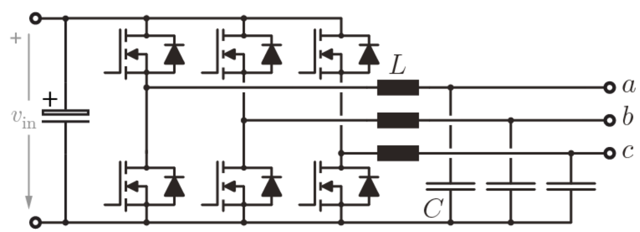


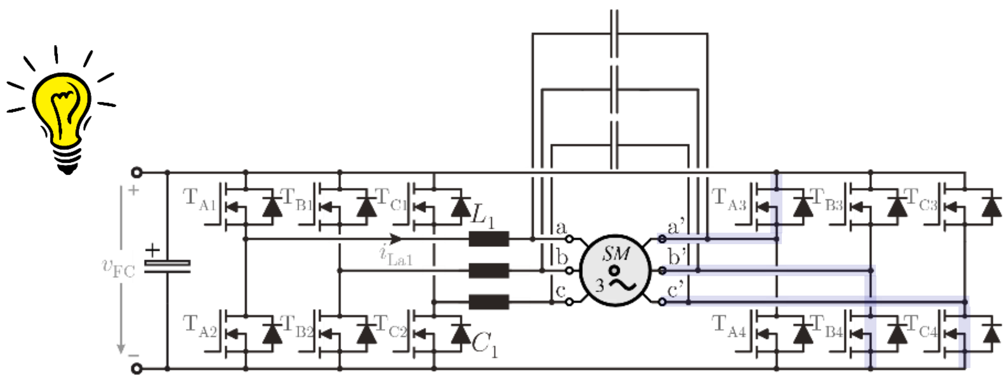


- Preferable for Low Dynamics Drive Systems

▶ Double-Bridge Inverter (1)

- *Alternative to Front-End DC/DC Converter → Eff. Doubles DC-Link Voltage*
- *2nd Bridge Switching with Output Frequ. → "Unfolder" Operation*
- *Avoids Volume and Losses of Boost Stage → Eff. Single-Stage Conversion*
- *Only Three Inductive Components*



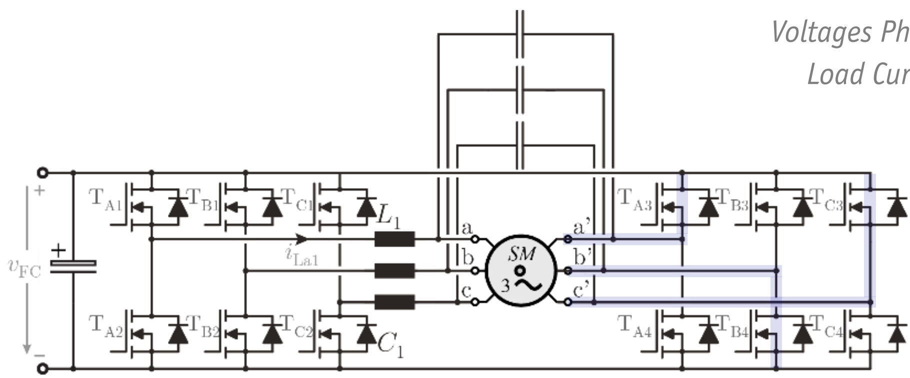


- *Requires Open Winding Motor & Higher Number of Gate Drives*

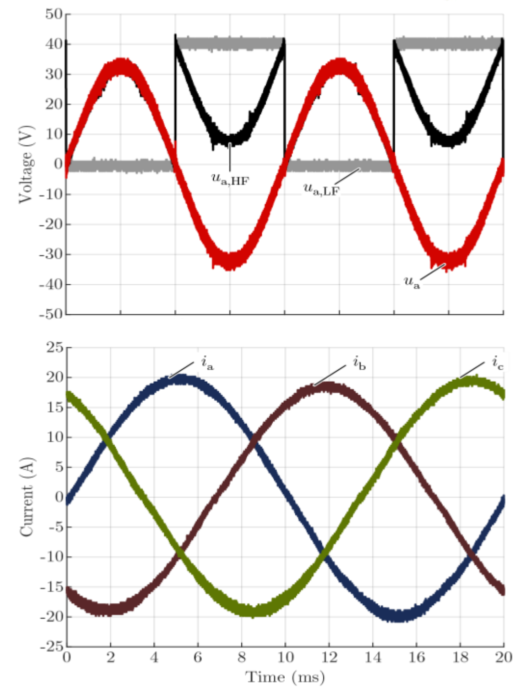
▶ Double-Bridge Inverter (2)

■ Hardware Demonstrator

U_{FC} = 40V
P = 1.0kW
f_S = 350kHz (200V EPC GaN, 2 per Switch)
f_0 = 5kHz



Voltages Phase a
Load Currents



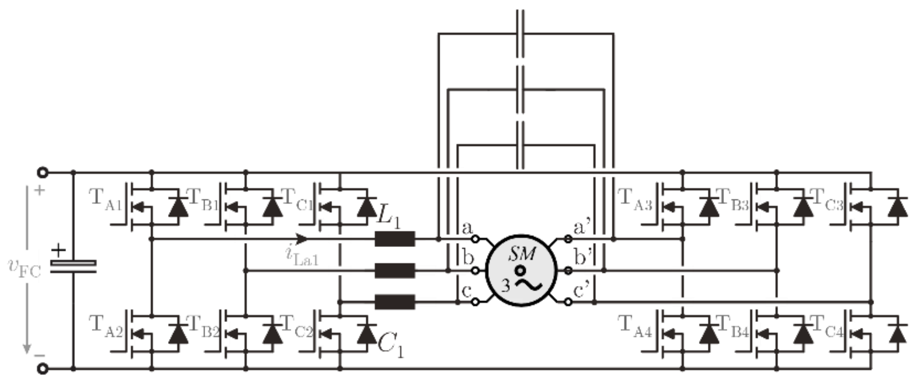
- Requires Open Winding Motor & Higher Number of Gate Drives

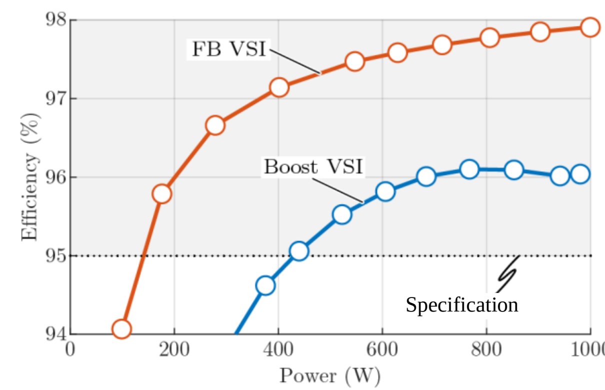
▶ Double-Bridge Inverter (3)

■ **Hardware Demonstrator**

U_{FC} = 40V
P = 1.0kW
f_S = 350kHz (200V EPC GaN, 2 per Switch)
f_0 = 5kHz

240 W/in³





• Requires Open Winding Motor & Higher Number of Gate Drives

Phase-Modular Topologies

Boost+Buck Modules
Buck+Boost Modules

General Remarks

- *Usually DC Link Voltage Midpoint Considered as AC Output Ref. Point*
- *Open Machine Starpoint → Introduce CM Voltage Shift → Neg. DC Rail as Reference*

Source: Cuk (1982)

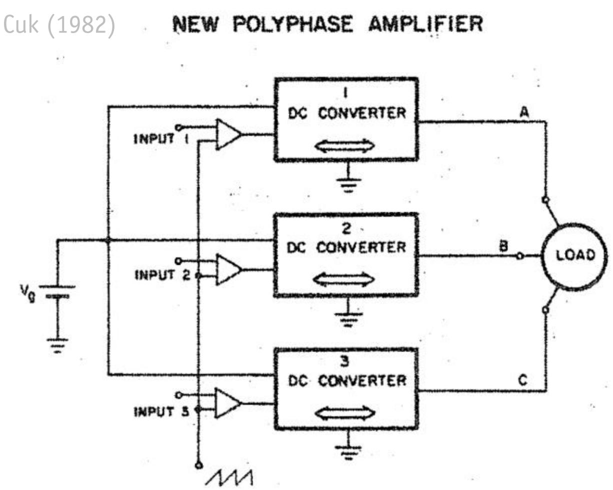


Fig. 7. New three-phase switching amplifier. Three bidirectional dc-dc converters, with their own modulators, driven by a set of three-phase sine waves, constitute three phase voltages around the differential load.

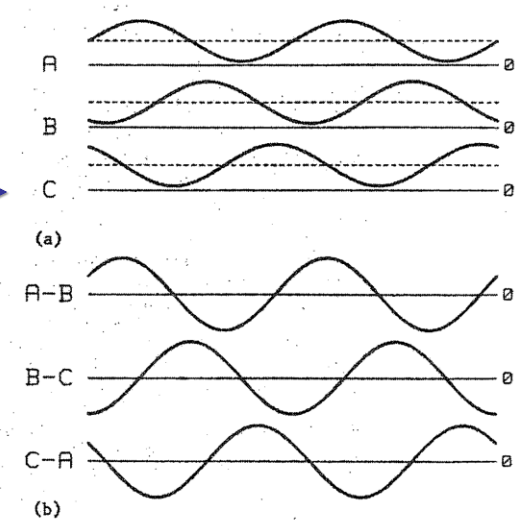
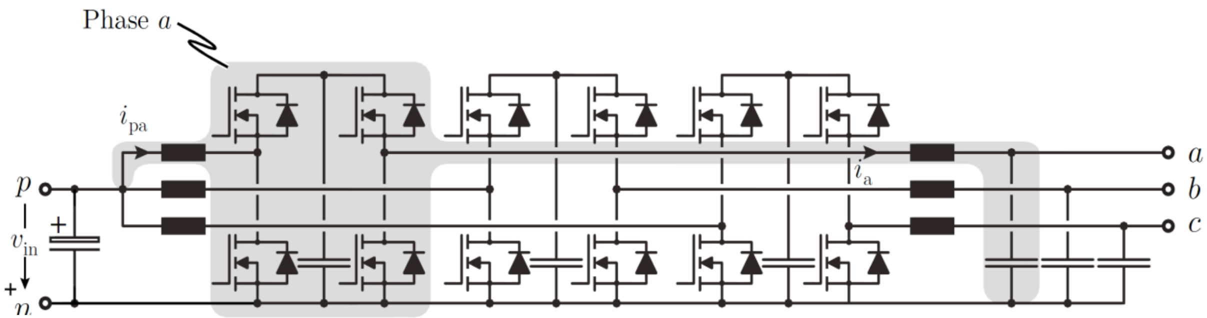


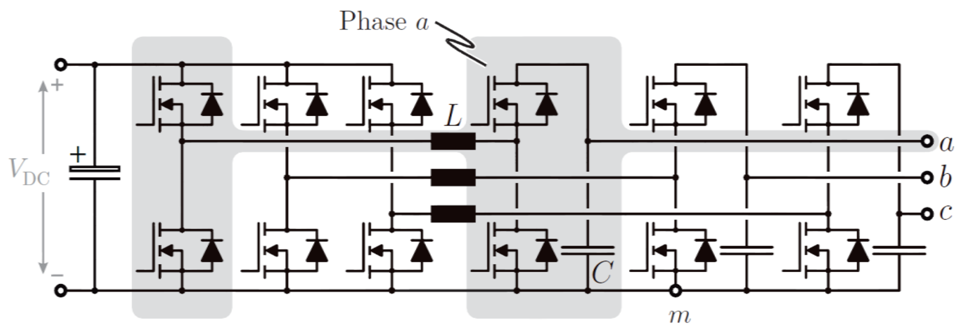
Fig. 8. (a) Line-to-ground and (b) line-to-line voltages generated by the new three phase power amplifier. The dc component of the line-to-ground voltages automatically disappears in line-to-line voltages which are pure ac.

→ *Realization of 3-Φ Inverter Using 3 DC/DC Converter (Phase) Modules — S. Cuk/1982*

▶ *Phase-Modular Boost+Buck / Buck+Boost Inverter*

- *Wide Voltage Conv. Range* → *Battery or Fuel-Cell Supply & Adaption to Motor Voltage*
- *Continuous Output Voltage* → *Explicit / Integr. LC Output Filter*

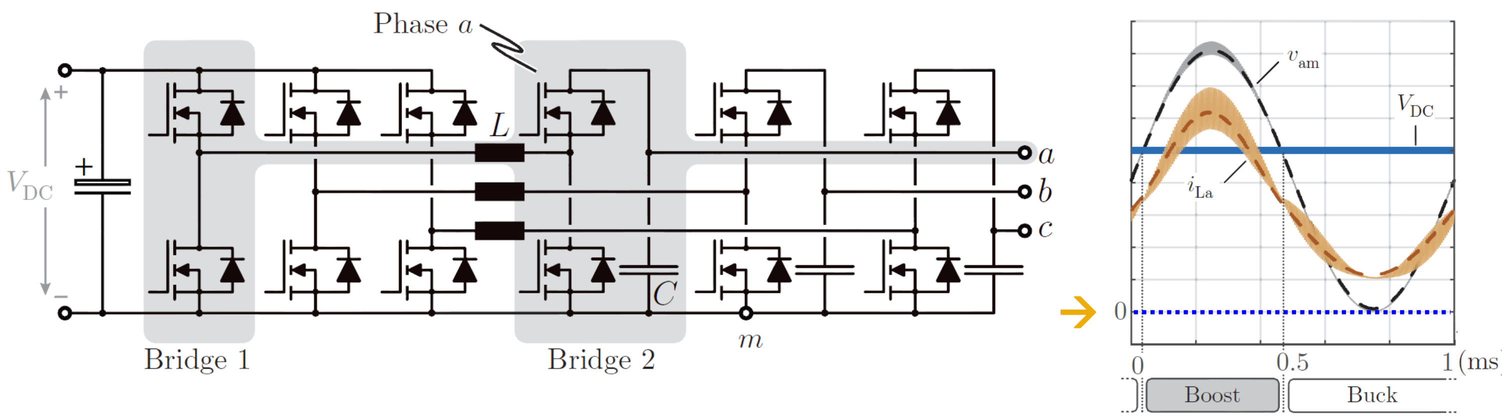




→ *Preference for Low Number of Ind. Components* → *Buck+Boost Concept — "Y-Inverter"*

Y-Inverter Lighthouse Project

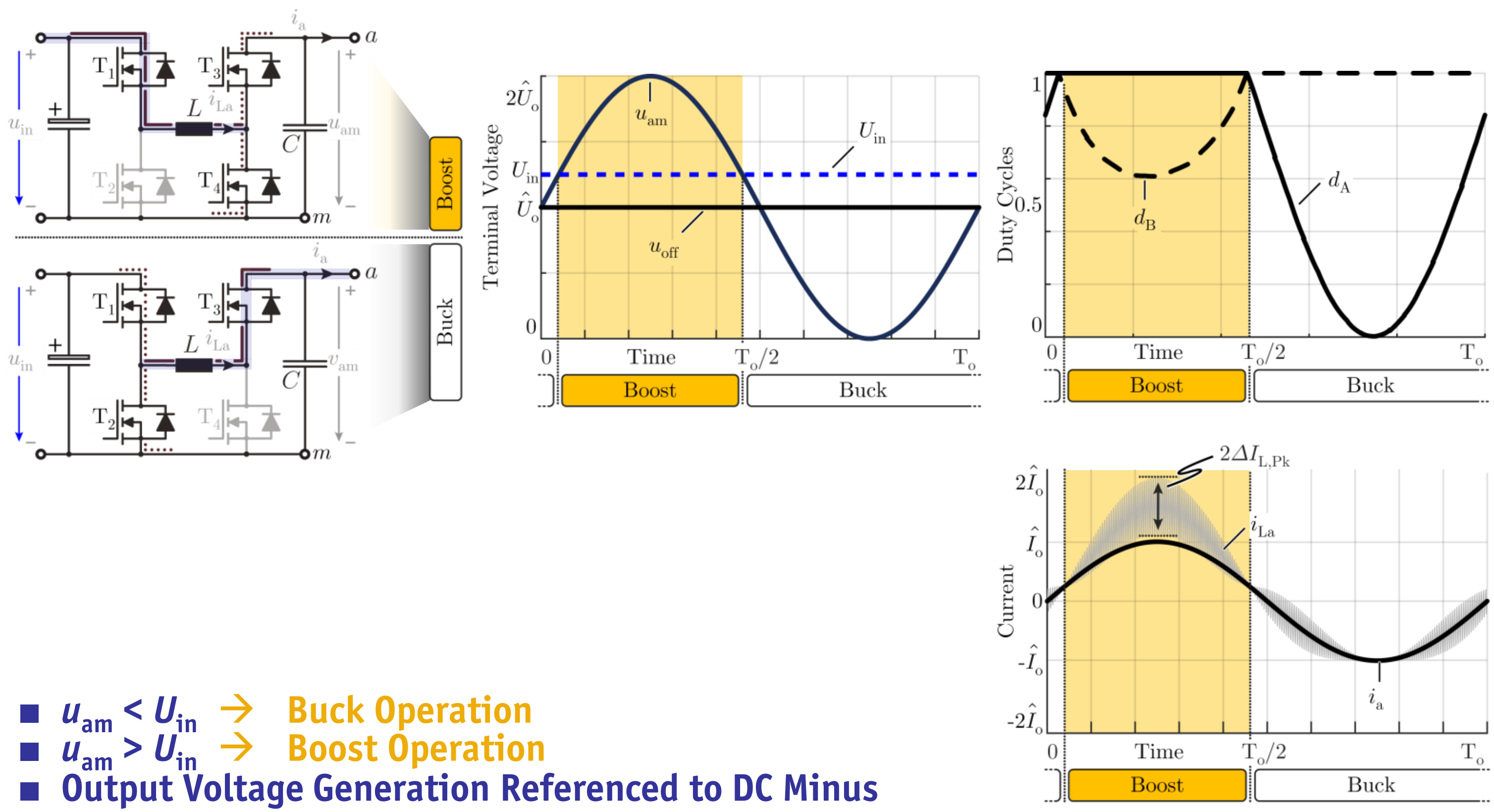
- Three-Phase Continuous Output / Low EMI ! - No Shielded Cables / No Insul. Stress
- Buck+Boost Operation / Wide Input &/or Output Range - Industrial Drive
- Standard Bridge Legs / Building Blocks - 1.2kV SiC MOSFETs
- ZVS Operation / Extreme Power Density



■ Project Scope → Hardware Demonstrator / Exp. Analysis / Comparative Evaluation

▶ Y-Inverter (1)

- *Operating Behavior*

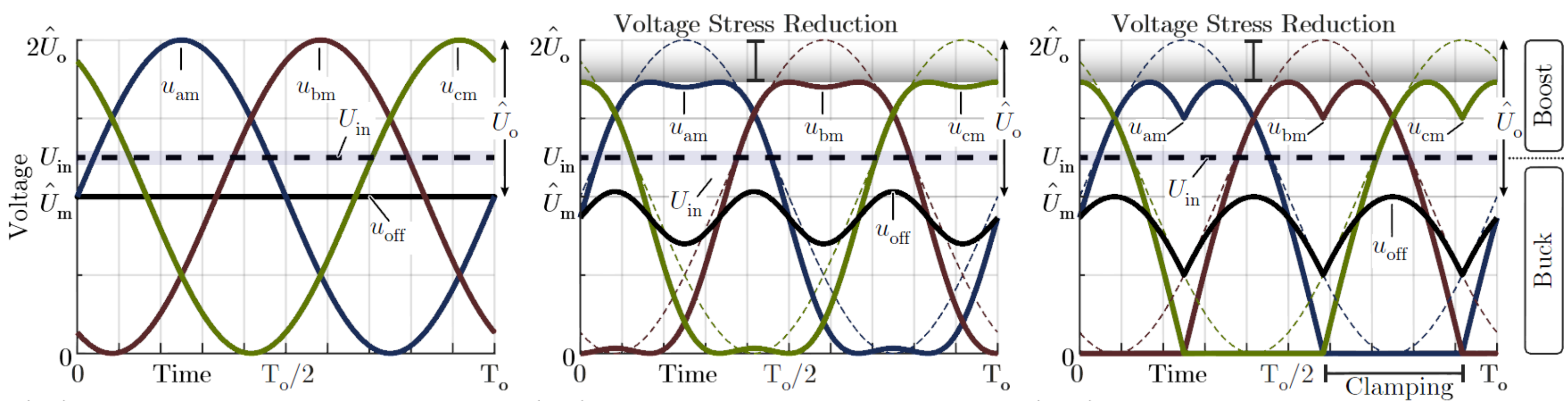


- $u_{am} < U_{in}$ → **Buck Operation**
- $u_{am} > U_{in}$ → **Boost Operation**
- **Output Voltage Generation Referenced to DC Minus**

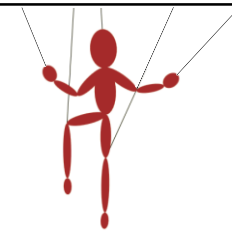
▶ Y-Inverter (2)

- *Modulation Scheme*

- *Sinusoidal Modulation* → *Variable Output Voltage DC Offset for Low Mod. Index*
- *3rd Harmonic Injection* *OR Phase Clamping as Alternative Concepts*

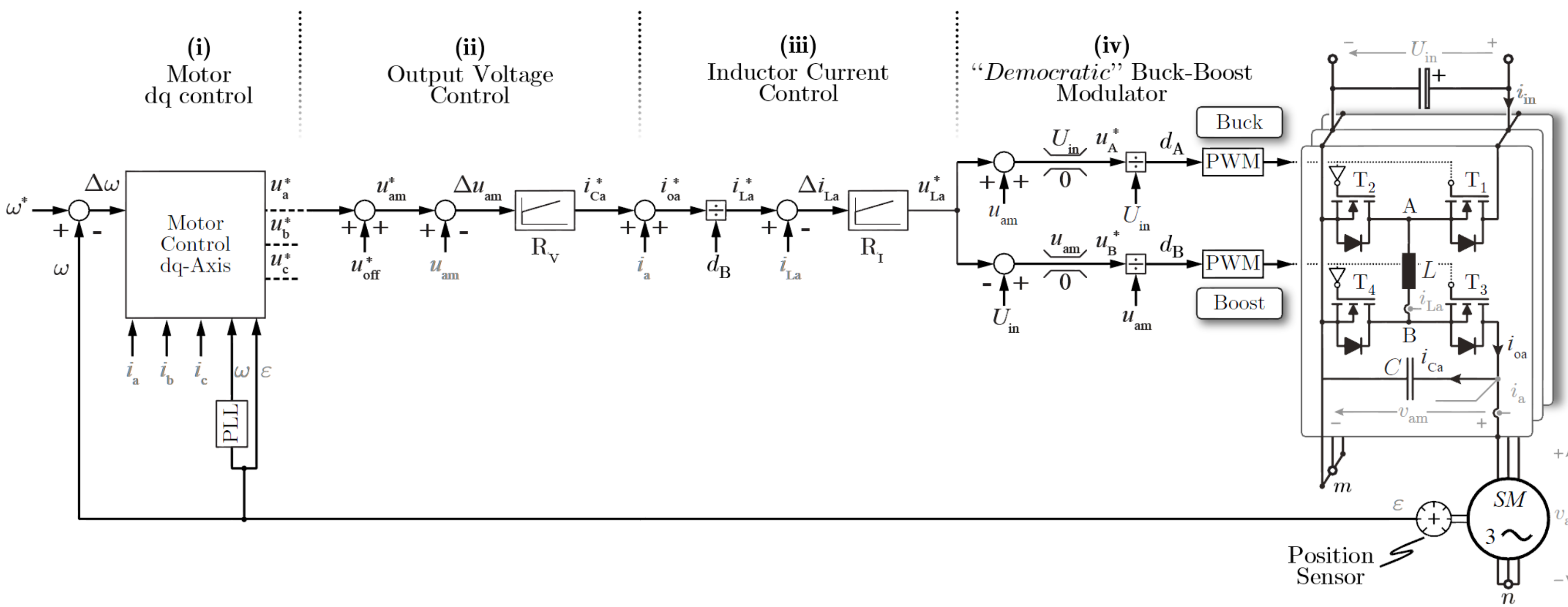


- *Adv. of Reduced Voltage Against DC-* & *Reduction of Sw. Losses*



▶ Y-Inverter (3)

- *Control Structure*

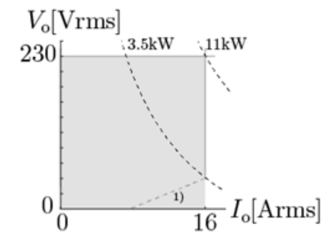


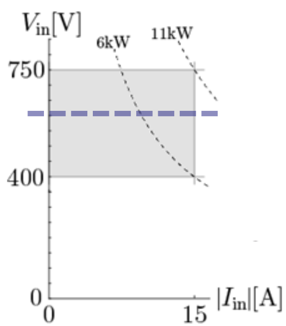
- *"Democratic Control"* → **Seamless Transition Between Buck & Boost Operation**

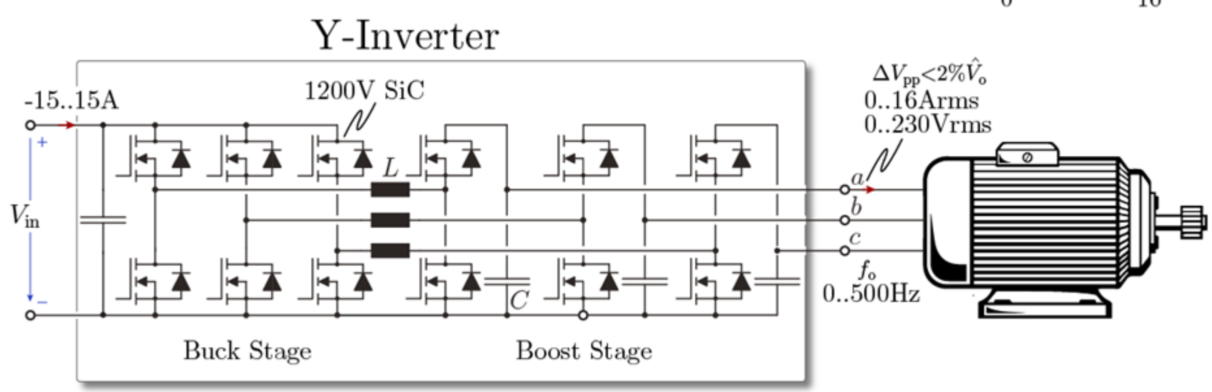
▶ Y-Inverter Prototype (a)

- *Demonstrator Specifications*

- Wide Input Voltage Range → 400...750V_{DC}
- Max. Input Current → ± 15A



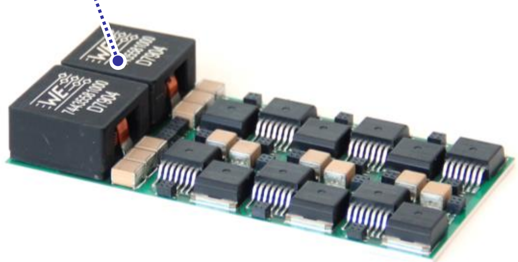


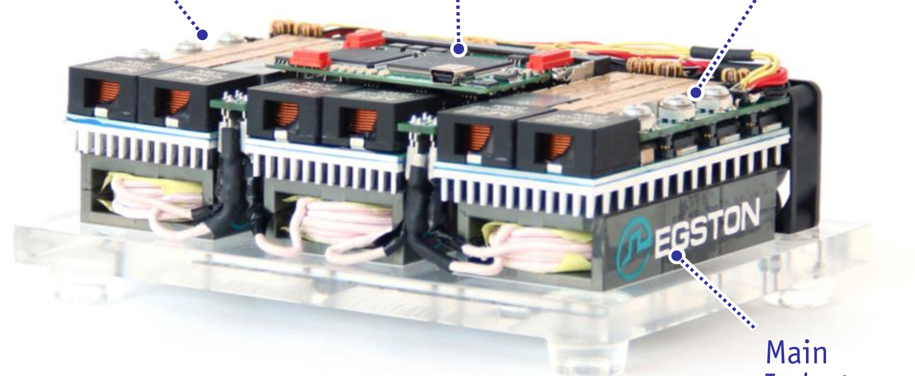


- Max. Output Power → 6...11 kW
- Output Frequency Range → 0...500Hz
- Output Voltage Ripple → 3.2V Peak-to-Peak (incl. Add. Output Filter)

► Y-Inverter Prototype (b)

- DC Voltage Range 400…750V_{DC}
- Max. Input Current ± 15A
- Output Voltage 0…230V_{rms} (Phase)
- Output Frequency 0…500Hz
- Sw. Frequency 100kHz
- 3x SiC (75mΩ)/1200V per Switch
- IMS Carrying Buck/Boost-Stage Semicond. & Comm. Caps & 2nd Filter Ind.





- Dimensions → 160 x 110 x 42 mm^3 (15kW/dm^3, 245W/in^3)

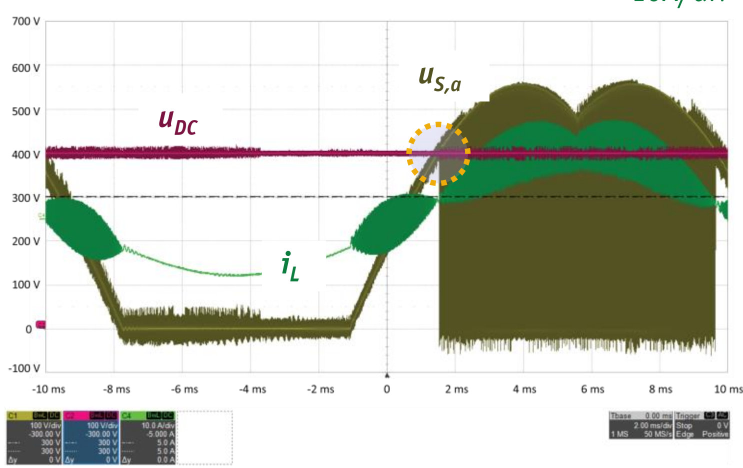
▶ Y-Inverter Prototype (c)

- *Measurement Results*

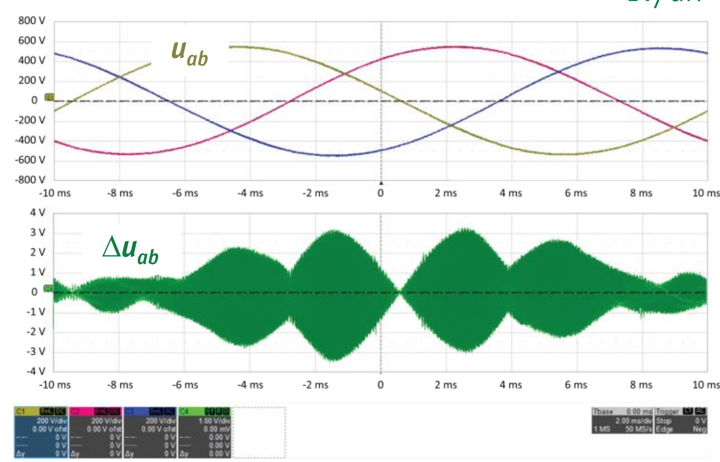
U_{DC}= 400V
U_{AC}= 400V$_{rms}$ (Motor Line-to-Line Voltage)
f_0= 50Hz
f_S = 100kHz / DPWM

P = 6.5kW

100V/div
10A/div



200V/div
1V/div

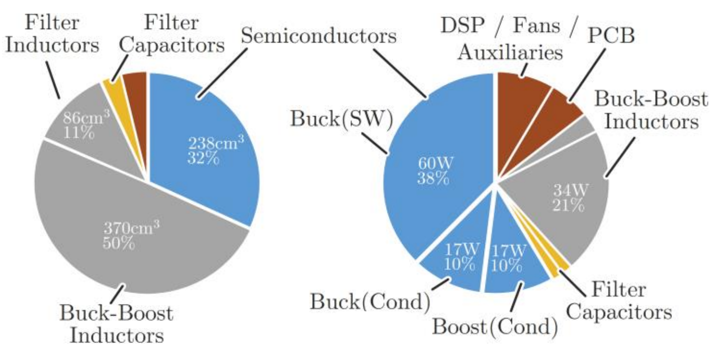


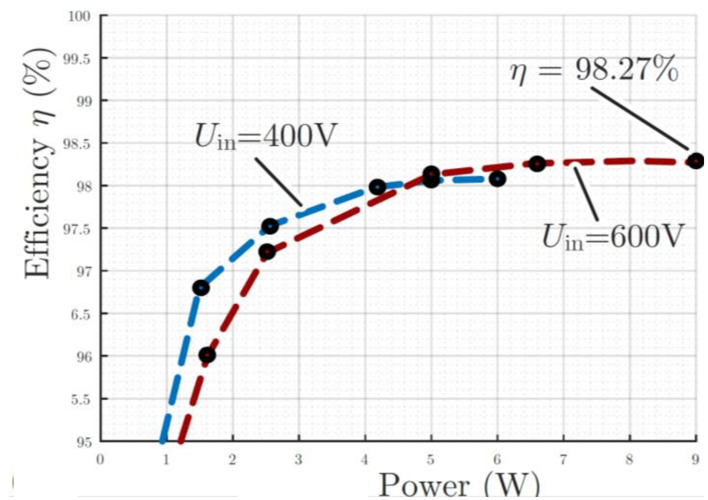
→ *Line-to-Line Output Voltage Ripple < 3.2V*

► Y-Inverter Prototype (d)

- *Demonstrator Performance – Efficiency over Output Power @ Given Input Voltage*

U_{DC}= 400V / 600V
U_{AC}= $230V_{rms}$ (Motor Phase Voltage, rms)
f_S = 100kHz

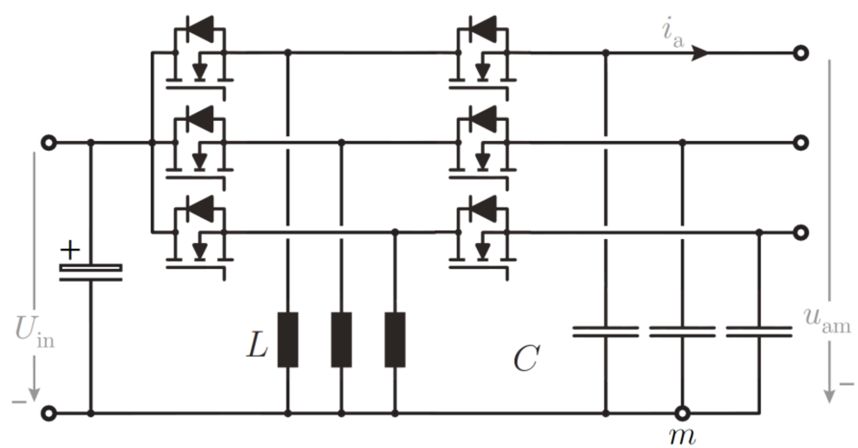




→ *Multi-Level Bridge Leg Structure for Ind. Comp. Volume Reduction*

▶ Alternative Topology

- *Phase Modules Based on 2-Switch Buck+Boost Topology*



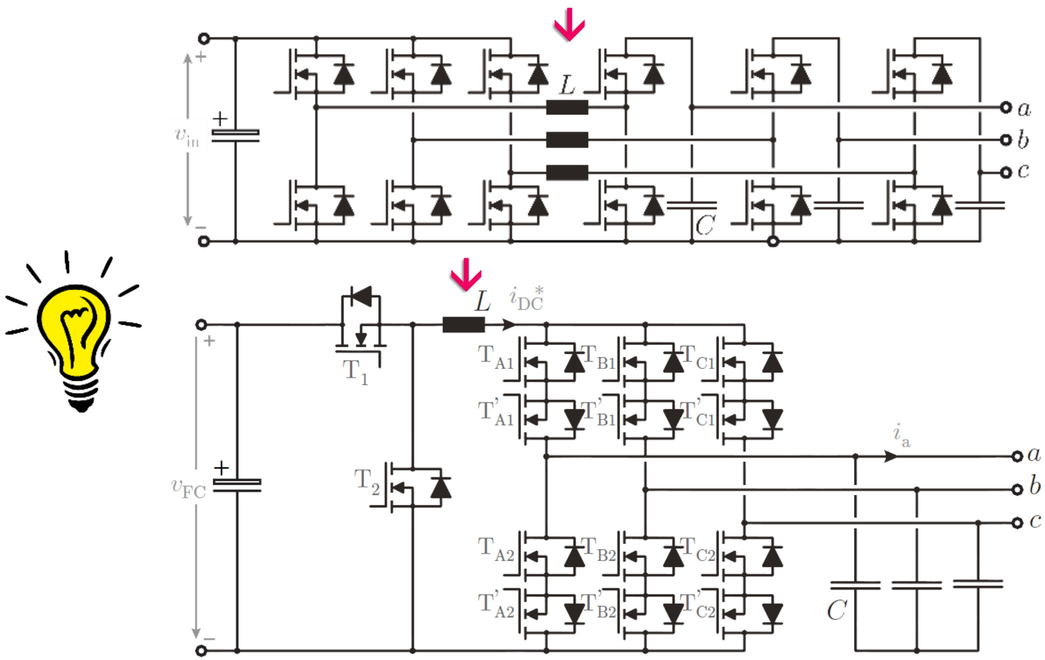
■ **Lower Number of Switches / Higher Component Stresses** → *Low Power Applications*

DC/DC Buck Stage & Current Source Inverter

Monolithic Bidir. GaN Switches
Synergetic Control

► Current Source Inverter (CSI) Topologies

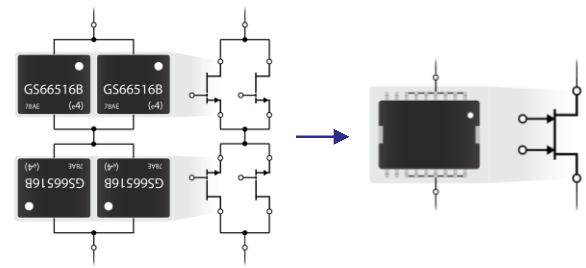
- *Phase Modular Concept → Y-Inverter (Buck-Stage / Current Link / Boost-Stage)*
- *3-Φ Integrated Concept → Buck-Stage & Current DC Link Inverter*

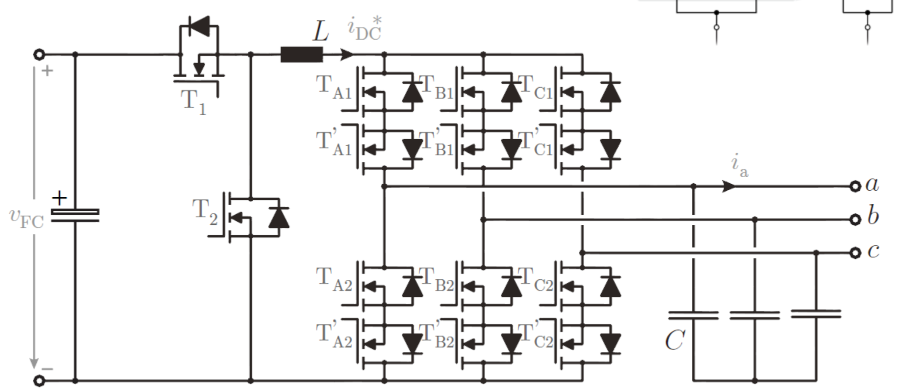


→ Low Number of Ind. Components & Utilization of Bidir. GaN Semicond. Technology

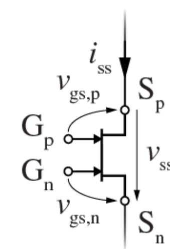
► 3-Φ Integrated Buck-Boost CSI (1)

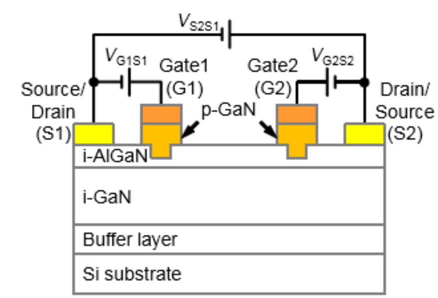
- Basic Topology Proposed in 1984 (Ph.D. Thesis of K.D.T. Ngo/CPES)
- Bidir./Bipolar Switches → Positive DC-Side Voltage for Both Directions of Power Flow





Source: Panasonic ideas for life

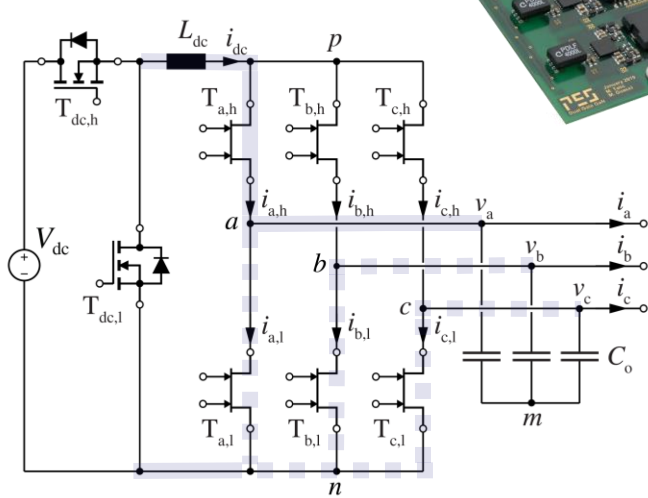


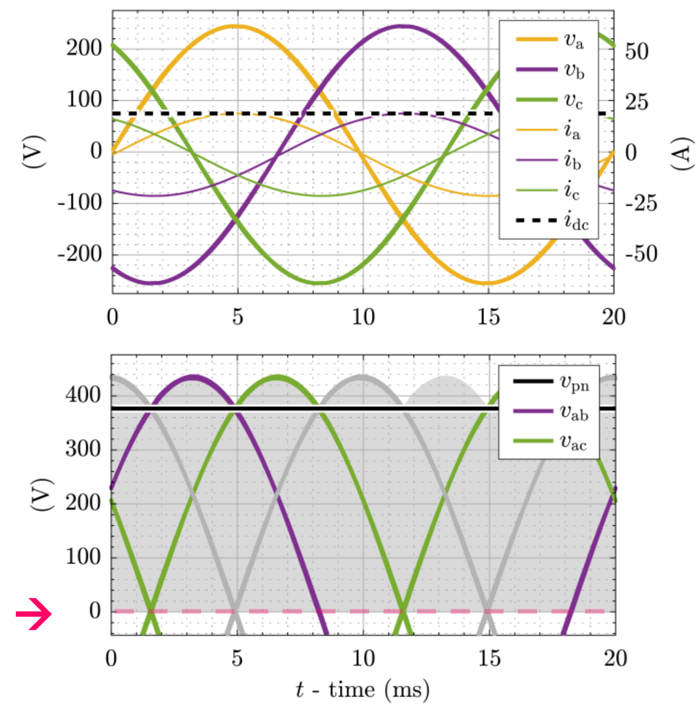


→ Monol. GaN Switches → Factor 4 Improvement in Chip Area Comp. to Discrete Realiz.
→ Also Beneficial for Matrix Converter Topologies

▶ 3-Φ Integrated Buck-Boost CSI (2)

- ***Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates / Full Controllability***
- ***Buck-Stage for Const. DC Current / PWM CSI for Output Voltage Control***

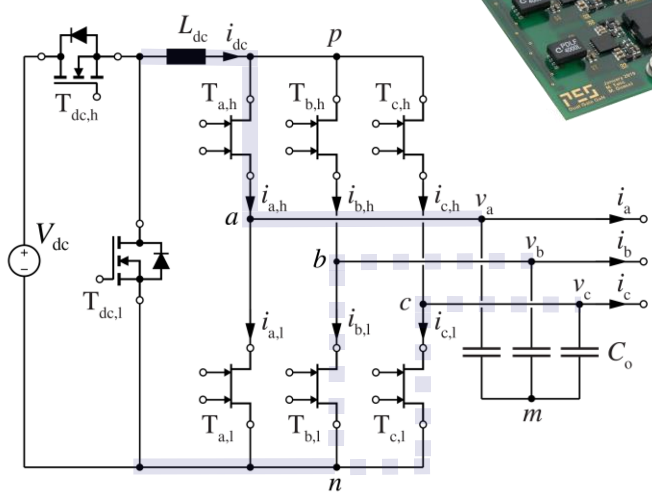


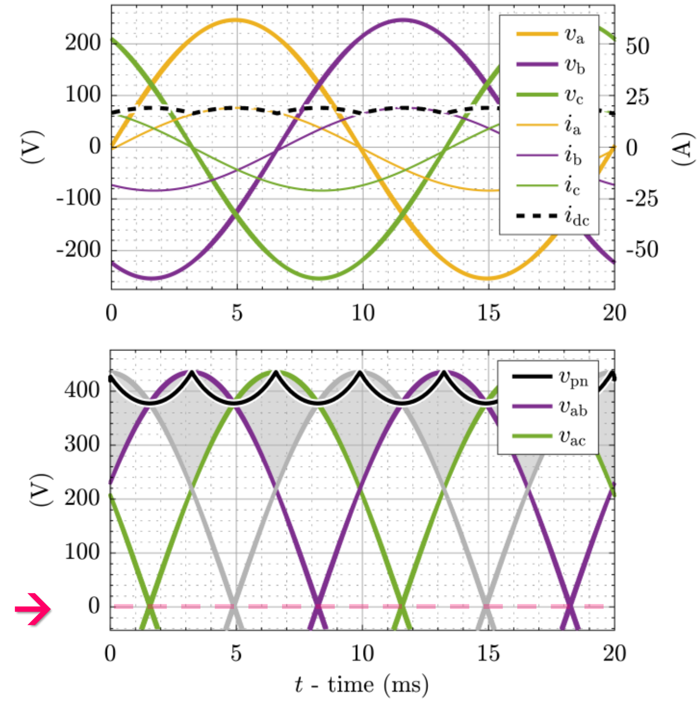


→ ***"Synergetic Control" of Buck & Inverter Stage for Red. of Sw. Losses (≈ -86%)***

▶ 3-Φ Integrated Buck-Boost CSI (3)

- Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates / Full Controllability
- "Synergetic" Variable DC Curr. Control of Buck Stage & Inv. Stage Clamping → 2/3 PWM

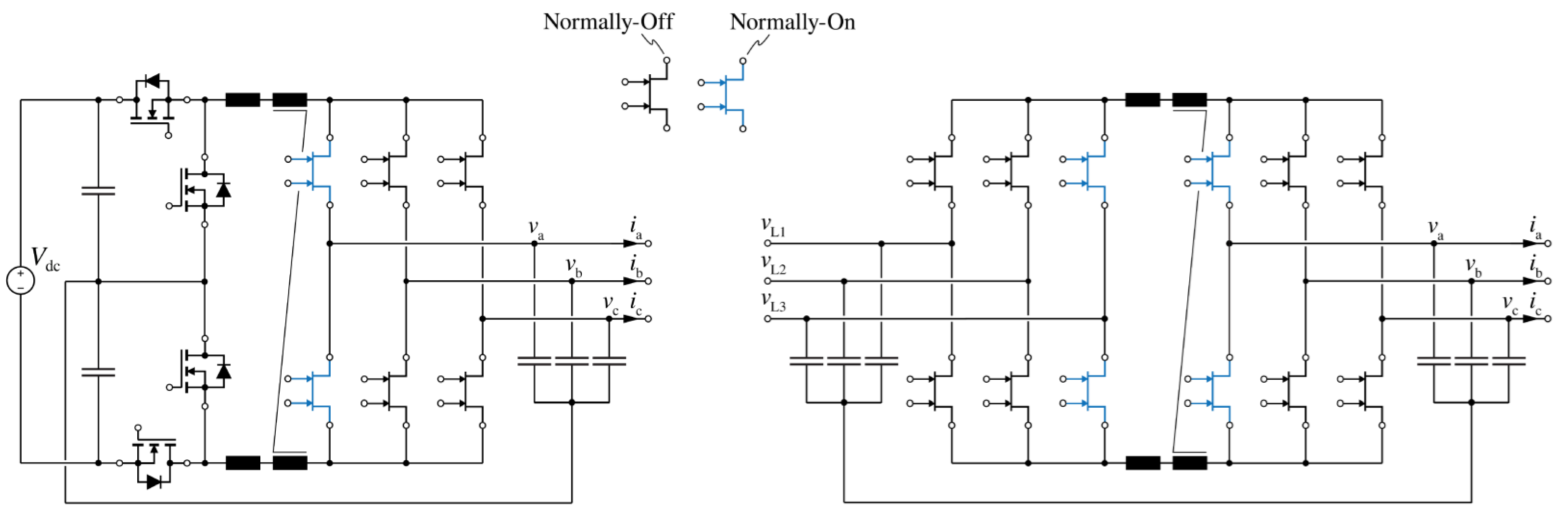




→ Experimental Analysis in Progress (Upcoming Publication)

► Future Research

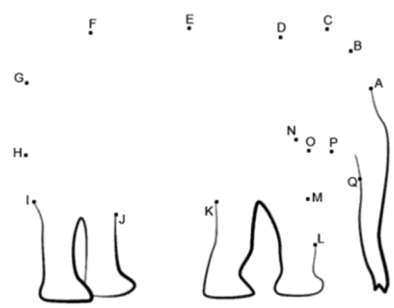
- *Advanced DC/AC Topologies incl. CM-Filtering*
- *Extension of 2/3-PWM to Bipolar DC-Link Voltage 3-Φ AC/AC Converter*
- *Multi-Objective Design & Comparative Evaluation*



- *Partial Use of "Normally-On" Switches for Freewheeling in Case of Auxiliary Power Loss*

Further Concepts

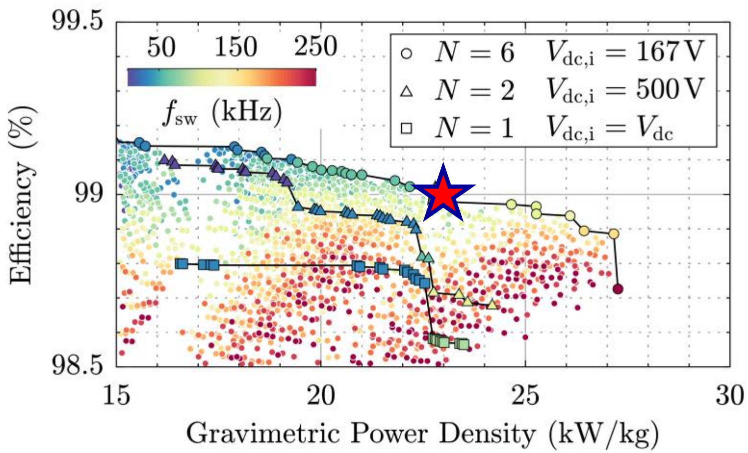
Integrated Modular Motor Drive

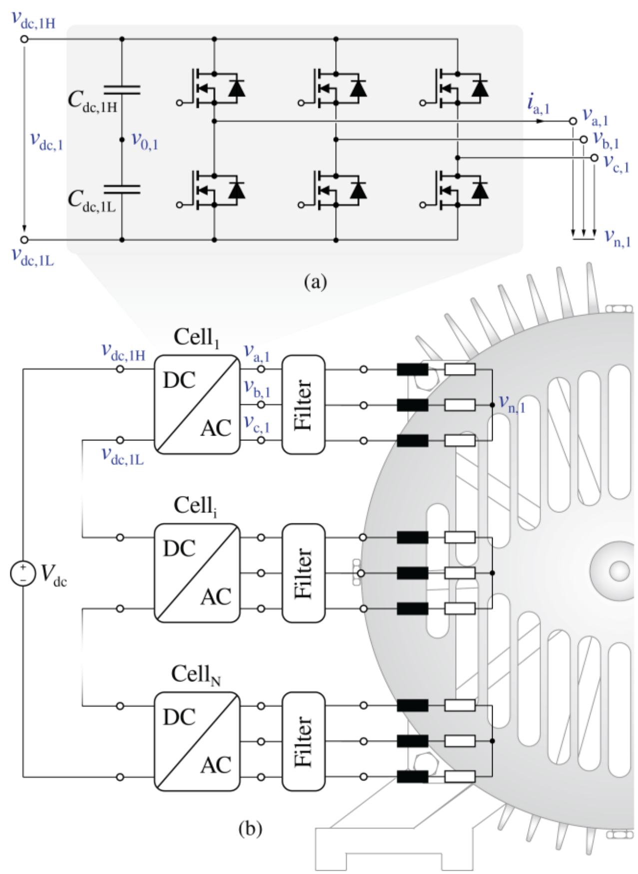


► Integrated Modular Motor Drive

- Machine/Inverter Fault-Tolerant VSD
- Motor Integr. Low-Voltage Inverter Modules
- Very-High Power Density / Efficiency
- Supply of 3-Φ Winding Sets / Low C Buffer Cap.

- Rated Power 45kW / f_{out} = 2kHz
- DC-Link Voltage 1 kV





→ Evaluate Machine Concept (PMSM vs. SRM etc.) / Wdg Topologies / Filter Requ. / etc.

3-Φ PFC Rectifier System

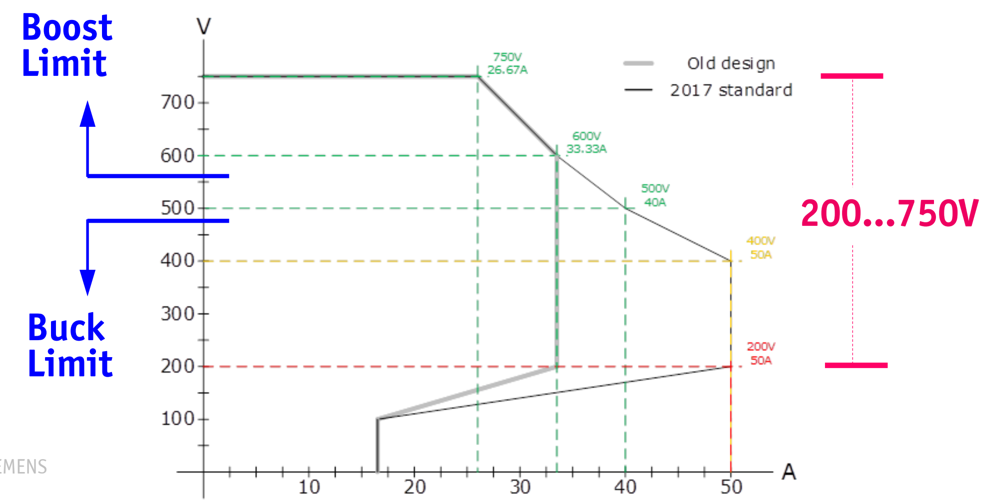
Introduction
Buck+Boost Topologies

Source: Porsche Mission-E Project

High-Power EV Battery Charging

- *China* - EV Charging Equipment Supplier Qualification Standard
- *Extremely Wide DC Output Voltage Range*

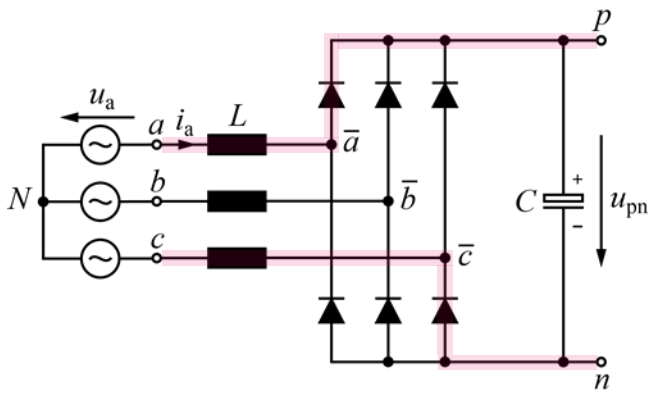
Source: SIEMENS

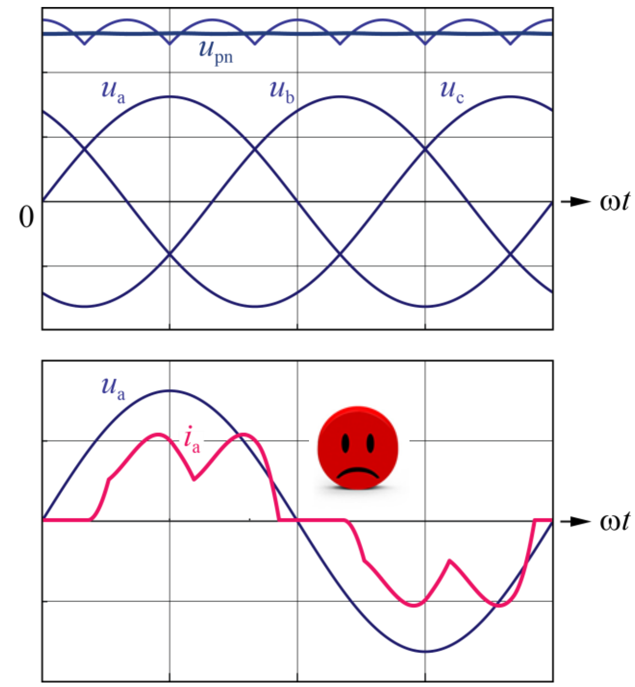


→ *Buck-Boost Functionality & Isolation Requirement*

▶ 3-Φ Diode Bridge Rectifier

- Conduction States Defined by *Line-to-Line* Mains Voltages
- Intervals with *Zero Current* / LF Harmonics
- No Output Voltage Control

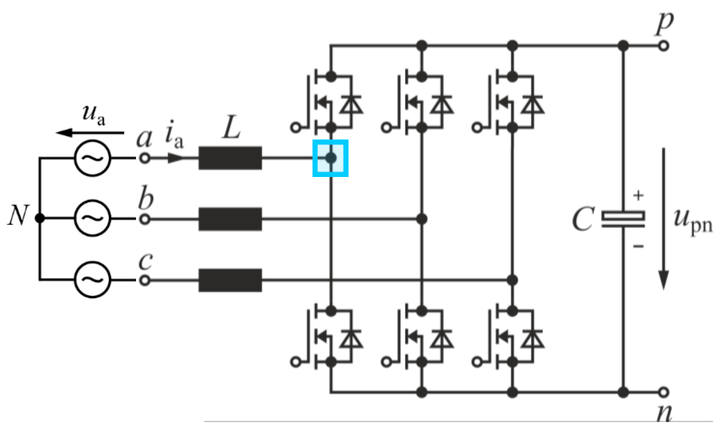


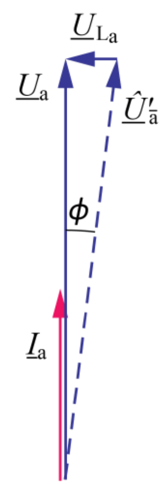


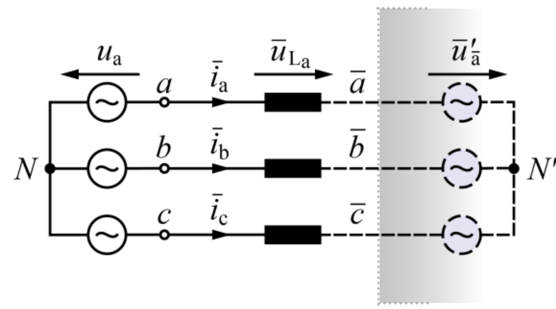
→ *Active Mains Current Shaping* / Modulation of Diode Bridge Input Voltages

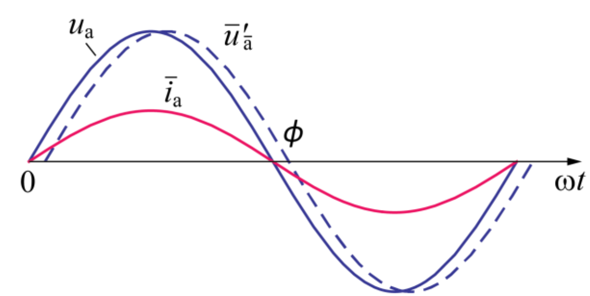
▶ 3-Φ Sinusoidal Input Current Rectifier

- *Mains Current Impressed by Difference of Mains & Diode Bridge Input Voltage*
- *Pulse-Width Modulation of Bridge Legs for Avg. Sinusoidal Voltage Generation*





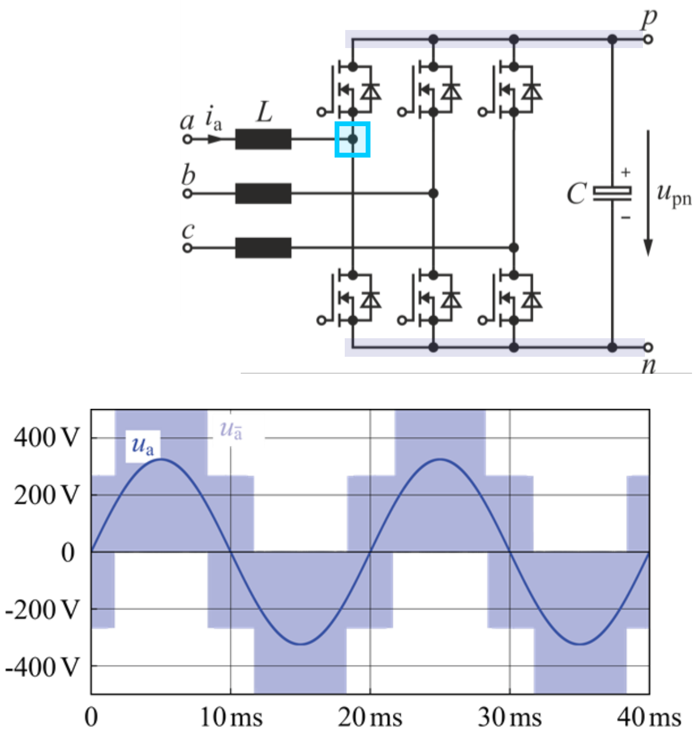


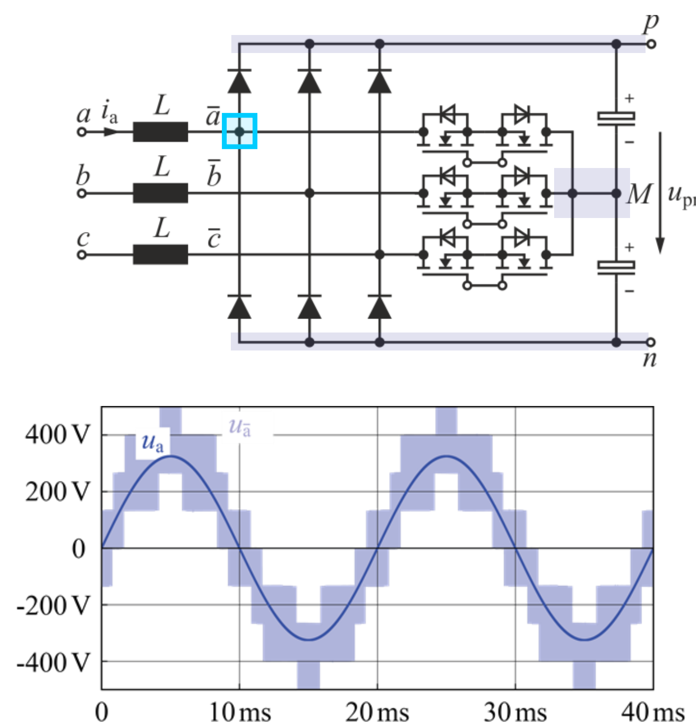


→ *2-Level vs. 3-Level PWM Voltage Generation*

► 2-Level vs. 3-Level Voltage Generation (1)

- Comparison to Standard *2-Level* PWM Rectifier & *3-Level VIENNA Rectifier*
- *9 vs. 5 Volt. Levels & Factor 2…3 Lower Sw. Losses → Factor 4…6 (!) Lower L*

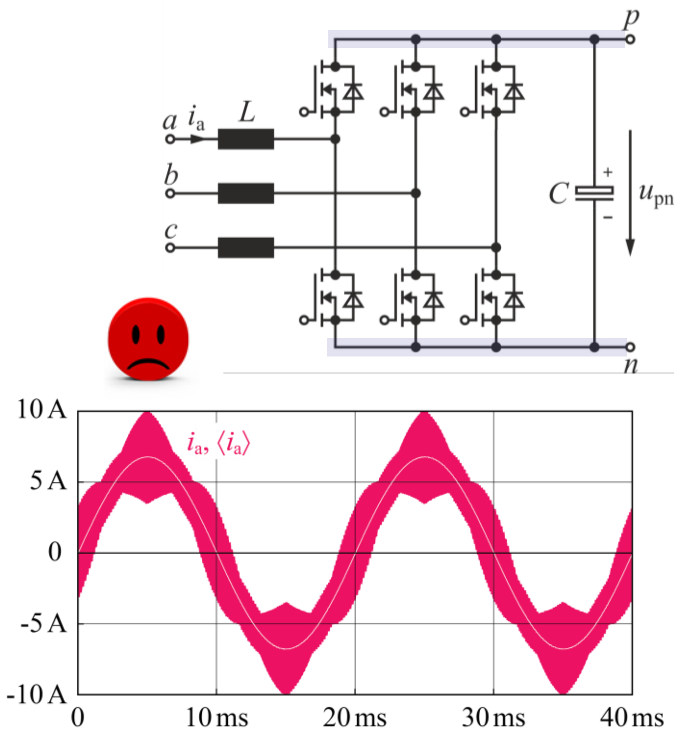


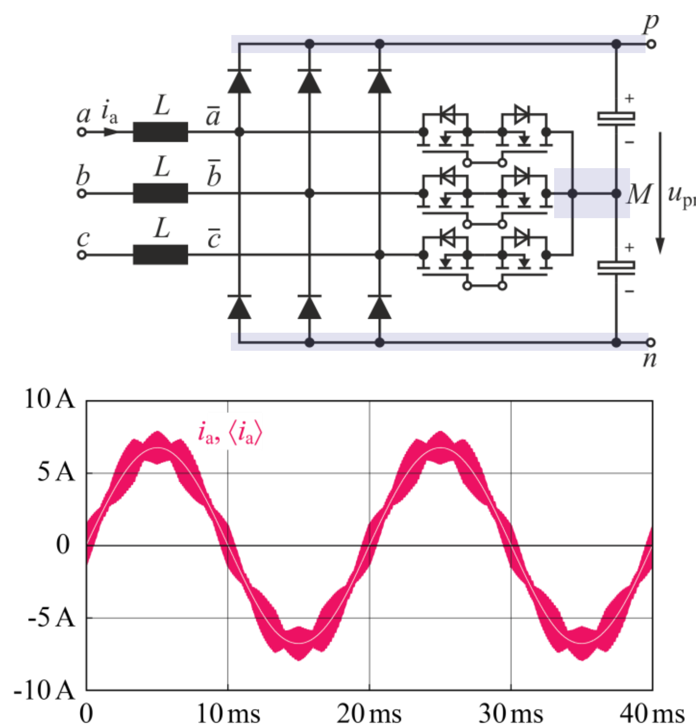


- Standard PWM Rectifier
- *VIENNA Rectifier*

▶ 2-Level vs. 3-Level Voltage Generation (2)

- **Comparison to Standard *2-Level* PWM Rectifier**
- ***9 vs. 5 Volt. Levels & Factor 2…3 Lower Sw. Losses* → *12 kW/dm³* vs. *8 kW/dm³* @ 22kW**



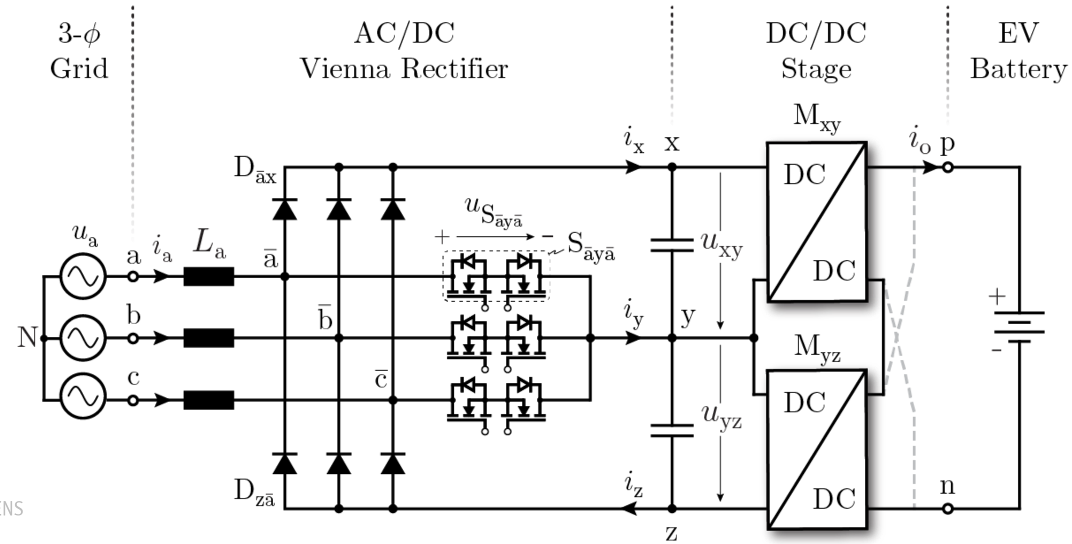


- **Standard PWM Rectifier**
- ***VIENNA Rectifier***

▶ Selected EV Charger Topology

- Isolated Controlled Output Voltage
- Buck-Boost Functionality & Sinusoidal Input Current
- *Applicability of 600V GaN Semiconductor Technology*
- *High Power Density / Low Costs*

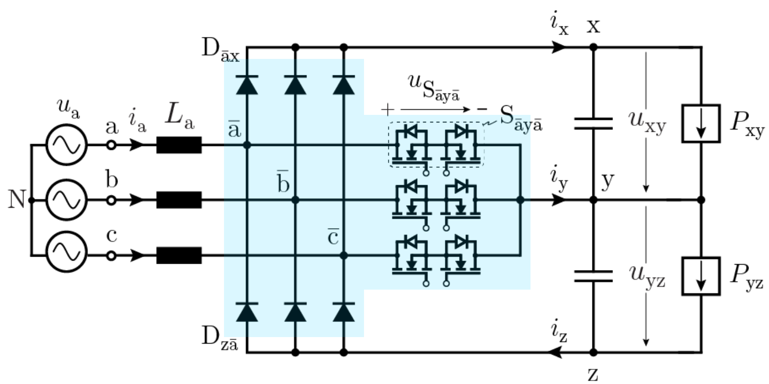
Source: SIEMENS

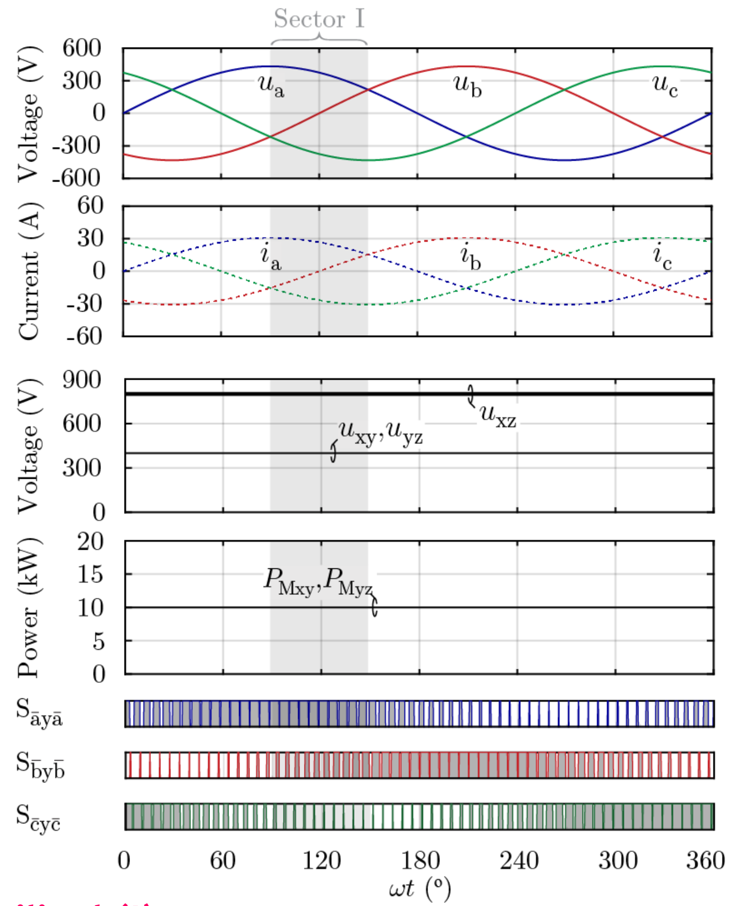


→ Conventional / Independent ***OR*** *"Synergetic Control" of Input & Output Stage*

▶ Conventional Control

- **Decoupled Control of AC/DC- & DC/DC-Stage**
- **Constant DC-Link Voltage (Equally Splitted)**
- **Cont. Sw. of All AC/DC Phases → 3/3 PWM**

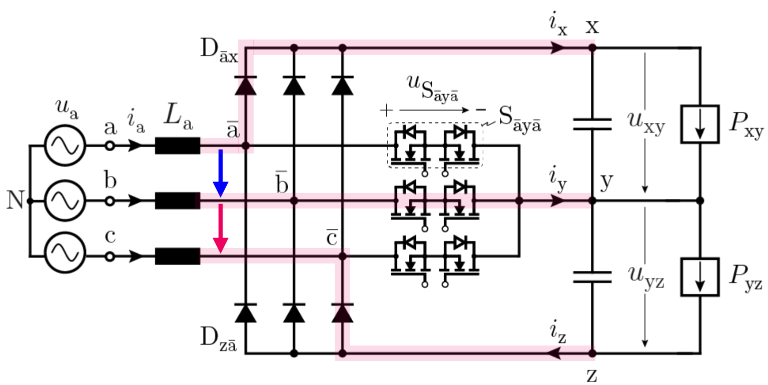


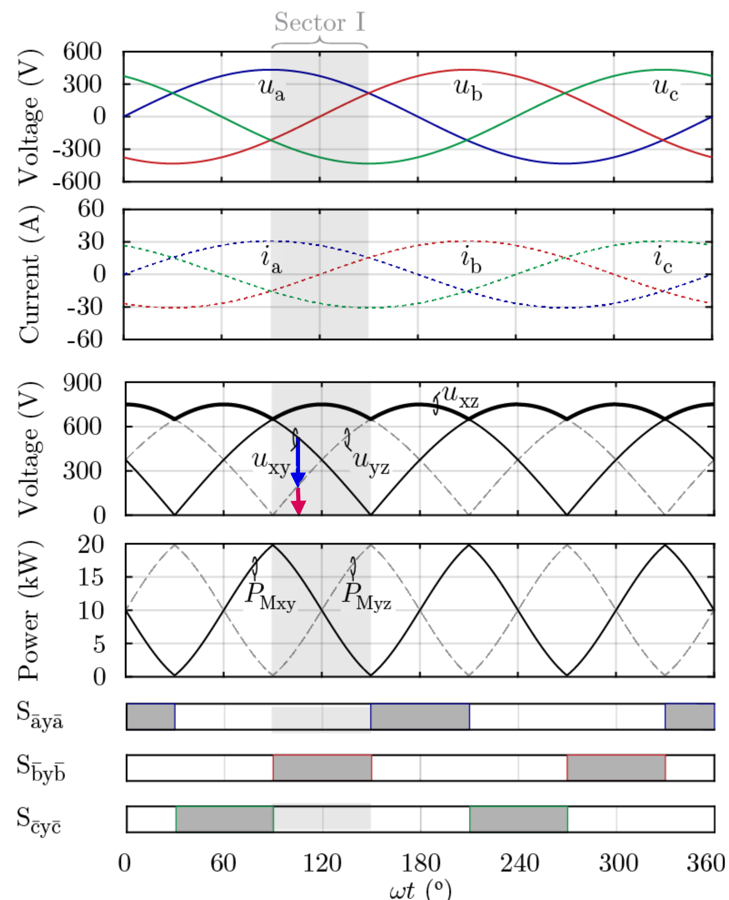


→ **Control Capability & Control DOFs NOT Fully Utilized (!)**

▶ 3-Φ Unfolder Rectifier Stage

- *100Hz/120Hz Operation of Power Switches*
- *Only Conduction Losses of AC/DC Stage*
- *All Current & Voltage Control by DC/DC Stage*
- *600V Semiconductors CANNOT Be Used (!)*

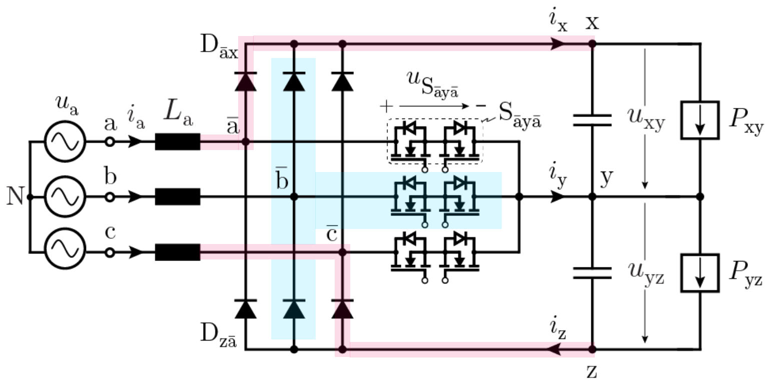


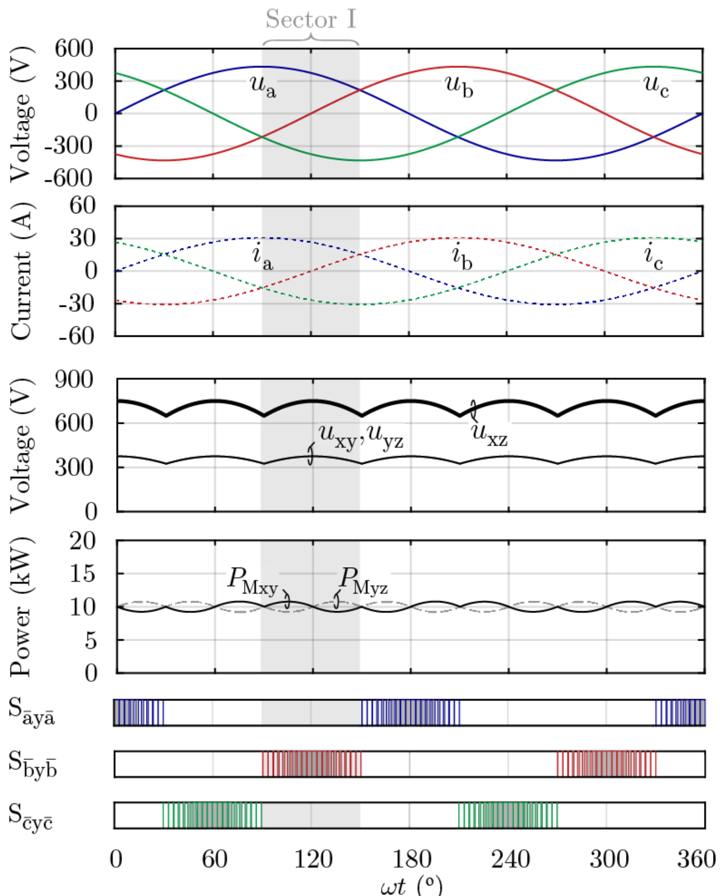


→ *Remark: Inductors Could be Omitted (!)* → *No Boost Capability*

► "Synergetic" Control

- *Only Phase with Lowest Current Switched*
- *Control of 2 Phase Currents by DC/DC-Stage*
- *Low Stresses on Power Switches*
- *600V GaN Semiconductors Can be Used (!)*



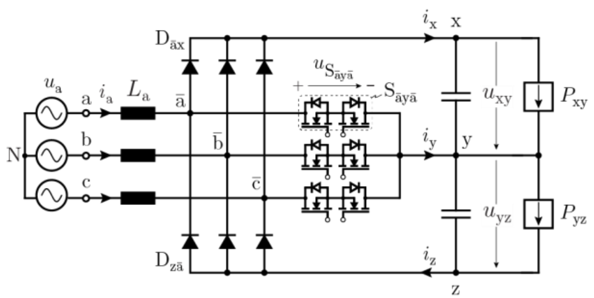


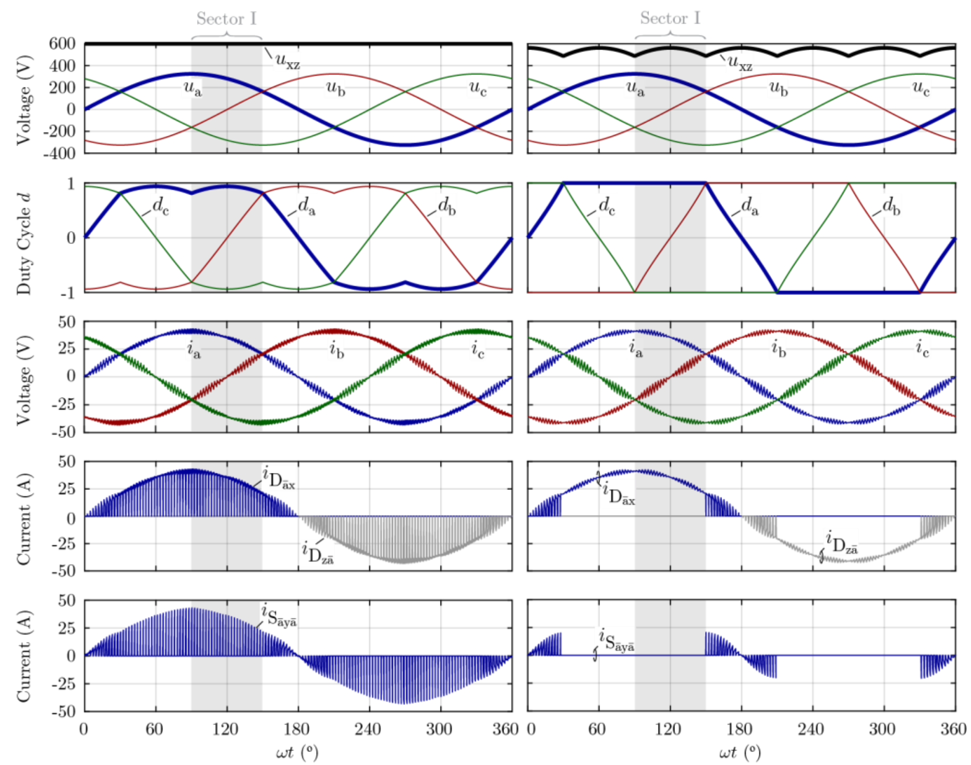
→ *Boost Capability Maintained (Transition to 3/3-PWM)*

▶ Conventional vs. "Synergetic" Control

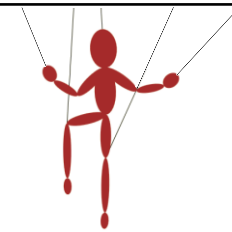
- *1/3-Modulation → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM*

- *Conduction Losses ≈ -80%*
- *Switching Losses ≈ -70%*





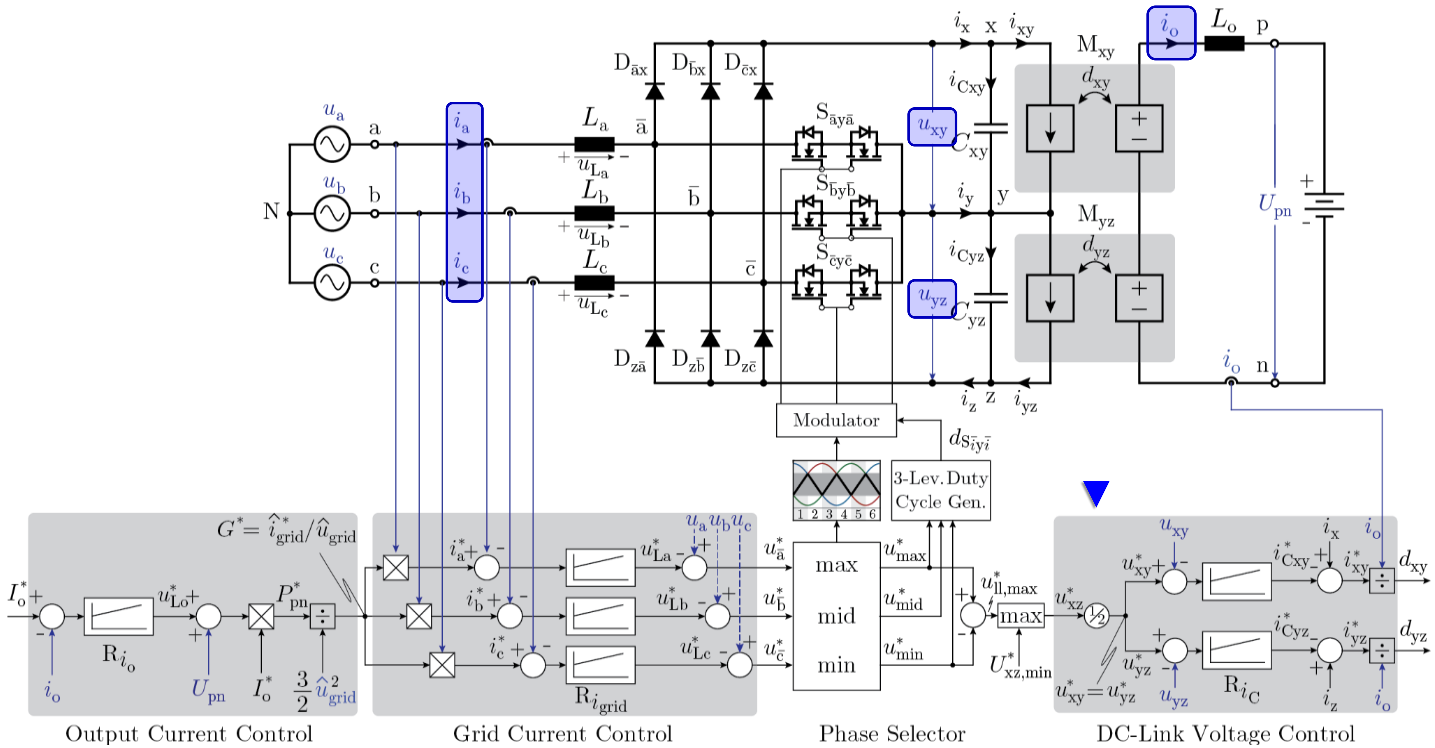
→ Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses



"Synergetic" Cascaded Control Structure

▶ "Synergetic" Control Structure

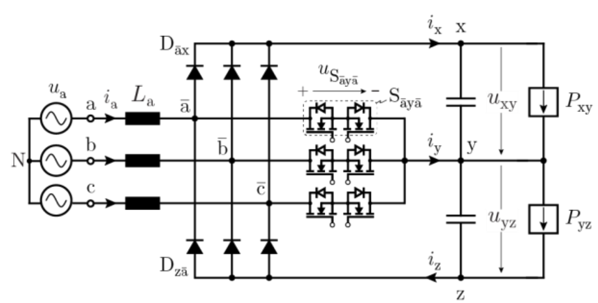
- *Cascaded Control of Output & Input Current (Direct & Through DC-Link Voltage)*
- *Active Equal DC-Link Voltage Splitting*

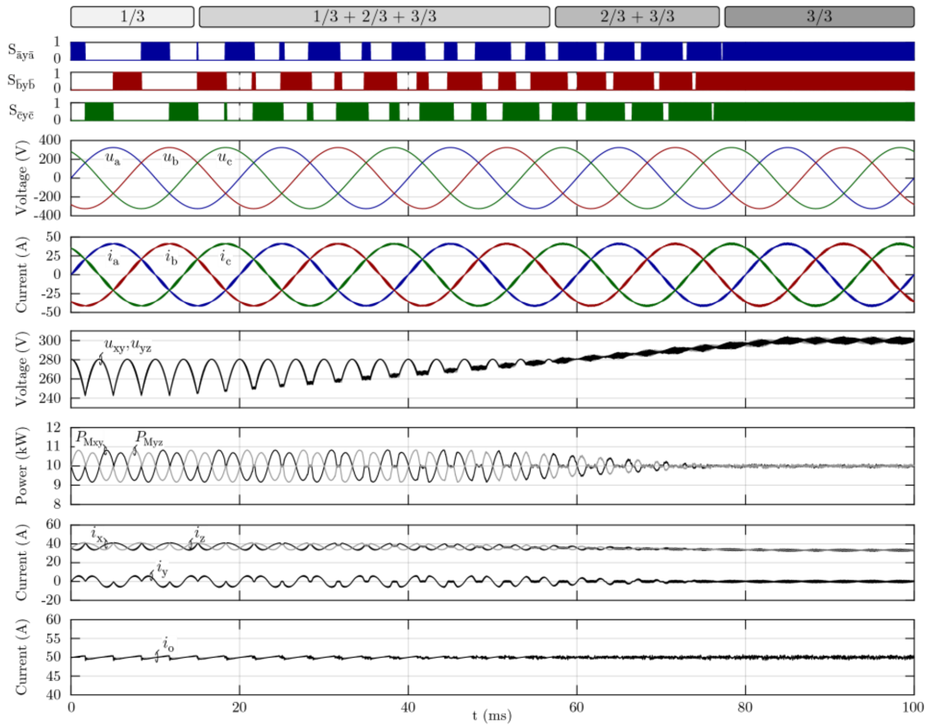


→ *Same Control Structure for 3/3-PWM (Full-Boost Mode) Using Diff. Ref. Values*

► AC/DC-Stage Transition to Full-Boost Operation

■ ***Different Operating Regimes*** → ***Synergetic*** | ***Partial-Boost*** | ***Full-Boost***

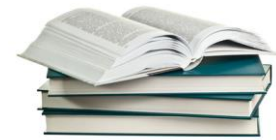




→ ***Intermediate 2/3-Operation for Limiting DC-Link Center Point Current (Low DC-Cap.)***

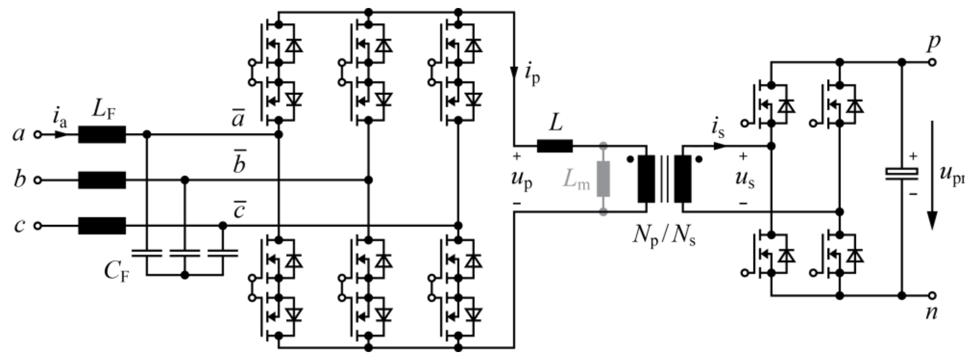
Isolated Single-Stage

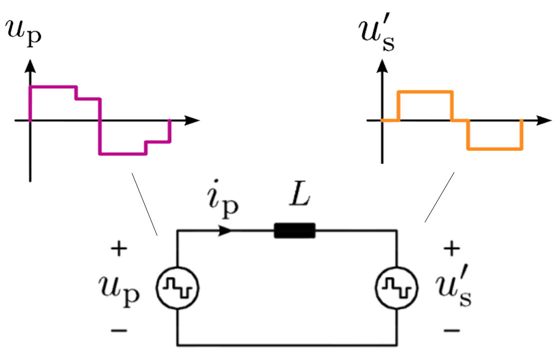
Matrix-Type Rectifier
D3AB-Rectifier

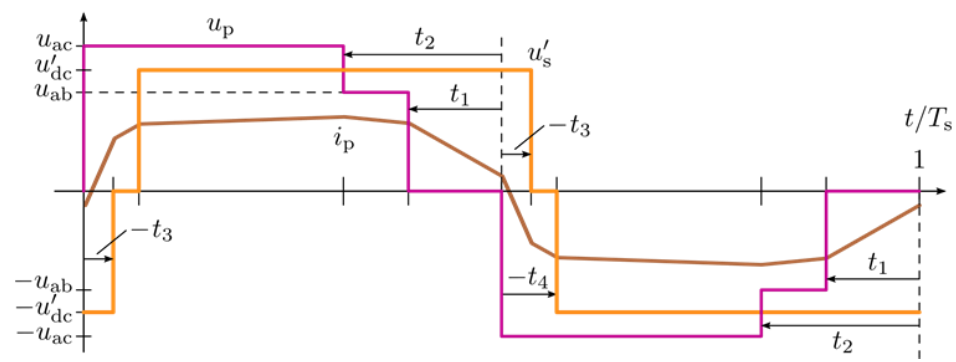


▶ *Isolated* Matrix-Type *PFC Rectifier (1)*

- *Based on Dual Active Bridge* (DAB) Concept
- Opt. Modulation ($t_1 \ldots t_4$) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation







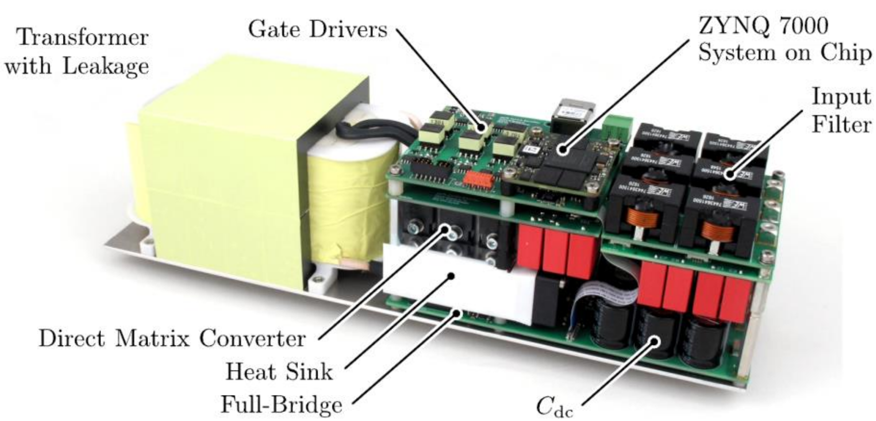
▶ Equivalent Circuit

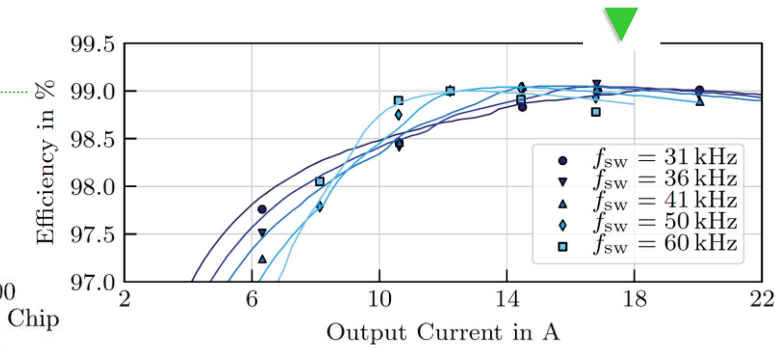
▶ Transformer Voltages / Currents

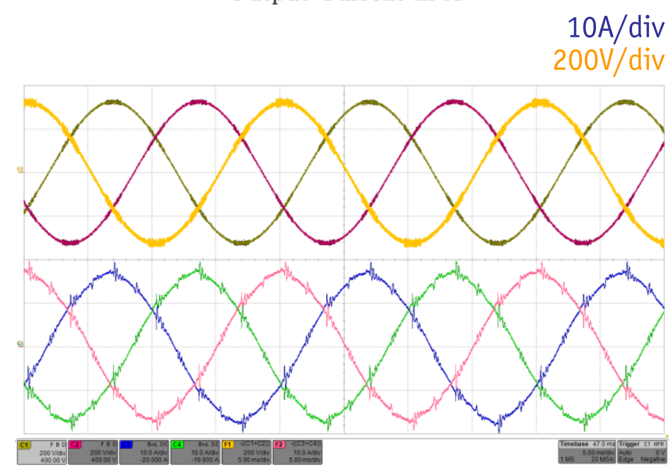
▶ *Isolated* Matrix-Type *PFC Rectifier (2)*

- Efficiency η = 98.9% @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW/dm}^3$

P_0= 8 kW
U_N= 400V_{AC} → U_0= 400V_{DC}
f_S = 36kHz





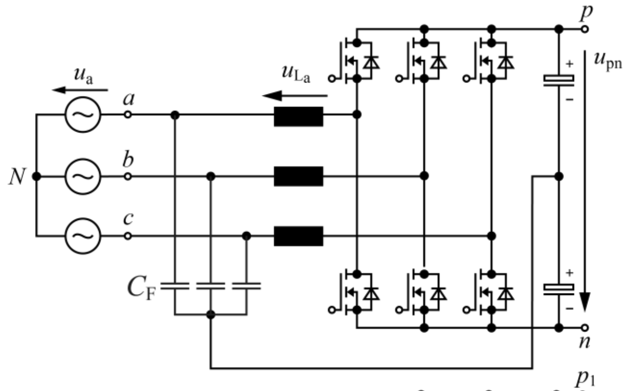


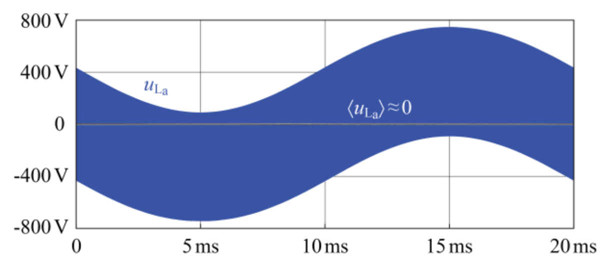
▶ 900V / 10mΩ SiC Power MOSFETs
▶ Opt. Modulation Based on 3D Look-Up Table

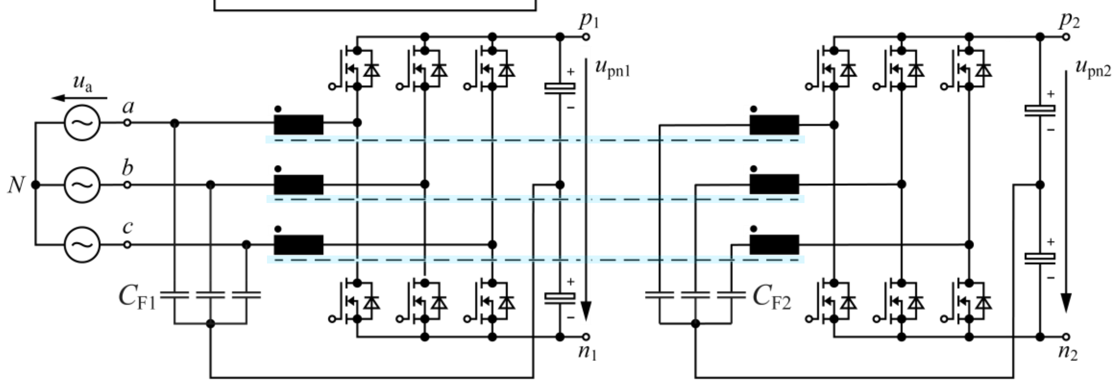
Isolated
Dual 3-Φ Active Bridge
Rectifier

▶ Dual 3-Φ Active Bridge PFC Rectifier (1)

- *HF-Components of Boost Ind. Voltages Utilized for Power Transfer*
- *Dual Active Bridge Concept*
- *ZVS*



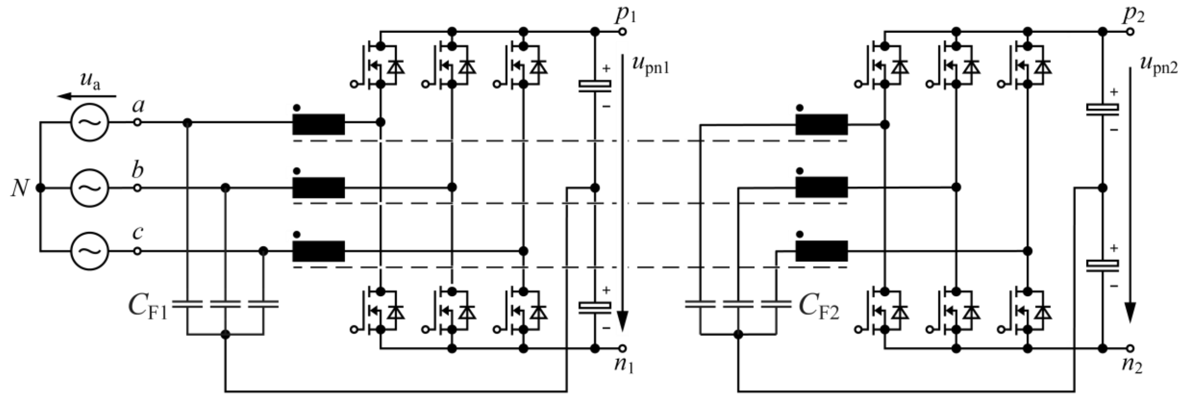


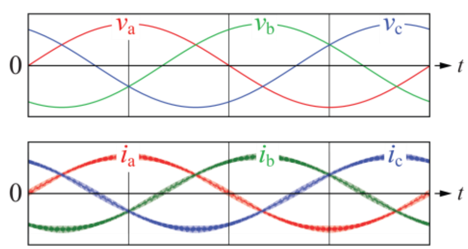


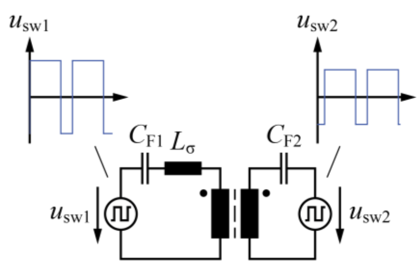
▶ *Three-Port System* - AC Input / Isol. DC Output / Non-Isol. DC Output

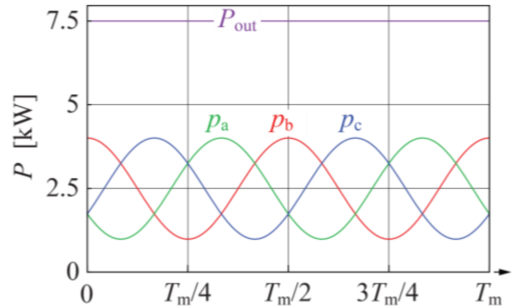
▶ Dual 3-Φ Active Bridge PFC Rectifier (2)

- *HF-Components of Boost Ind. Voltages Utilized for Power Transfer*
- *Dual Active Bridge Concept*
- *ZVS*









▶ *Three-Port System* - AC Input / Isol. DC Output / Non-Isol. DC Output

Conclusions

▶ Conclusions

■ **Future Need for „SWISS Knife"-Type Systems**

— Wide Input / Output Voltage Range
— Continuous / Sinusoidal Output Voltage
— Electromagnetically „Quiet" - No Shielded Cables
— On-Line Monitoring / Industry 4.0
— "Plug & Play" / Non-Expert Installation
— SMART Motors

Source: UK Outdoor Store

■ **Enabling Technologies**

— SiC / GaN
— Adv. (Multi-Level) Topologies incl. PFC Rectifier
— "Synergetic" Control
— Monolithic Bidirectional GaN
— Intelligent Power Modules
— Integration of Switch / Gate Drive / Sensing / Monitoring
— Adv. Modeling / Simulation / Optimization

■ **System Level →** Integration of Storage, Distributed DC Bus Systems, etc.

Thank You !