Gate Drive and Protection for SiC Devices

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The University of Tennessee, Knoxville

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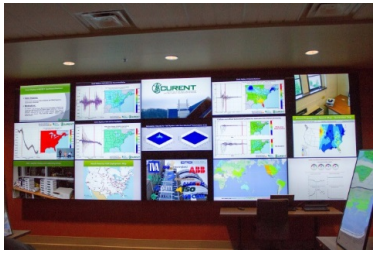
UTK Power Electronics

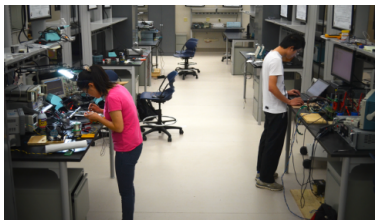
- Four full-time power electronics faculty (5th joining Jan. 2020)
  - Kevin Bai, Daniel Costinett, Leon Tolbert, Fred Wang, Helen Cui

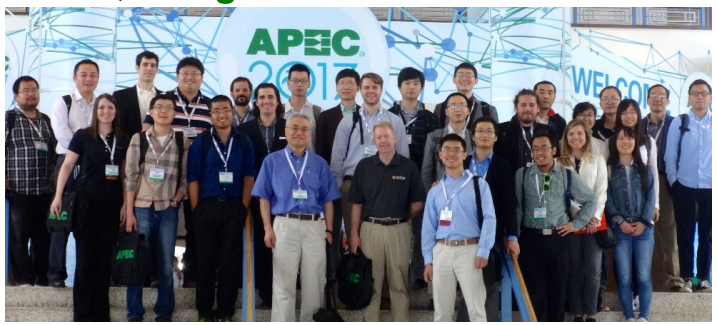






- 43 Graduate Students in Power Electronics at UTK
- CURENT is an NSF/DOE Engineering Research Center focused on grid of the future with high penetration of renewables: CURENT.utk.edu
- ~80 graduate students in CURENT at UTK
- Close collaboration with Oak Ridge National Laboratory (faculty have ORNL appointments and students participate in ORNL project)
- DOE WBG Graduate Traineeship: poTENNtial.eecs.utk.edu
- Focus on **hands-on**, **design-oriented** coursework and training



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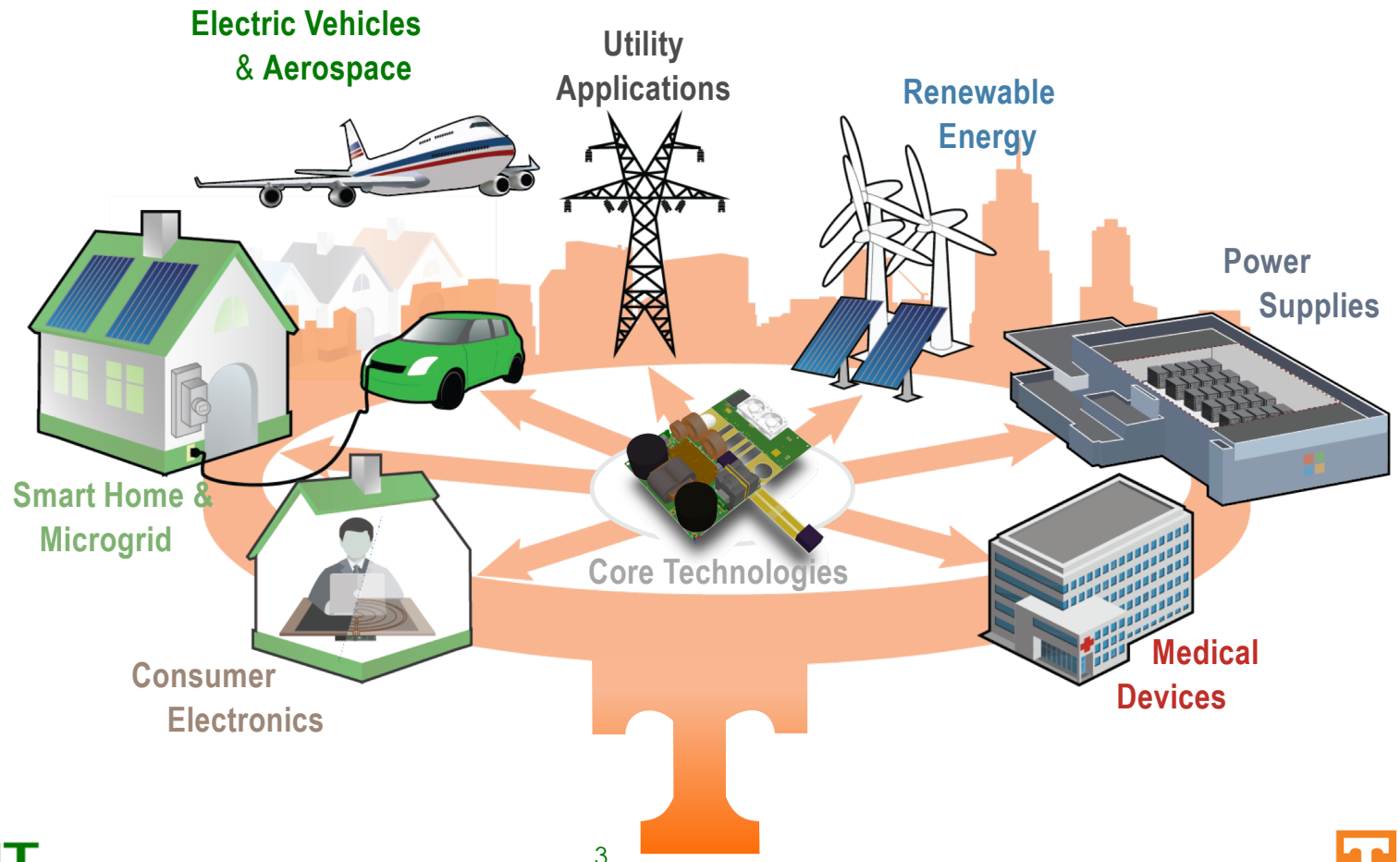
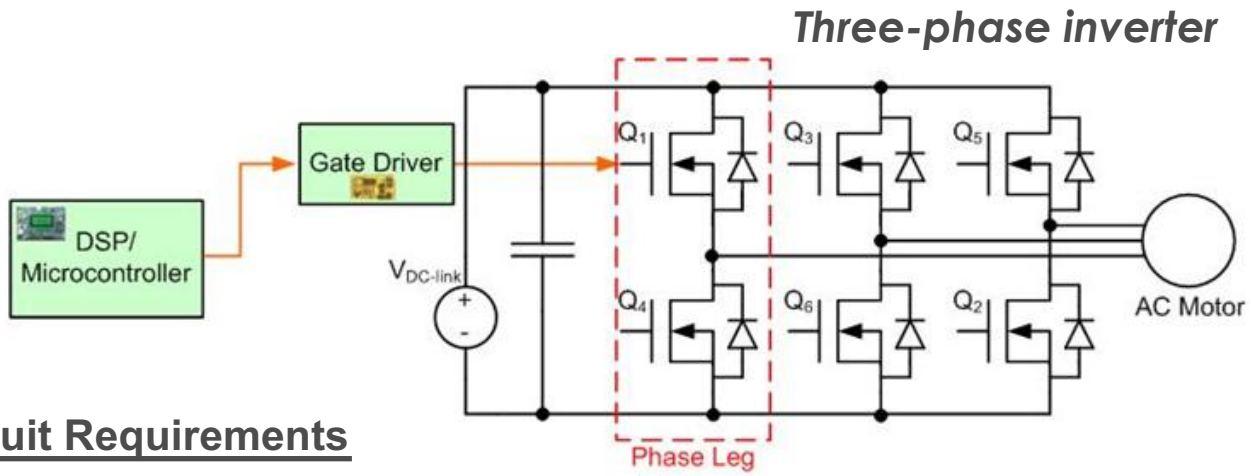
Power Electronics Research Applications



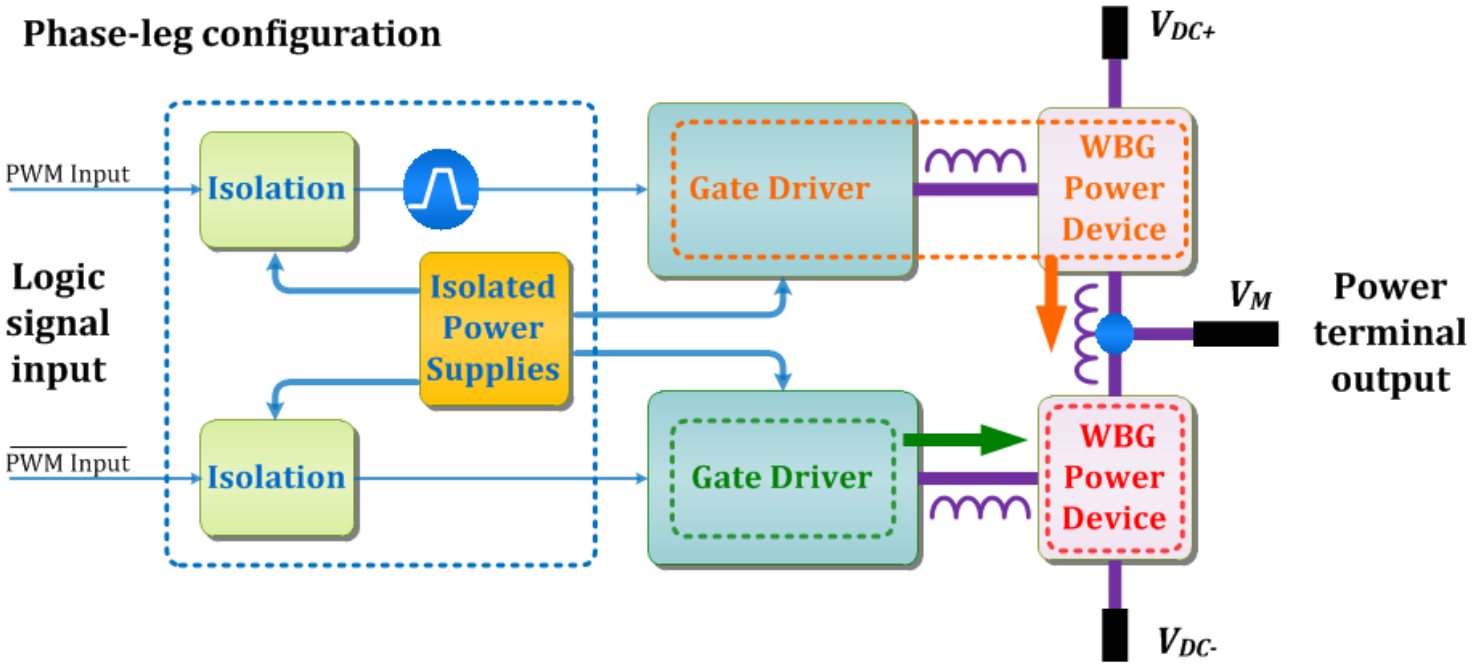
Role of Gate Driver Circuits



Gate Driver Circuit Requirements

- Interface between power devices and logic generators.
- Source and sink large drive current to minimize turn-ON and turn-OFF time to **minimize switching losses.**
- Provide enough voltage to minimize R_{ON} of power switches to **reduce conduction power loss**.
- Provide protection – clamp short circuit current and soft-turn off capability

Key Factors Limiting Switching Speed



- **High switching-speed performance of the lower switch is limited by:**
  - Gate driver capability
  - Interference from the upper switch
  - Parasitics
  - *dv/dt* immunity of isolator & power supply

Outline

- Short circuit capability and protection needs in SiC MOSFETs
- Role of parasitics in phase leg with SiC MOSFETs
- Gate drives for series-connected SiC MOSFETs
- Gate drives for 10 kV SiC MOSFETs
- Need for current-driven gate drives in SiC MOSFETs

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Protection in SiC MOSFETs

Overcurrent protection of SiC MOSFETs is more challenging compared to Si devices:

1. Lower short circuit withstand capability

- Smaller chip area and higher current density have direct negative impacts
- SiC MOSFETs present significantly lower ruggedness and robustness under short-circuit condition due to positive temperature coefficient of channel mobility

2. Poor long term stability, e.g. gate oxide degradation, electromagnetic migration

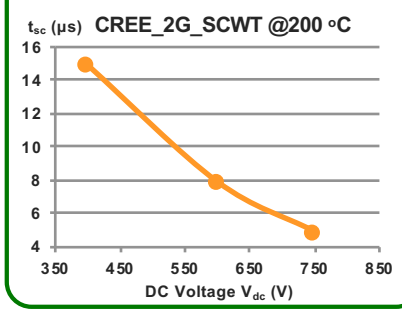
- Significant degradation resulting from Fowler–Nordheim tunneling current into the dielectric is evident under overcurrent condition
- Even pulsed overcurrent operation at room temperature also results in degradation due to high junction temperature induced electron trapping
- Low channel mobility of SiC MOSFETs requires higher positive gate bias (+20 V), i.e. higher gate electric field, and further worsens the degradation under overcurrent condition

Protection circuit should respond to a fault as fast as possible to avoid potential destruction and/or degradation.

Requirements for Short Circuit Protection of SiC MOSFETs

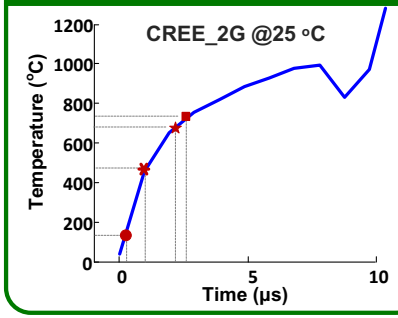
Requirements for Active Protection Schemes

Single-event Short Circuit



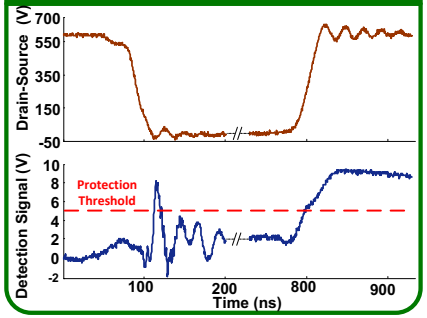
- ✓ Fault response time (Δt) less than the lowest short circuit withstand time, i.e. Δt < 5 μs

Repetitive Short Circuit



- ✓ Δt < 2 μs for metallization layer reliability
- ✓ Δt < 1 μs for ohmic contact and passivation reliability
- ✓ Δt < 300 ns for gate oxide reliability

Noise Immunity

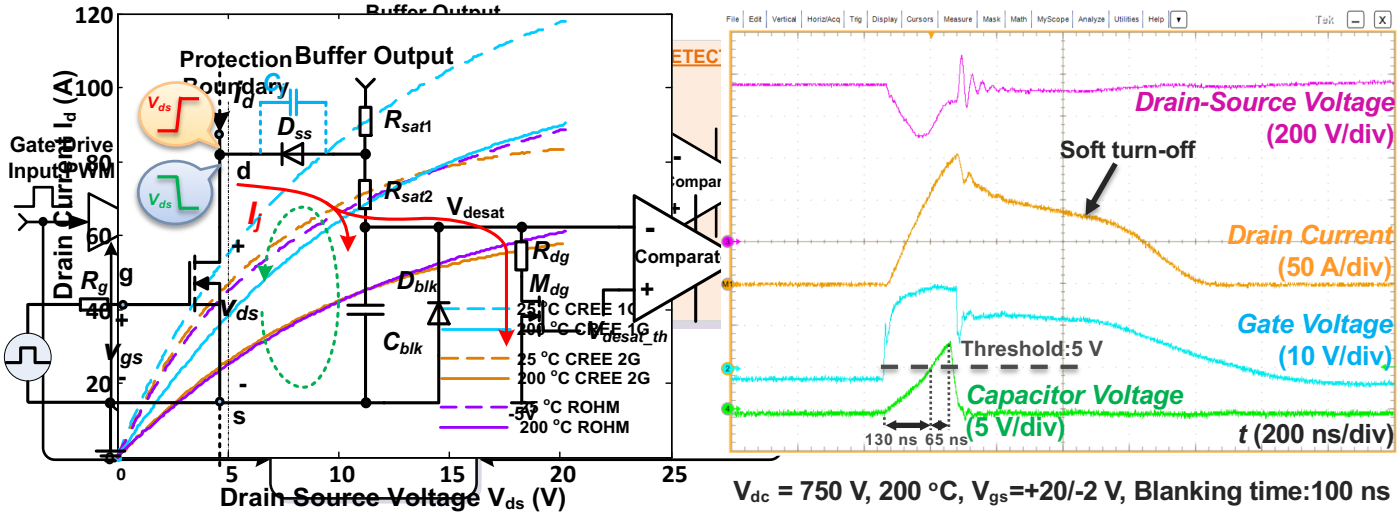


- ✓ No false triggering during fast switching transient
- ✓ No false triggering under different conditions (low gate resistance, high temperature, etc.)

Desaturation Technique

Key Design Consideration:

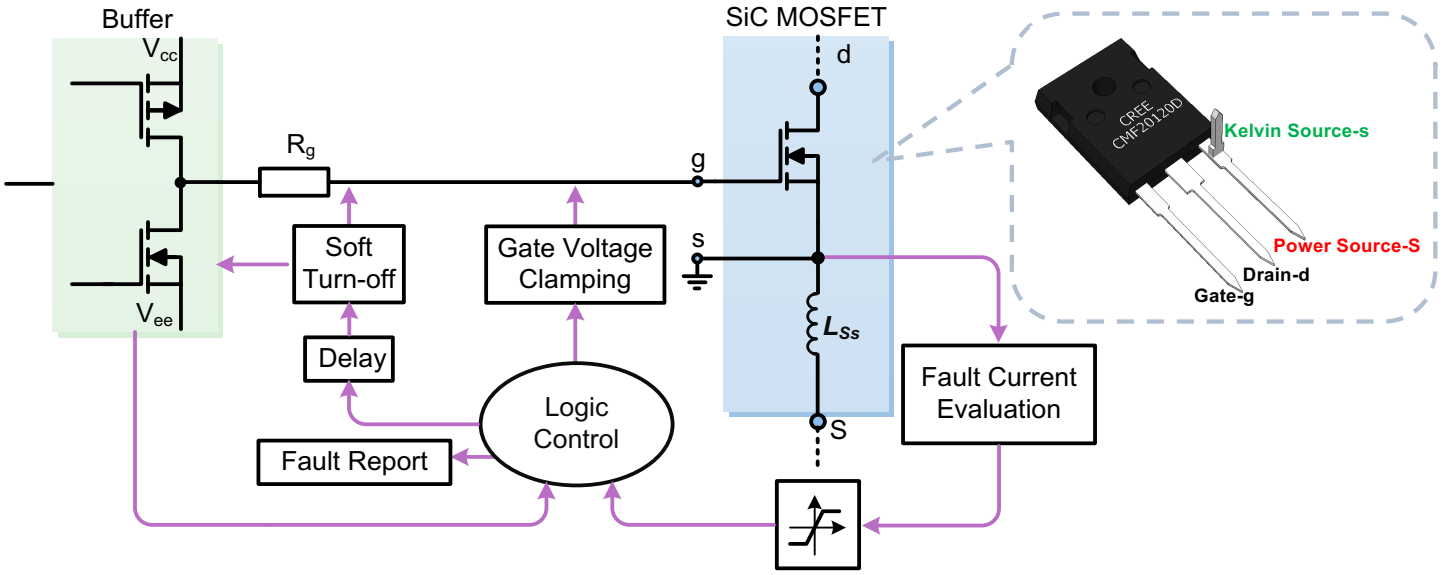
- Commercial Si IGBT/MOSFET gate drivers usually have slow fault response time (>3 µs) ⇒ Minimum allowable response time to avoid potential device degradation
- Proper blanking time considering the trade off between fault response time and noise immunity
- Proper protection threshold based on temperature dependent output characteristics



V_{dc} = 750 V, 200 °C, V_{gs}=+20/-2 V, Blanking time:100 ns

Active Protection Scheme

An active protection scheme without blanking time and with strong noise immunity!



Proposed fault current evaluation protection scheme

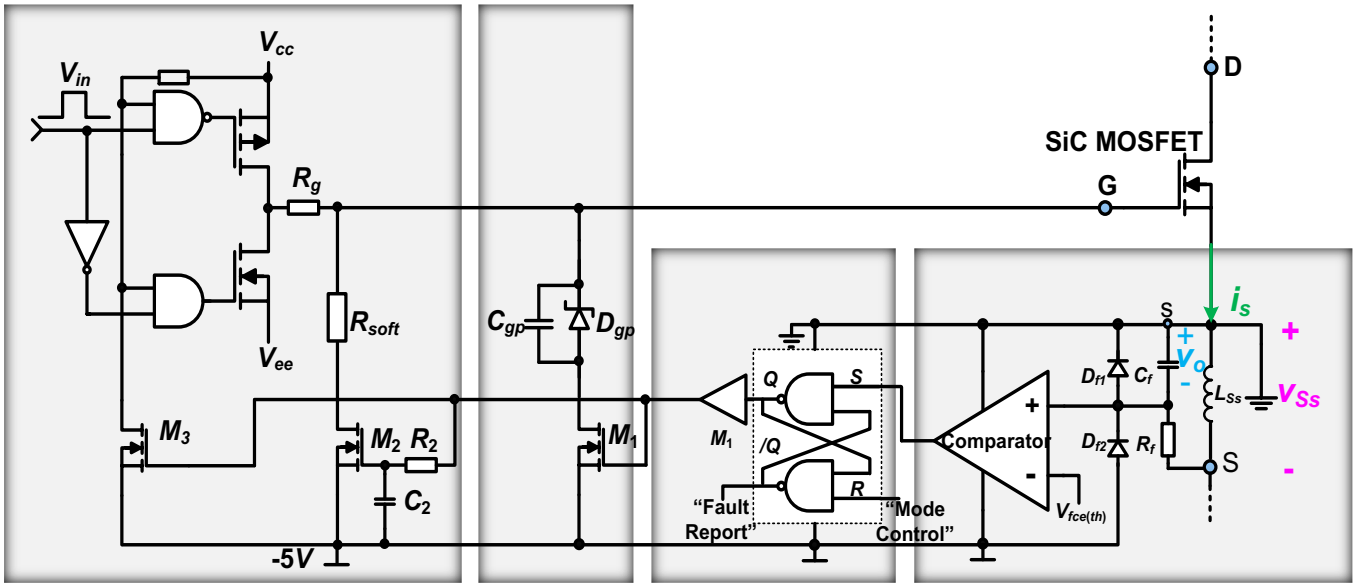
Fault Current Evaluation: *Detect an overcurrent/short circuit fault by di/dt monitoring*

Logic Control: *Activate/Deactivate the protection circuit and protection mode control*

Gate Voltage Clamping: *Limit the transient short circuit current*

Soft Turn-off: *Suppress the voltage overshoot during turn-off transient*

Operating Principle



Operating Principle:

M3 : Clamp the gate driver output to be low

- M_3 is turned on following a delay to guarantee fault current is stably clamped

R_{soft}: Increase gate resistance to reduce turn-off overvoltage

- M_2 is turned on after the input PWM signal is blocked

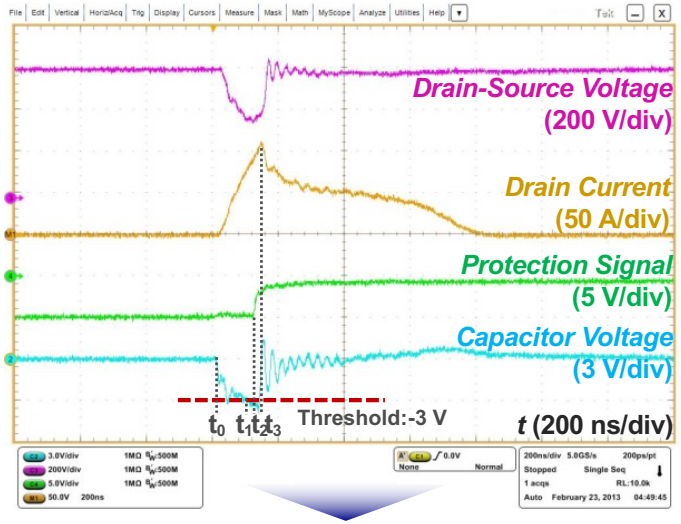
$(s) \cdot \frac{C_f R_f}{L_{Ss}}$

voltage

Fault Current Evaluation–Testing Results

V_{dc}= 600 V; $V_{fce(th)}$ = -3 V; R_f = 200 Ω; C_f = 1 nF

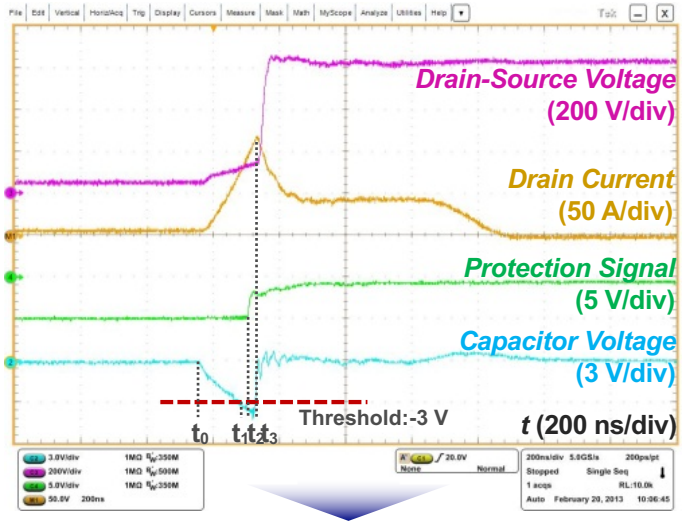
Hard Switching Fault (HSF)



Total protection delay-(140 ns)

1. **Detection delay (t_0~t_1):** 100 ns
2. **Comparator response delay (t_1~t_2):** 15 ns
3. **Total Logic control delay (t_2~t_3):** 25 ns

Fault Under Load (FUL)



Total protection delay-(170 ns)

1. **Detection delay (t_0~t_1):** 130ns
2. **Comparator response delay (t_1~t_2):** 15 ns
3. **Total Logic control delay (t_2~t_3):** 25 ns

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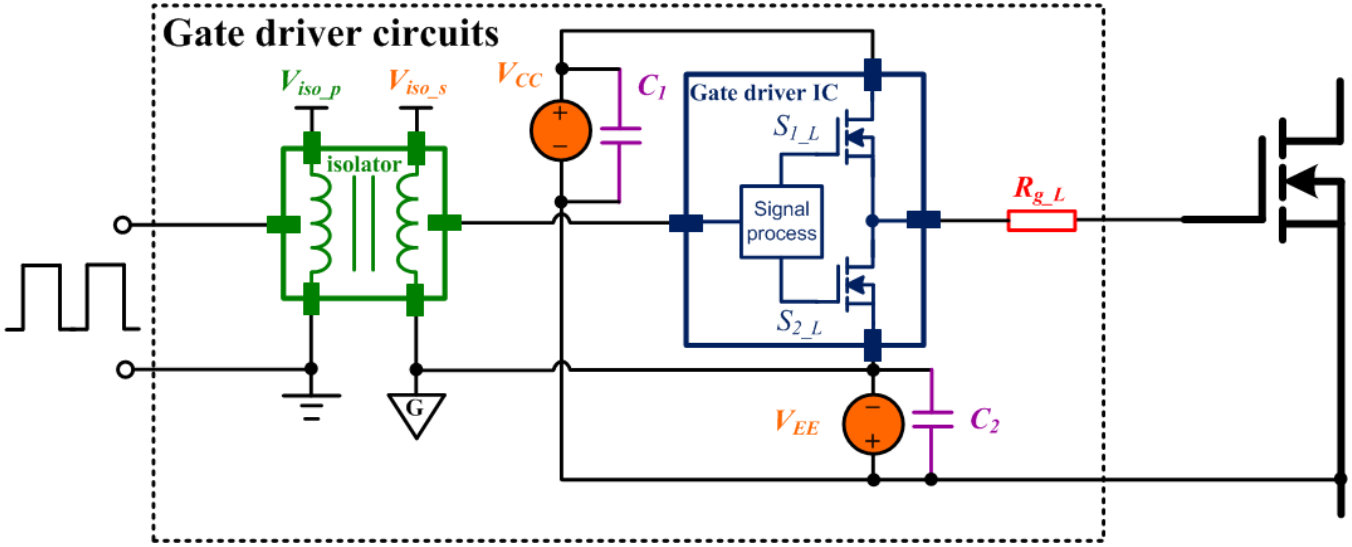
Gate Driver for SiC MOSFETs

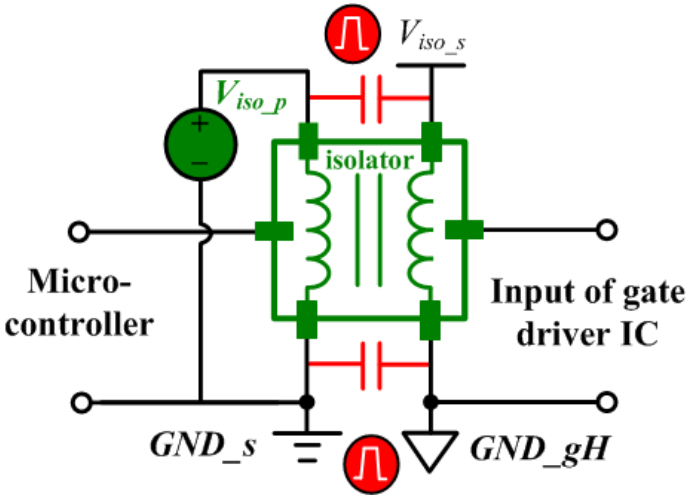


1. Signal isolator
2. Isolated power supply
3. Decoupling capacitors
4. Gate driver IC
5. Gate resistor

[1] P. J. Grbovic, "Advanced power semiconductors: art of control, from theory to practice," 2013.
[2] Z. Zhang and F. Wang, "Driving and Characterization of wide bandgap semiconductors for voltage source converter applications," 2014.

CMTI for Signal Isolator

- **Common mode transient immunity (CMTI)**
  - Switching transitions cause high *dv/dt* across the signal isolator
  - Coupling capacitances offer parasitic paths
  - *dv/dt* coupled through these parasitic paths leads isolator to lose control by inadvertently triggering a function or causing false feedback.



- **Typical *dv/dt* for wide bandgap switches**
  - SiC discrete switch (Wolfspeed CMF20120D): ~ 30 kV/μs
  - SiC power module (Wolfspeed CPM212000025B): ~ 80 kV/μs
  - GaN e-mode HFET (GaN Systems GS66508P): ~ 200 kV/μs

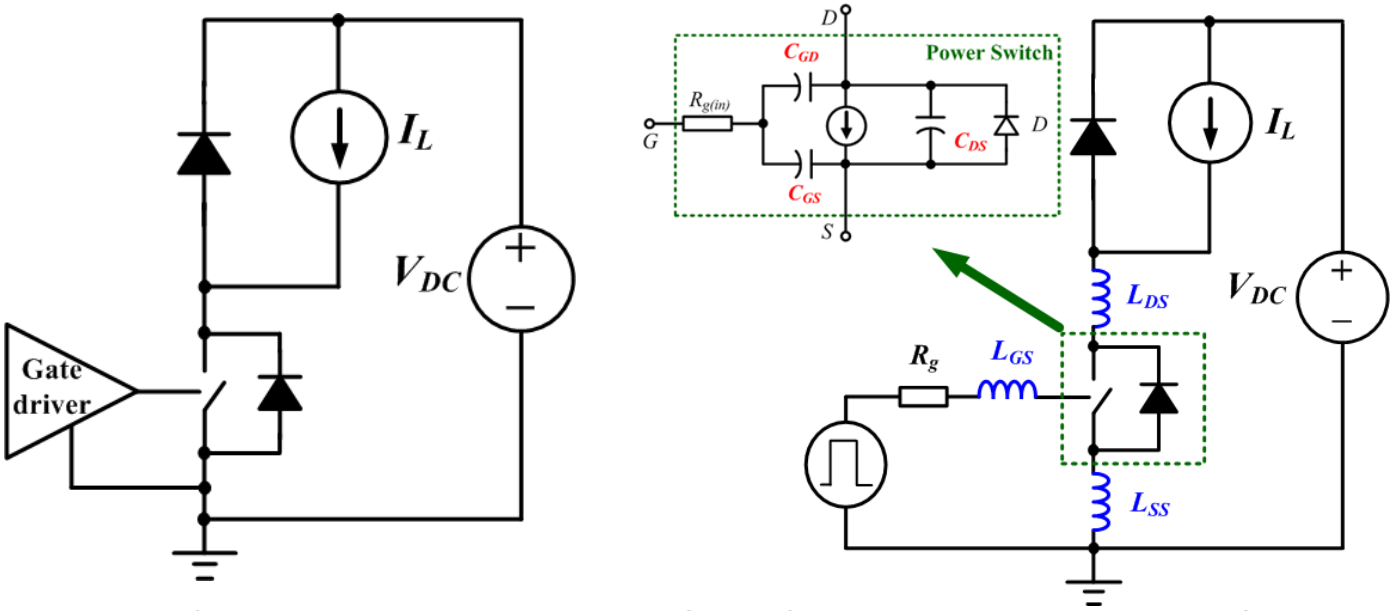
- **Commercially available signal isolators**

	Opto-coupler [1]	Capacitive [2]	Transformer [3]	RF-based [4]
Minimum CMTI	30 kV/μs	15 kV/μs	25 kV/μs	200 kV/μs

- **PCB traces on input side of isolator may also couple some noise**
  - Simple low-pass filter can be easily added to input of isolator with a small capacitor in the pF range.

[1] http://www.avagotech.com/docs/AV01-0193EN [2] http://www.ti.com/lit/ds/symlink/iso721-q1.pdf
[3] http://www.analog.com/media/en/technical-documentation/data-sheets/ADUM5240_5241_5242.pdf
[4] http://www.silabs.com/products/power/isodrivers/Pages/default.aspx

Parasitics in the Switching Loop



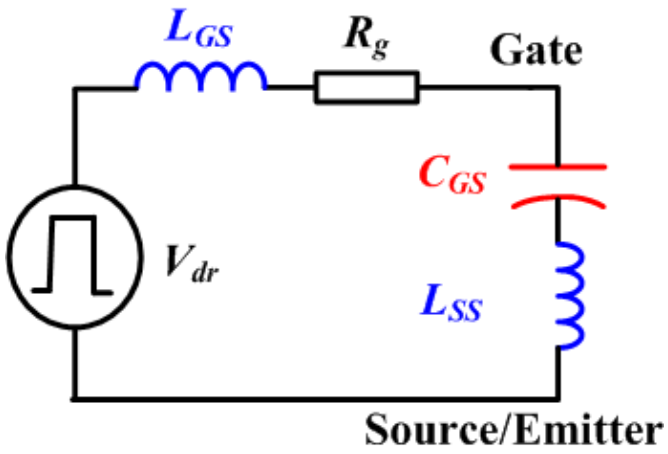
Ideal simplified switching test circuit *Simplified switching test circuit w/ parasitics*

- Parasitic inductances: gate loop inductance L_{GS}, power loop inductance L_{DS}, common source inductance L_{SS}
- Parasitic capacitances: gate-source capacitance C_{GS}, drain-source capacitance C_{DS}, Miller capacitance C_{GD}

[1] Z. Chen, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," 2010.

Parasitics in the Gate Loop

- Gate loop inductance L_{GS} and gate-source capacitance C_{GS} are two parasitics in the gate loop
  - C_{GS} determines the time constant of the gate circuit
  - L_{GS} resonates with input capacitance of devices, causing parasitic ringing in the gate loop

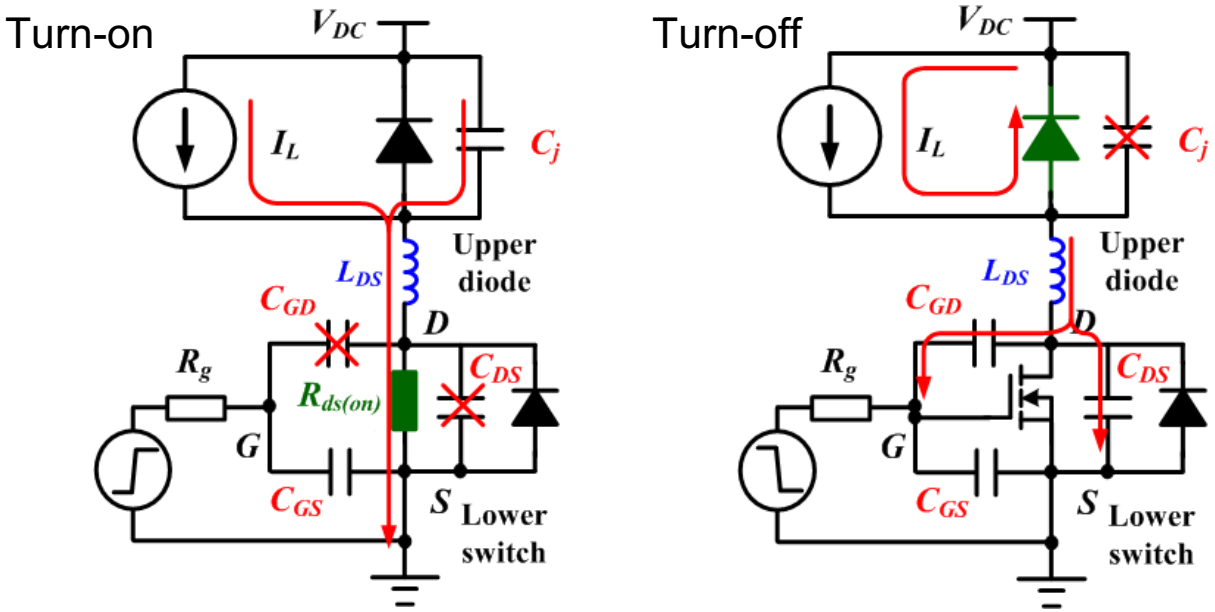


- Higher C_{GS} reduces slew rate of gate voltage
  - Switching delay: increase
  - di/dt: decrease
  - Switching losses: increase
- Higher L_{GS} causes more ringing in gate loop w/ limited impact on power loop
  - Switching delay: increase
  - di/dt, dv/dt: no change
  - Switching losses: no change

[1] Z. Chen, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," 2010.

Parasitics in the Power Loop

- Power loop inductance L_{DS}, drain-source capacitance C_{DS}, and junction capacitance C_j are three parasitics in the power loop

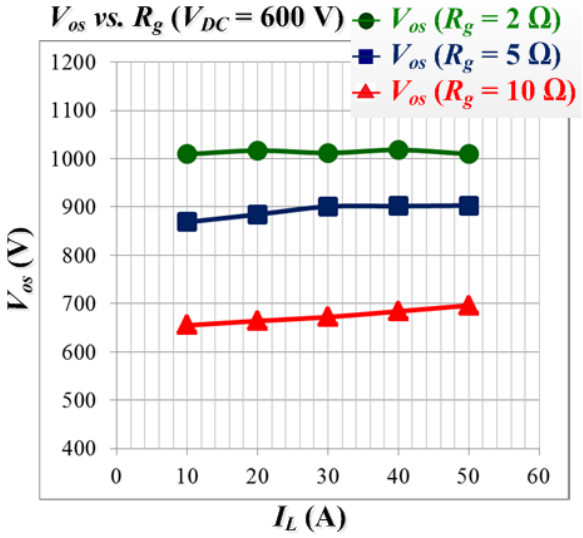


- Turn-on transient, ringing is caused by resonance between C_j & L_{DS}
- Turn-off transient, ringing is caused by resonance between C_{OSS}* & L_{DS}

* C_{OSS}: C_{DS} + C_{GD}

Impact of Power Loop Parasitics on Switching Behavior

- For wide band-gap switches, the overshoot voltage and parasitic ringing become worse, due to:
  - High *dv/dt* & *di/dt* induced by fast switching speed
  - Small damping factor considering small ON state resistance
  - Small parasitic capacitance C_{oss} because of small die area



Overshoot voltage vs. R_g (SiC power module)

- Accordingly, power loop inductance L_{DS} is more sensitive in terms of its effect on parasitic ringing and overshoot voltage

[1] Z. Zhang, "Understanding the limitations and impact factors of wide bandgap devices' high switching-speed capability in a voltage source converter", 2014.

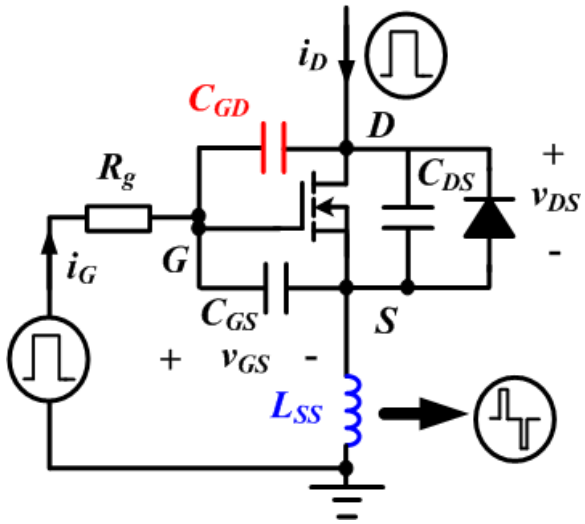
Mutual Parasitics in Both Power Loop & Gate Loop

- Common source inductance L_{SS} and Miller capacitance C_{GD} are two mutual parasitics in both power loop & gate loop
  - L_{SS} serves as a negative feedback from the power loop to the gate loop due to *di/dt* and its induced gate voltage

$$V_{LSS} = L_{SS}\frac{di_D}{dt} = L_{SS}\frac{di_D}{di_G}\times\frac{di_G}{dt}$$

  - C_{GD} serves as a negative feedback from the power loop to the gate loop due to *dv/dt* and its induced gate current

$$I_{CGD} = C_{GD}\frac{dv_{DS}}{dt} = C_{GD}\frac{dv_{DS}}{dv_{GS}}\times\frac{dv_{GS}}{dt}$$

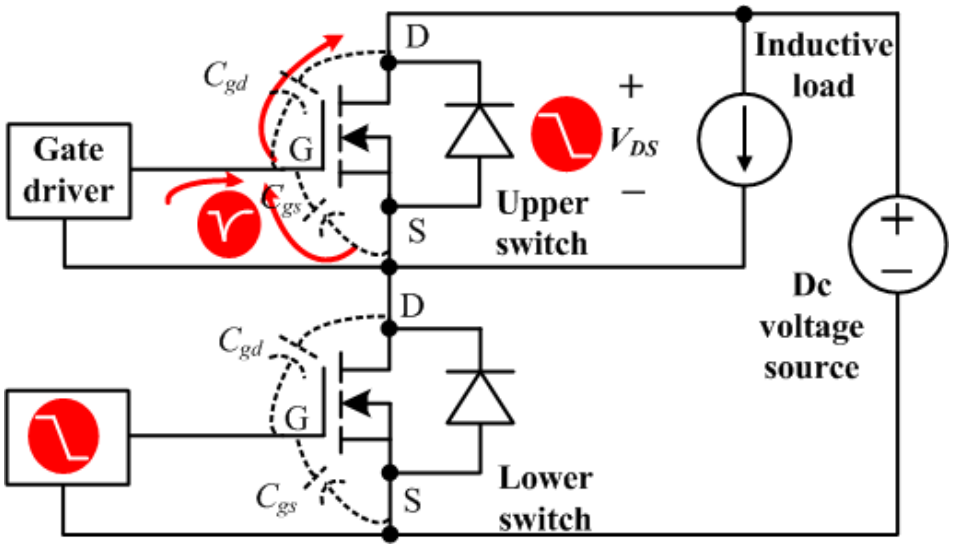


- L_{SS} and C_{GD} in both gate loop and power loop
  - Cause interference between the power stage and control circuit
  - Negatively impact the switching speed, leading to more switching losses

Layout Design Criteria for Parasitics Minimization

- For power device related parasitics, including C_{GS}, C_{DS}, C_{GD}
  - Avoid adding additional equivalent parasitics externally, especially for Miller capacitance due to its high sensitivity on the switching performance.
- For interconnection related parasitics, including L_{GS}, L_{DS}, L_{SS}
  - Minimize as much as possible
- For parasitics coupled between power stage and signal stage, e.g., coupling capacitance of signal isolator and isolated power supply
  - Minimize as much as possible

Mechanism Causing Cross-Talk



Phase-leg configuration

Turn-on transient → Positive spurious gate voltage ↑ → Shoot-through current

Cdv/dt ↑ → **worse**

Turn-off transient → Negative spurious gate voltage ↑ → Overstress gate terminal

Cross-Talk for WBG Switches

Characteristics of Several Comparable Power Devices

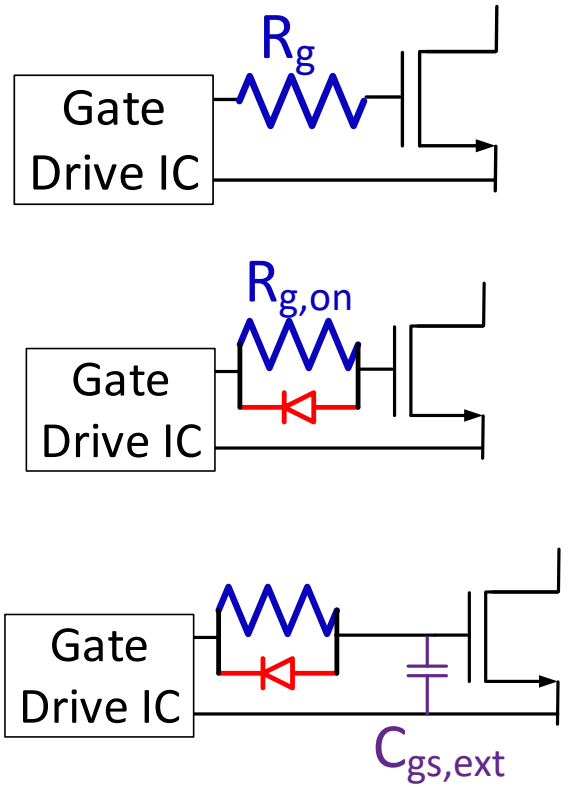
Type	Manufacturer	Model	V_{DS} / I_D (100 °C)	Q_{gs}	$V_{gs(th)}$ (25 °C)	$V_{gs\_max(-)}$
Si IGBT	IR	IRGP20B120U	1200 V / 20 A	169 nC	4.5 V	-20 V
Si MOSFET	Microsemi	APT34M120J	1200 V / 22 A	560 nC	4.0 V	-30 V
SiC MOSFET	CREE	C2M0080120D	1200 V / 20 A	49.2 nC	2.2 V	-10 V
GaN HFET	GaN Systems	GS66508P	650 V / 30 A	2.1 nC	1.4 V	-10 V

- **Properties of SiC & GaN devices**
  - Faster switching speed
  - Lower threshold voltage
  - Lower maximum allowable negative gate voltage
- WBG devices in a phase-leg configuration are easily affected by cross-talk, leading to extra switching losses & reliability issues

Passive Cross-Talk Suppression

To suppress cross-talk, we need to minimize spurious V_{gs_H} :

- Higher/lower symmetric R_g
  - Higher R_g reduces *dv/dt* but may actually increase cross-talk loss, in addition to turn-on and turn-off overlap losses
  - Lower R_g may improve or worsen cross-talk, because *dv/dt* will increase
- Asymmetric $R_{g,on}$
  - Higher turn-on R_g reduces *dv/dt*, but increases turn-on overlap loss
  - Likely to reduce cross-talk, but may increase overall turn-on loss
- Added parallel C_{gs}
  - Reduces *dv/dt*, but increases turn-on and turn-off overlap losses, as well as driving loss
  - May reduce cross-talk, but may increase overall loss

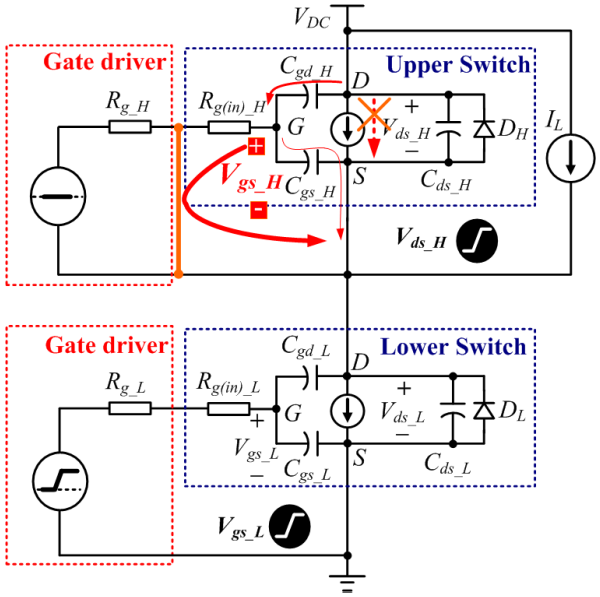


Active Cross-Talk Suppression Circuits

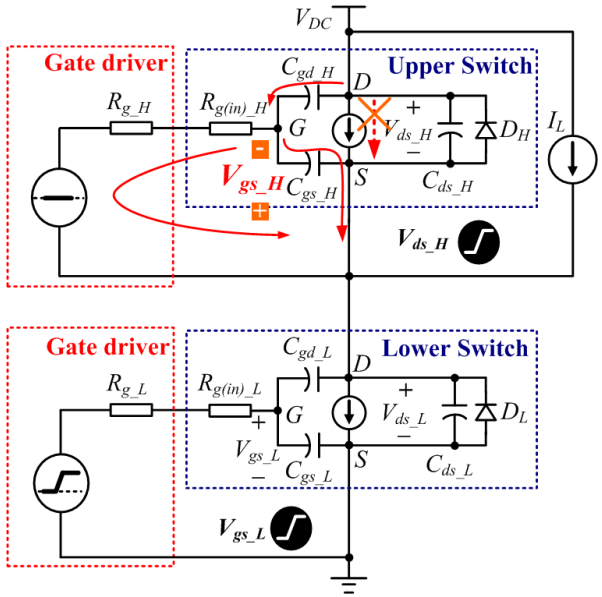
To suppress cross-talk, we need to minimize spurious V_{gs_H}:

- Reduce gate loop impedance during the switching transient
- Pre-charge the gate-source capacitance before the switching transient

Gate impedance regulation (GIR) assist circuit



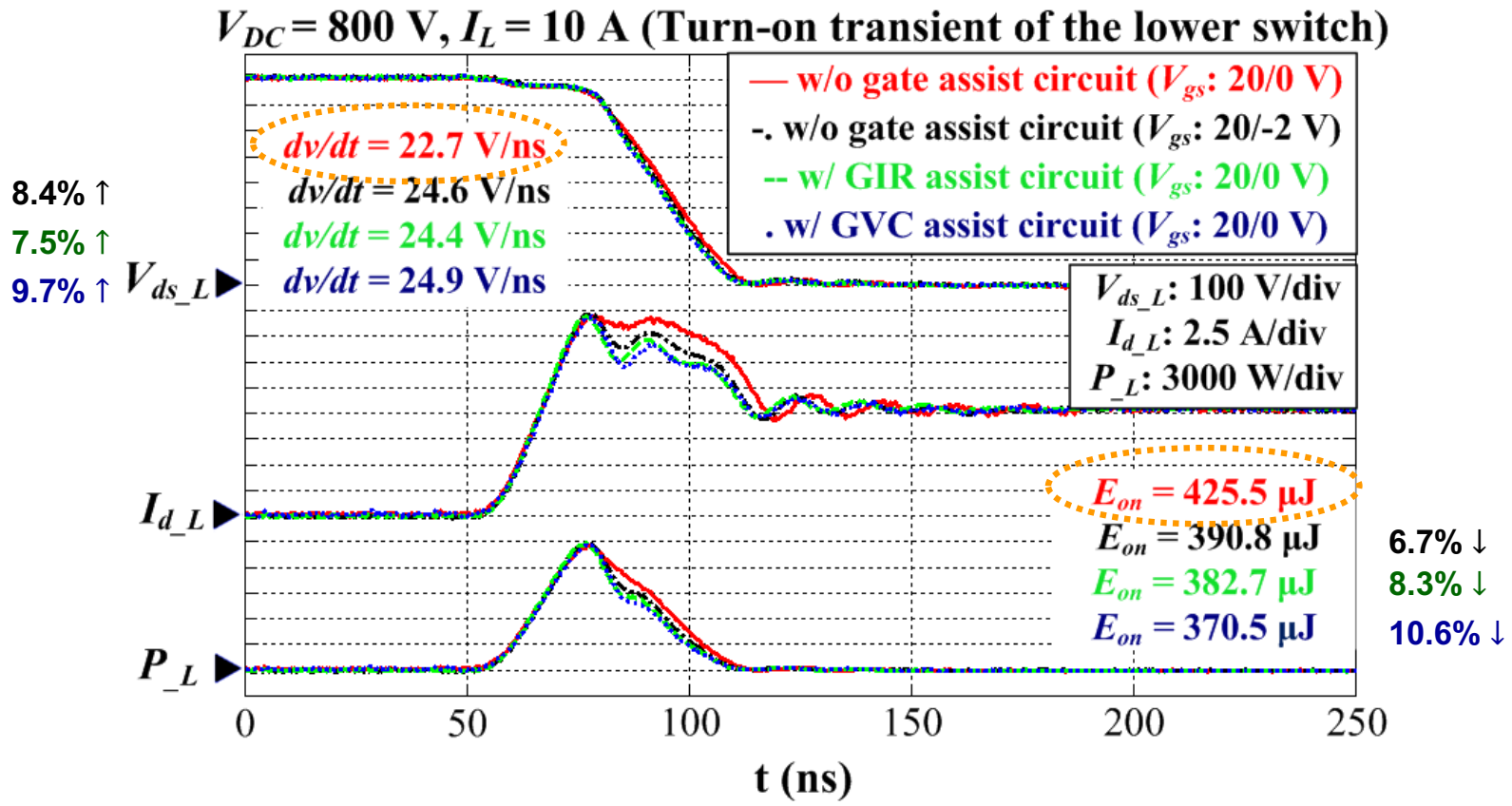
Gate voltage control (GVC) assist circuit



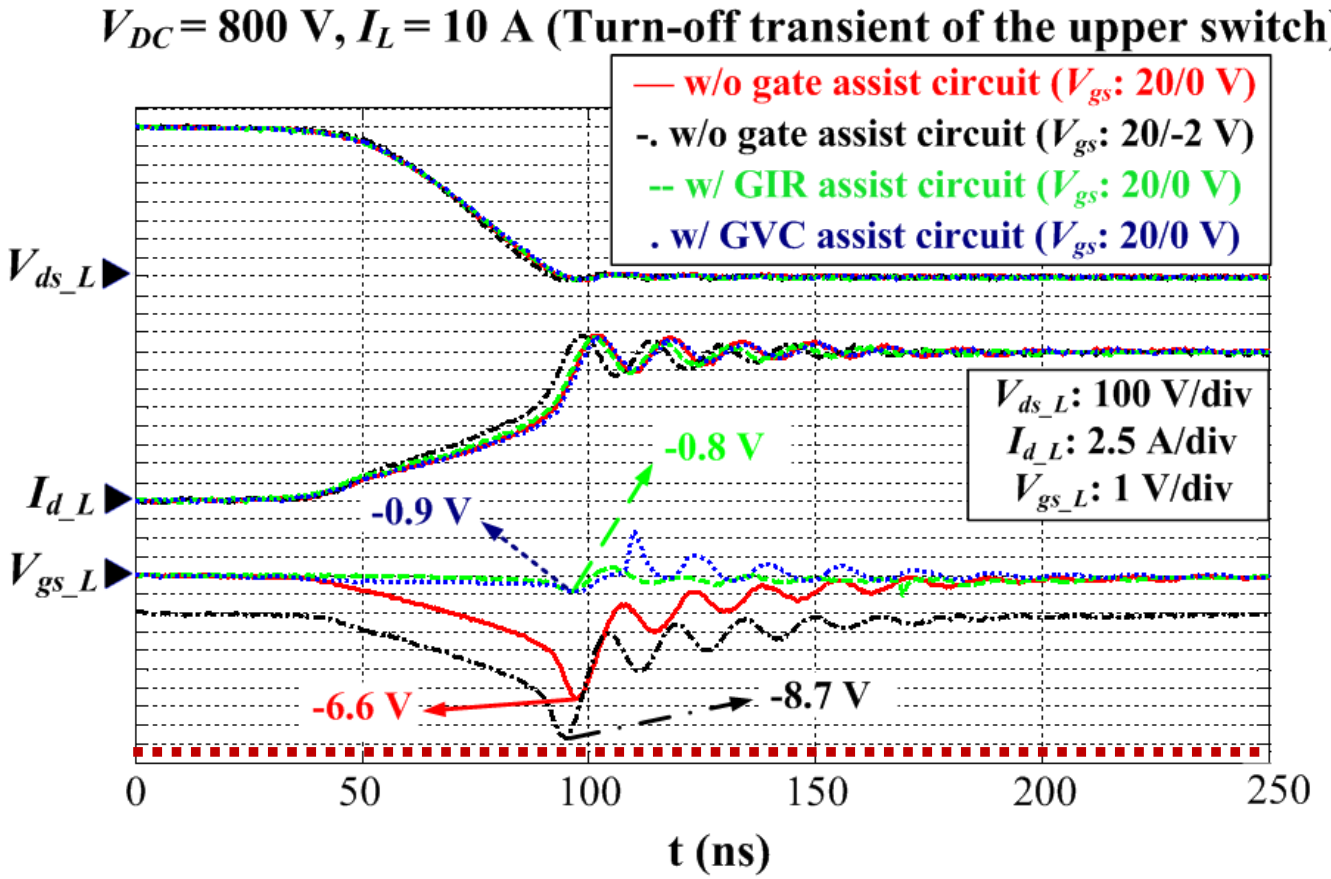
(Turn-on transient of lower switch as an example)

[1] Zheyu Zhang, "Active gate driver for cross talk suppression of SiC power devices in a phase-leg configuration", 2014.

Turn-on Transient of the Lower Switch



Turn-off Transient of the Upper Switch



[1] Zheyu Zhang, "Active gate driver for cross talk suppression of SiC power devices in a phase-leg configuration", 2014.

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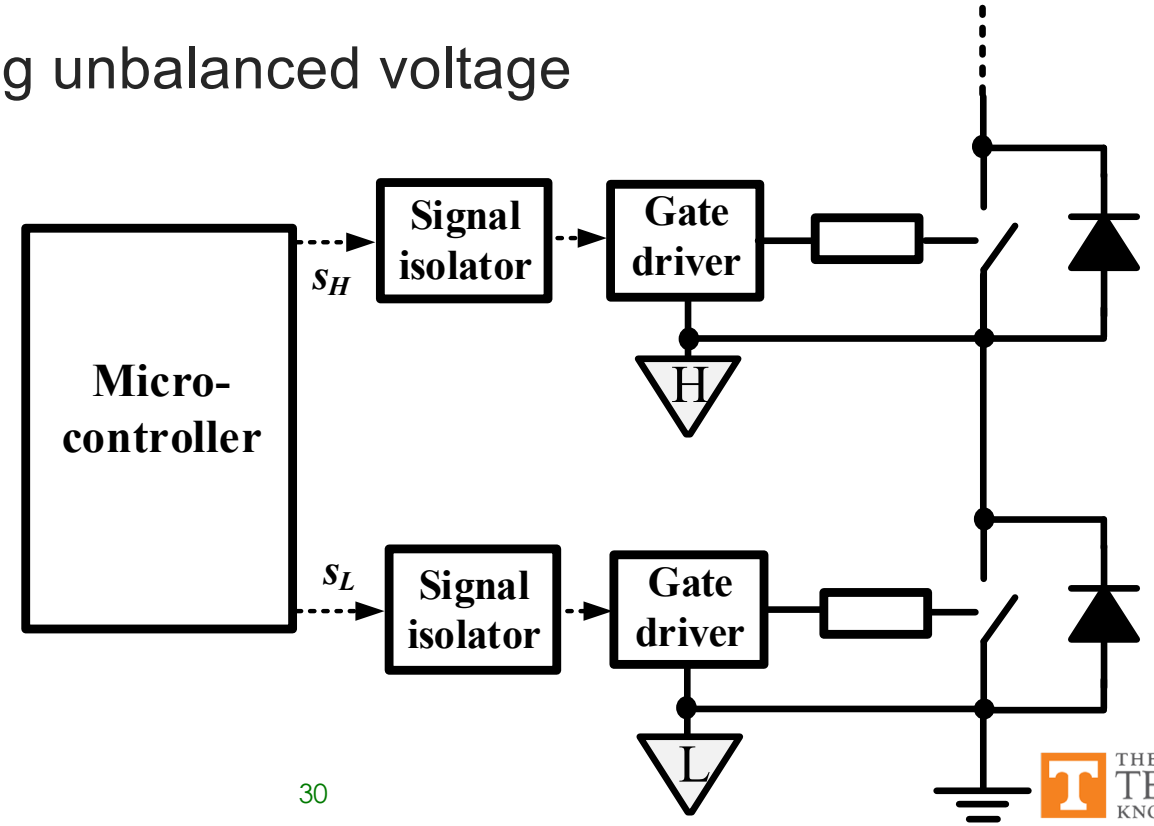
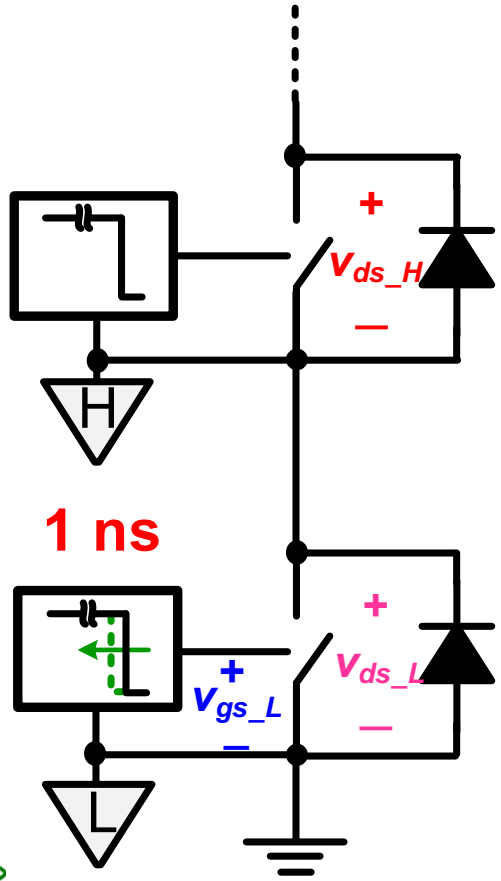
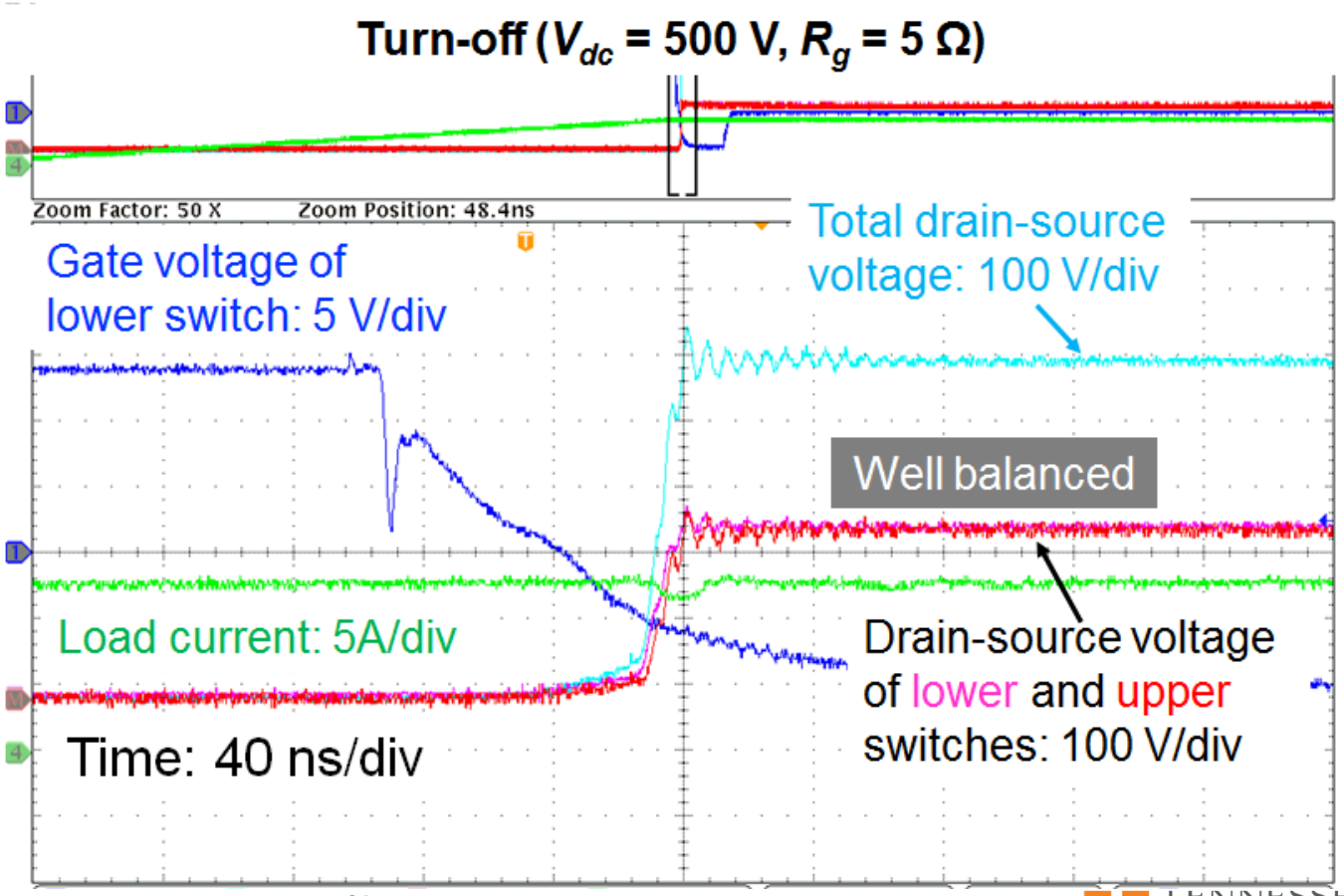
Challenges for Series-Connected SiC MOSFETs

- Voltage unbalance, especially during the fast switching transition, is challenging
- Mechanisms causing unbalanced voltage
  - Gate drive signal asymmetry
  - Device parameters mismatch
  - Parasitics mismatch

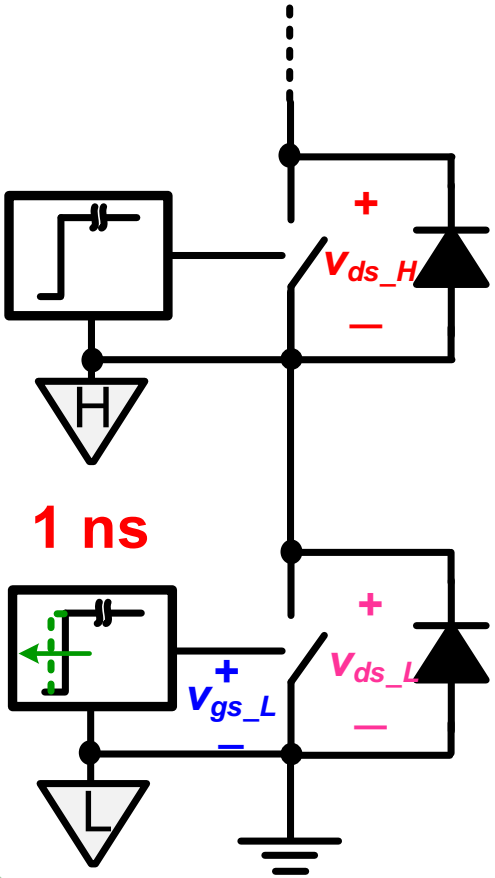


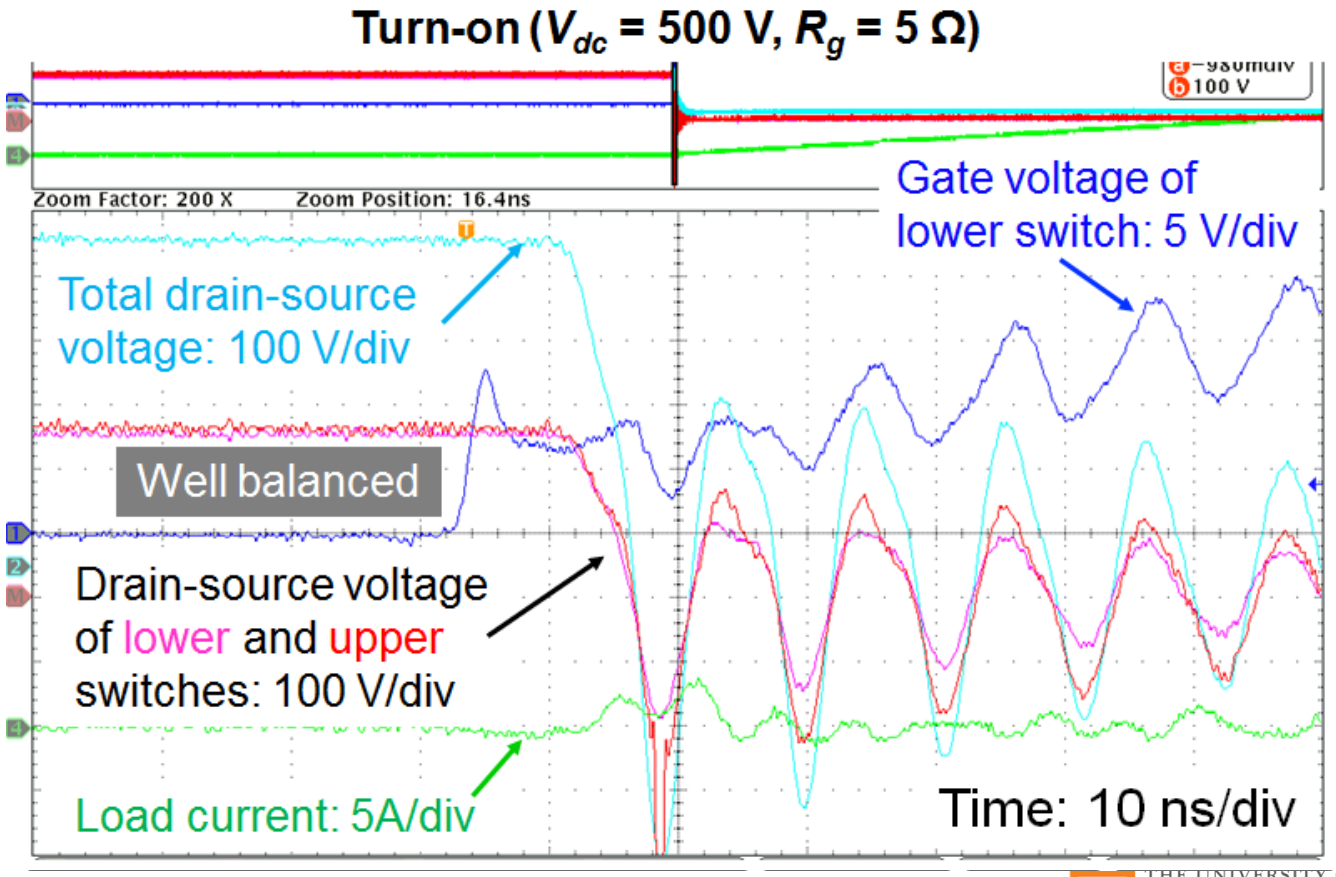
Basic Idea – High Precision Gate Signal Timing



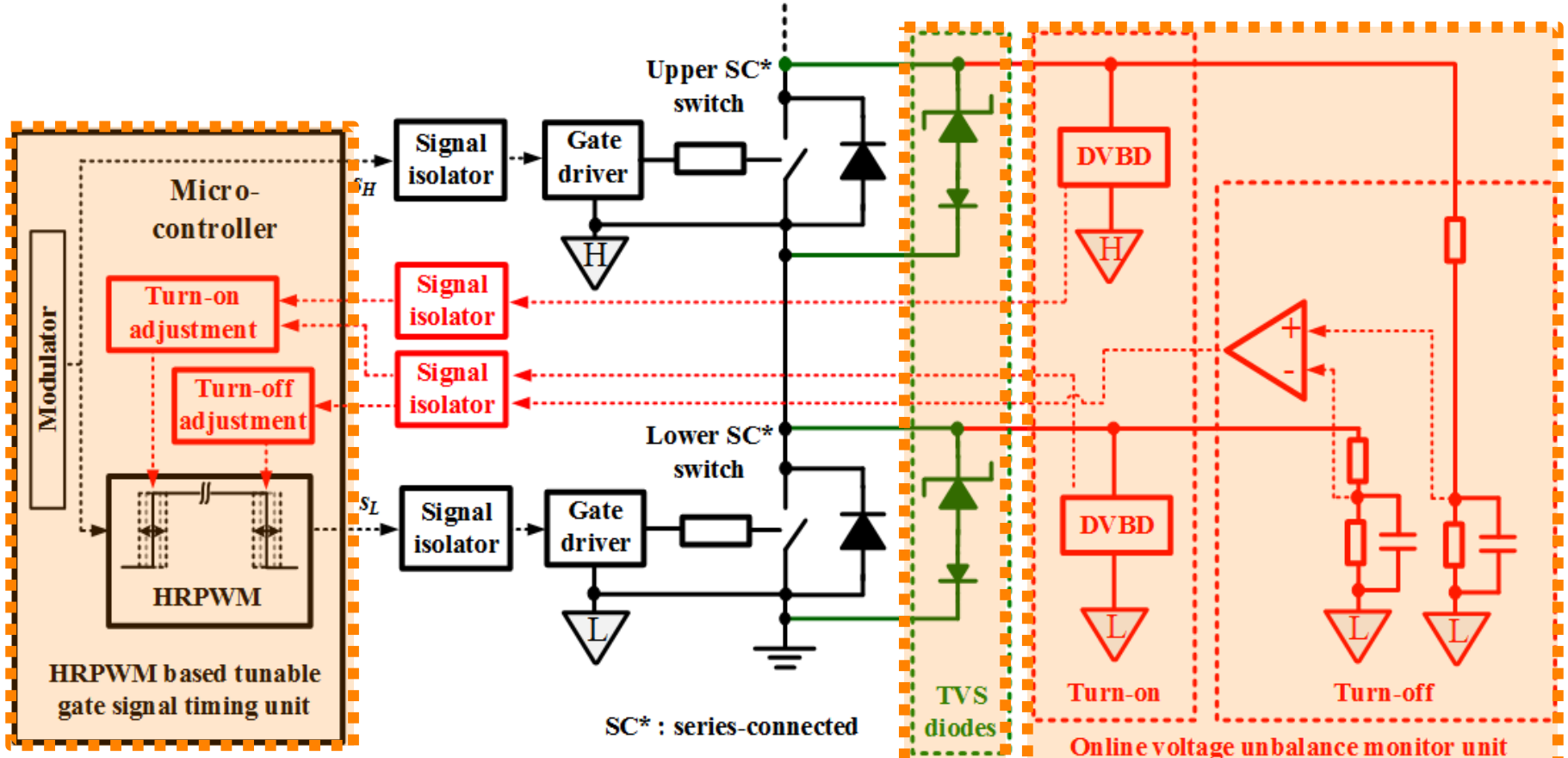


Basic Idea (Cont'd)

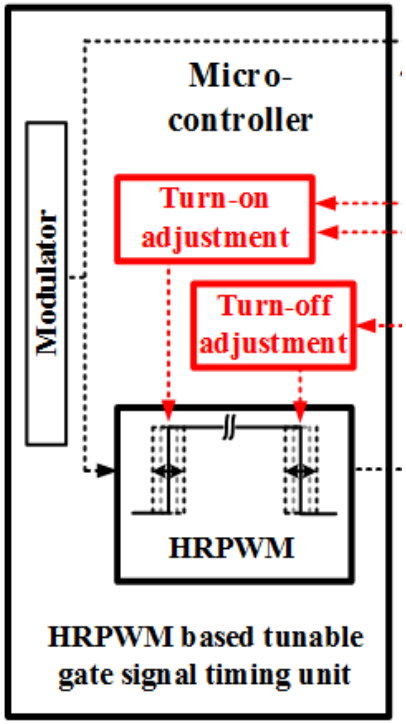


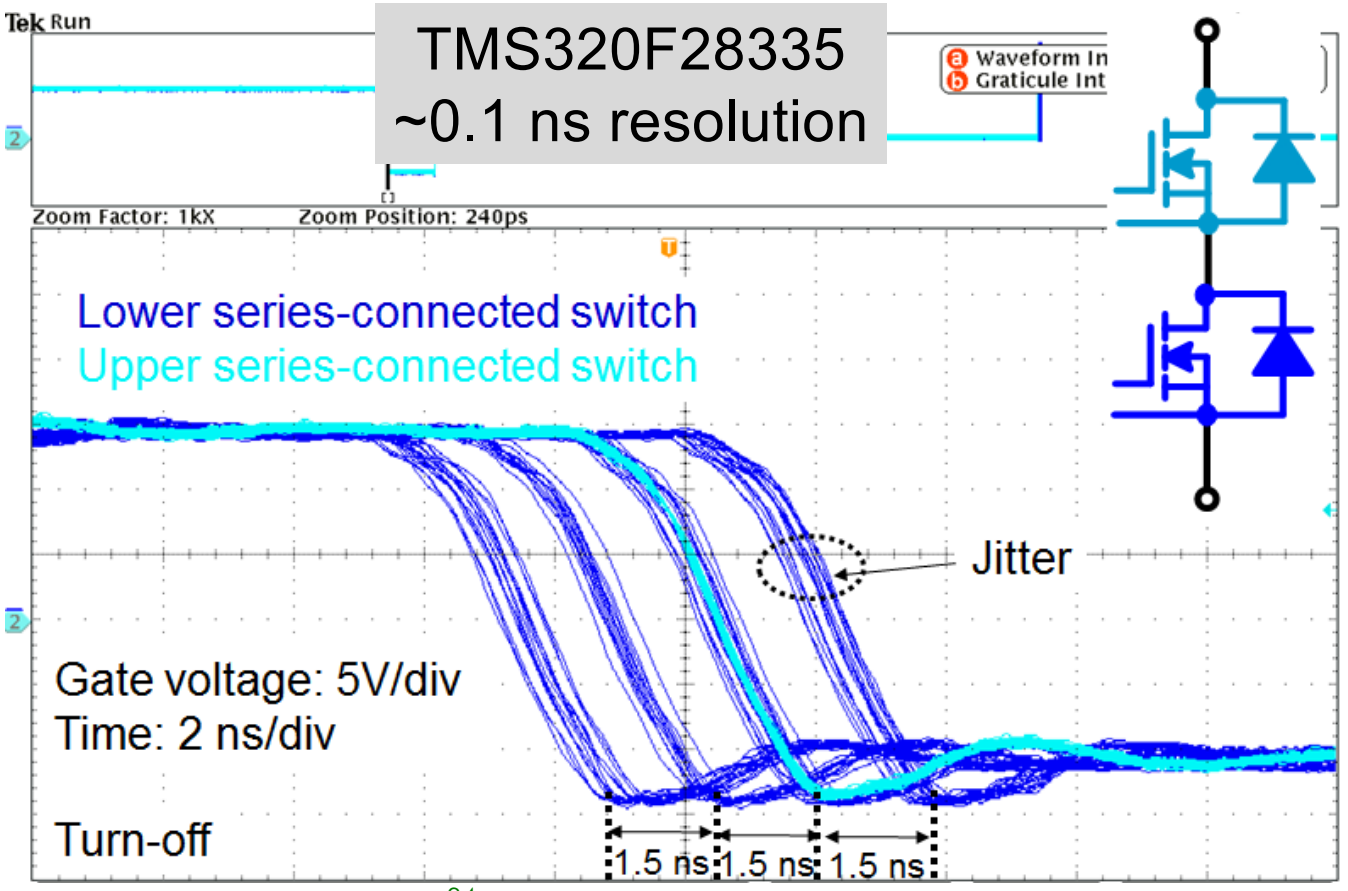


Conceptual Diagram



HRPWM Based Tunable Gate Signal Timing Unit





Outline

- Short circuit capability and protection needs in SiC MOSFETs
- Role of parasitics in phase leg with SiC MOSFETs
- Gate drives for series-connected SiC MOSFETs
- Gate drives for 10 kV SiC MOSFETs
- Current-driven gate drives in SiC MOSFETs

Benefits and Challenges of 10 kV SiC MOSFETs

- Example: 10 kV/100 A SiC MOSFET module vs. 6.5 kV/500 A Si IGBT module

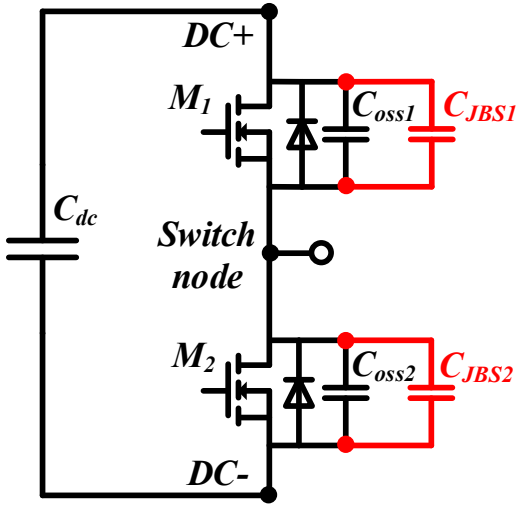
- 10 kV SiC MOSFETs: **>20X reduction** in switching energy loss

Operation conditions	E_{on} (mJ)	E_{off} (mJ)	$E_{on}+E_{off}$ (mJ)
SiC MOSFET at 7 kV, 121 A	**136**	**42**	**178**
SiC MOSFET at 3.5 kV, 61 A	**19**	**11**	**30**
Si IGBT at 3.5 kV, 60 A	279	335	614

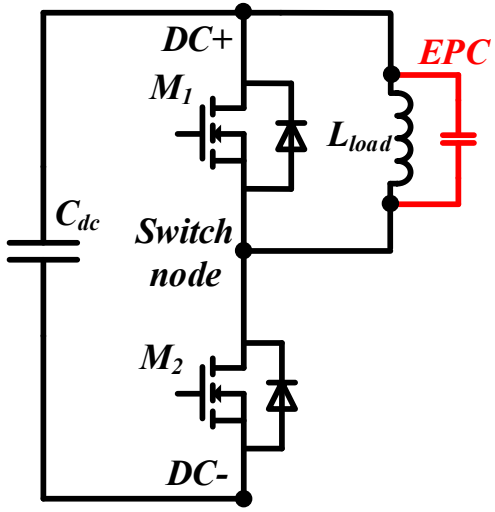
- 10 kV SiC MOSFETs have much higher *dv/dt* and *di/dt*
  - High *di/dt* and *dv/dt* should be tackled in converter design
  - Switching transients more sensitive to parasitics

Operation conditions	Turn-on *dv/dt*	Turn-off *dv/dt*	Turn-on *di/dt*	Turn-off *di/dt*
SiC MOSFET at 7 kV, 121 A	**28.2 V/ns**	**70.1 V/ns**	**1.07 A/ns**	**0.71 A/ns**
SiC MOSFET at 3 kV, 53 A	**20.4 V/ns**	**24.8 V/ns**	**0.8 A/ns**	**0.39 A/ns**
Si IGBT at 3 kV, 40 A	4.53 V/ns	0.95 V/ns	0.24 A/ns	0.05 A/ns
Si IGBT at 3.5 kV, 60 A	6.11 V/ns	1.24 V/ns	0.48 A/ns	0.34 A/ns

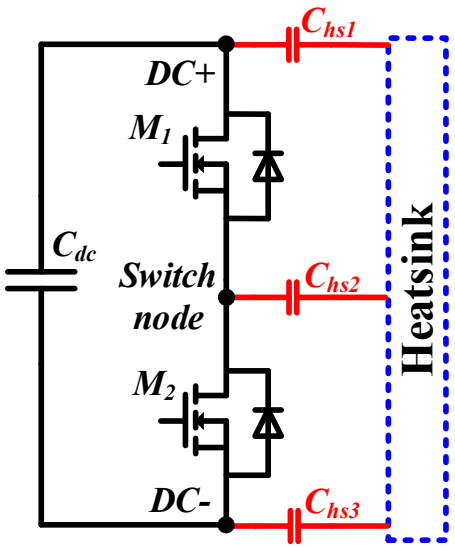
Parasitic Capacitance in MV Converters



Added anti-parallel JBS diode



Load inductor

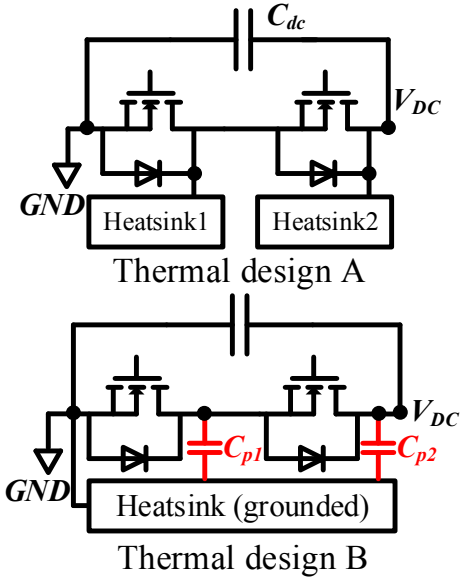


Heatsink

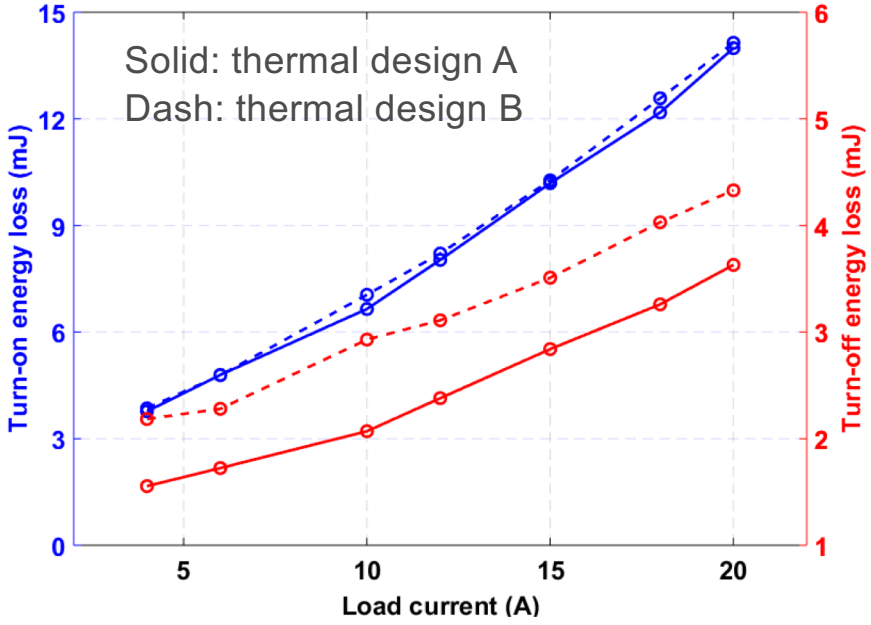
Three major sources of parasitic capacitors in converters based on 10 kV SiC MOSFETs

Heatsink Impact on Switching Transient and Loss

- Parasitic cap due to thermal design B significantly slows down turn-off transient, with little impact on the turn-on transient
- More significant percentage increase in switching loss at lower current



C_{p1} = 29.7 pF



Normalized E_{total} at 6.25 kV

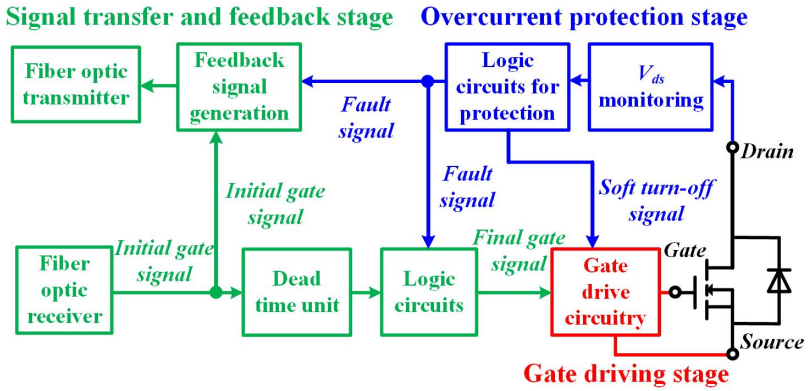
Load current (A)	Thermal design A	Thermal design B
4	100%	113.4%
6	100%	108.4%
15	100%	105.8%
20	100%	104.8%

Overview of Gate Driver Design for 10 kV SiC MOSFET

- Main consideration and challenge: realize fast switching speed and robust continuous operation with **6.5 kV insulation voltage** and ***dv/dt* up to 80 V/ns**

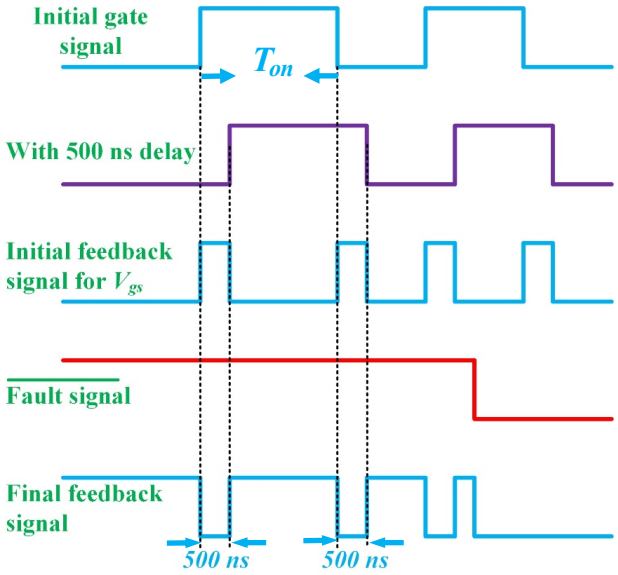
Specification	Target	Design result
Driving voltage	Maximum: +20 V; Minimum: -5 V	-5 V for off state; 15 V for on state
Peak driving current	> 8 A	9 A
Rise and fall times	< 30 ns	22 ns rise time; 15 ns fall time
Short circuit protection	< 1.5 us response time with soft turn-off	< 1.3 us response time with soft turn-off
Status feedback	Feedback signal sent back to controller in every switching cycle	Feedback signal generated for every rising or falling edge in gate signal
Dead time	Dead time realized with hardware	500 ns dead time realized in the gate driver

Signal isolation: fiber optics



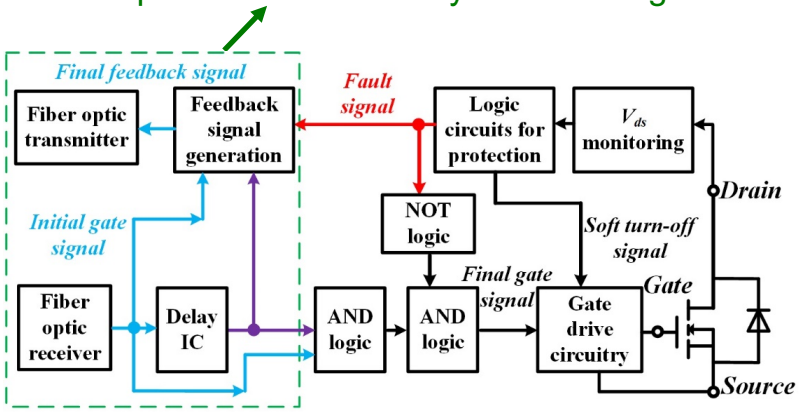
Signal Transfer and Feedback Stage

- Generating feedback signal sent back to controller
  - Status feedback to monitor communication and gate driver
  - Acknowledge every rising or falling edge with 500 ns LOW signal
  - Report the fault once the overcurrent protection is triggered



Generation scheme of final feedback signal

Components monitored by feedback signal



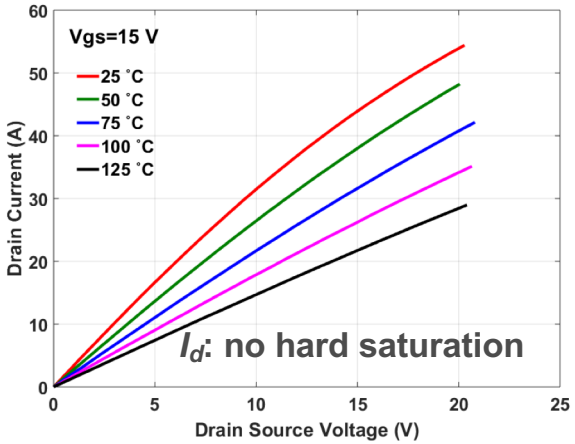
500 ns status feedback signal:

- Little limitation on the duty cycle of MOSFET
  - ✓Only requires >4% duty cycle if switching frequency is 80 kHz
- Controller identifies overcurrent fault if feedback signal is LOW for over 600 ns
- Sufficient noise immunity

Overcurrent Protection Stage

- Desat protection scheme selected for 10 kV/20 A SiC MOSFETs
  - Effective for different fault types
  - Relatively easy implementation to achieve high noise immunity
- Design challenges
  - Protection should respond within 1.5 µs with good noise immunity
  - Threshold current: higher at lower temperature
  - Desat diode should block high voltage with small parasitics

Specification	Detail
Response time	<1.3 µs
Threshold current	20 A at 125 ˚C 42.85 A at 25 ˚C
Soft turn-off	Turn-off with 47 Ω gate resistance
Output signal to controller	Always low signal via fiber optics if triggered
Voltage rating of desat diode	>10 kV

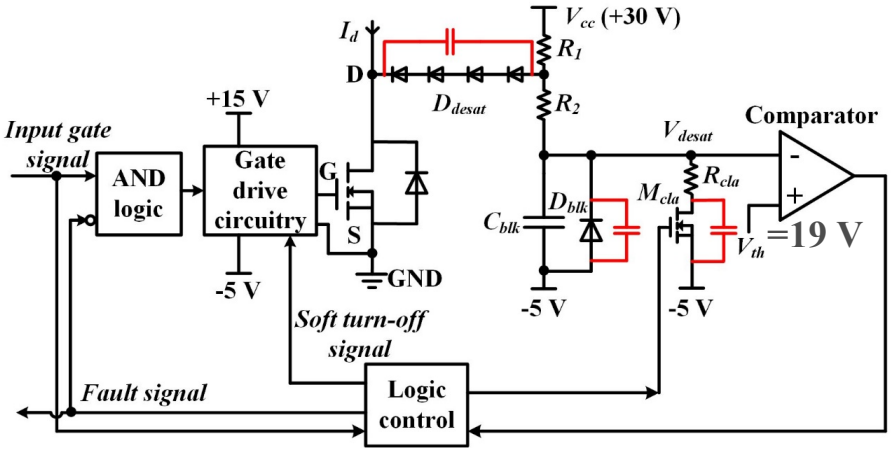


I-V characteristic at different temperatures

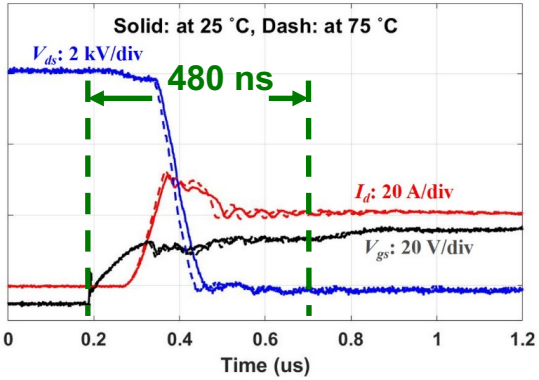
Implementation of Desat Protection

- Implementation with discrete components
  - Desat diode: four 3.3 kV SiC diodes in series with 4 V voltage drop
  - Avoid false triggering during turn-off transient: clamp V_{desat} to -5 V in OFF state
- **Blanking time:** avoid the false triggering during turn-on transient
  - Required blanking time : >550 ns (**minimum toal response time: 600 ns**)
  - Equation: $t_{blk} = \tau \ln\left(\frac{V_{cc}+5}{V_{cc}-V_{th}}\right), \tau = C_{total}(R_1 + R_2)$
  - Implementation result: 1.22 μs blanking time, 6.49 kΩ R_1, 75 pF C_{blk}
  - Reduce R_1 and C_{blk} for shorter response time

Total response time	1.26 μs
Comparator & control delay	0.04 μs
Blanking time due to C_{blk}	0.6 μs
Blanking time due to all parasitic caps	0.54 μs
Blanking time due to delay in the gate of M_{cla}	0.08 μs



Turn-on transient at 6.25 kV/20 A



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High Turn-on Loss of SiC MOSFET

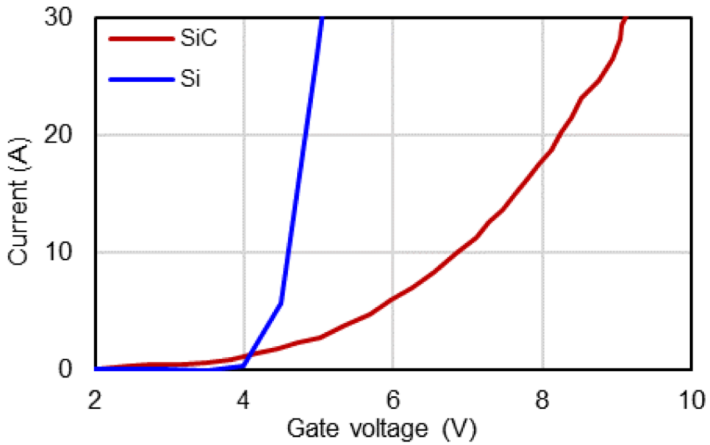
Si

I_L (A)	E_{on} (μJ)	t_{cr} (ns)	t_{vf} (ns)
10.44	63.24	2.00	6.60
21.05	99.81	2.60	7.40
31.99	145.71	4.20	8.60

SiC

I_L (A)	E_{on} (μJ)	t_{cr} (ns)	t_{vf} (ns)
9.76	71.31	1.60	11.40
20.09	160.62	2.80	16.00
31.76	310.15	5.80	16.60

- Current rise time does not have much difference
- SiC MOSFET has longer voltage fall time



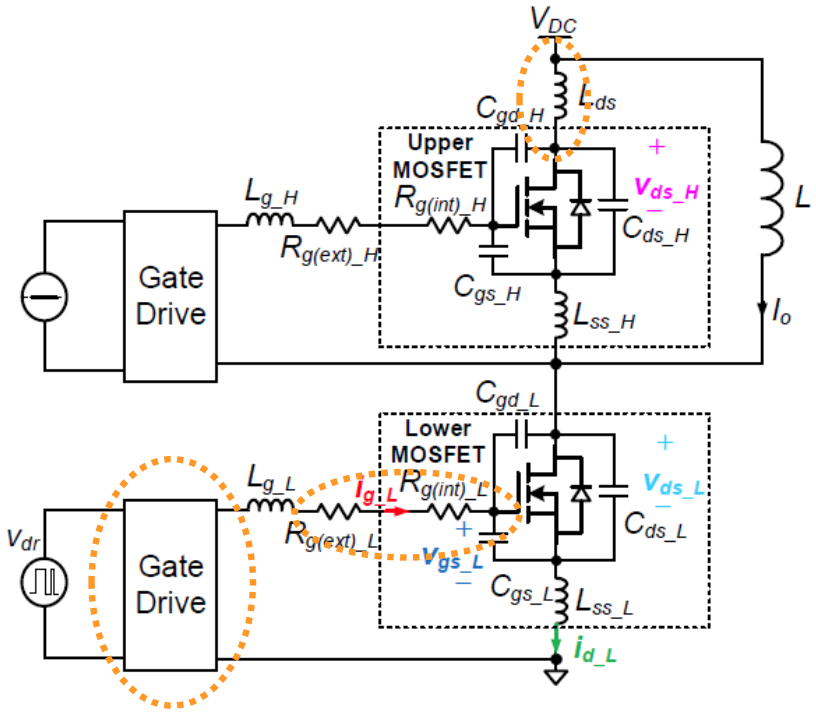
Tested transfer characteristics when V_{ds}=500 V

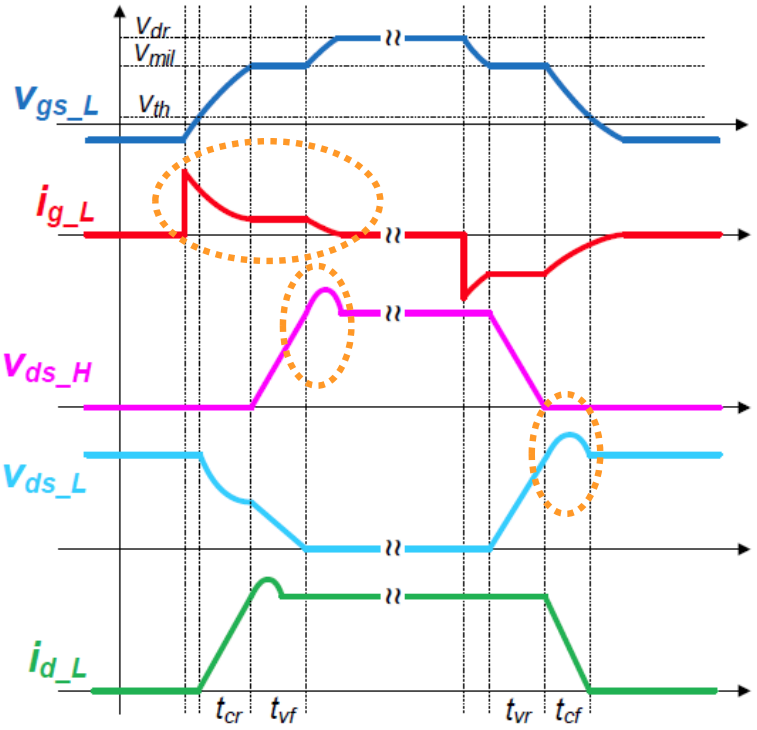
Lower transconductance ⇨ Higher Miller voltage

⇩

Longer voltage fall time ⇦ Lower gate current

Impact Factors of Switching Speed

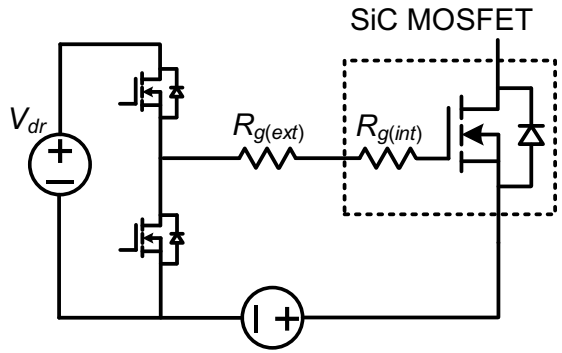




- Gate current limited by gate resistance and gate drive capability
- Over-voltage caused by parasitics

Need for Current Source Gate Drive

Motivation: Increase gate current during switching transient to reduce voltage fall time



Typical voltage source gate drive (VSG)

$$I_g = \frac{V_{dr} - V_{th} - \frac{I_o}{g_m}}{R_{g(int)} + R_{g(ext)}}$$

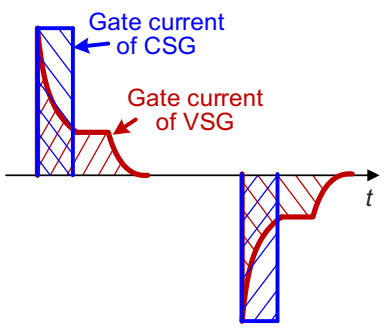
Changeable: $R_{g(ext)}$ & V_{dr}

- Decrease external gate resistance: Internal gate resistance is still high*

$R_{G(int)}$	Internal Gate Resistance		10.5

- Increase supply voltage: Limited by gate voltage rating*

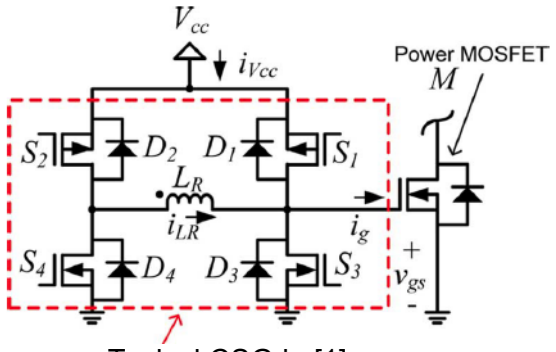
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V



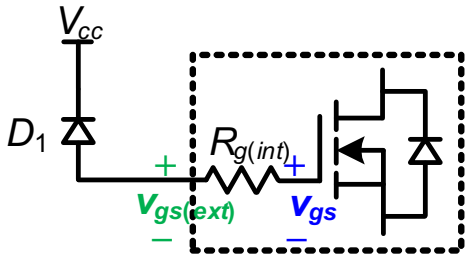
* Datasheet of C3M0075120K, Wolfspeed

Current source gate drive (CSG)
=> keep constant gate current

Limitation of Existing CSG



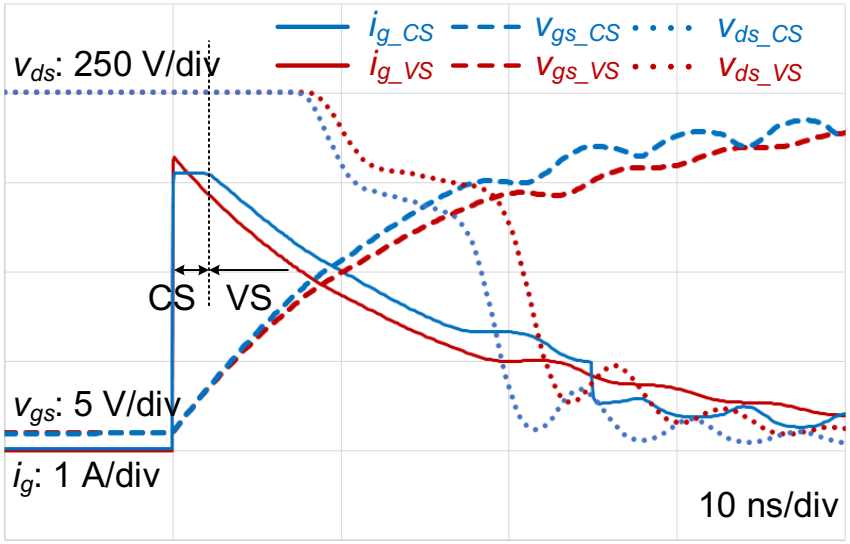
Typical CSG in [1]



Voltage occurs across $R_{g(int)}$ => $v_{gs(ext)}$ higher than v_{gs}

When $v_{gs(ext)}$ higher than V_{cc}=> D_1 conducts

CSG becomes VSG

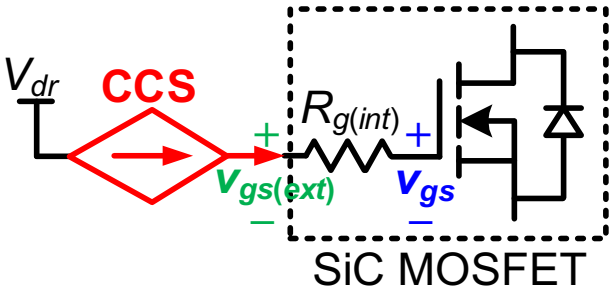


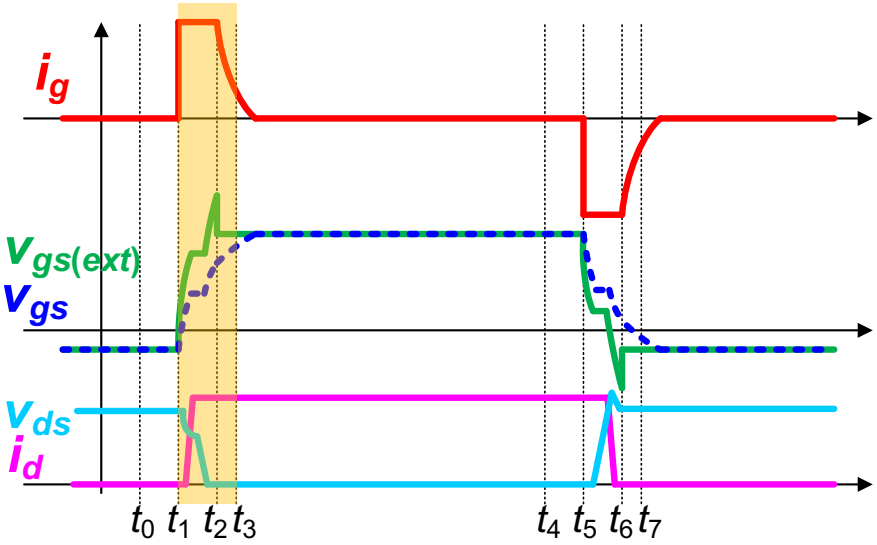
Simulation waveforms with CSG and VSG

Due to large internal gate resistance, CSG turns to VSG before drain-source voltage decreases. Reduced switching time is very limited with existing CSG technology.

[1] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz", *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 678-691, Mar. 2008.

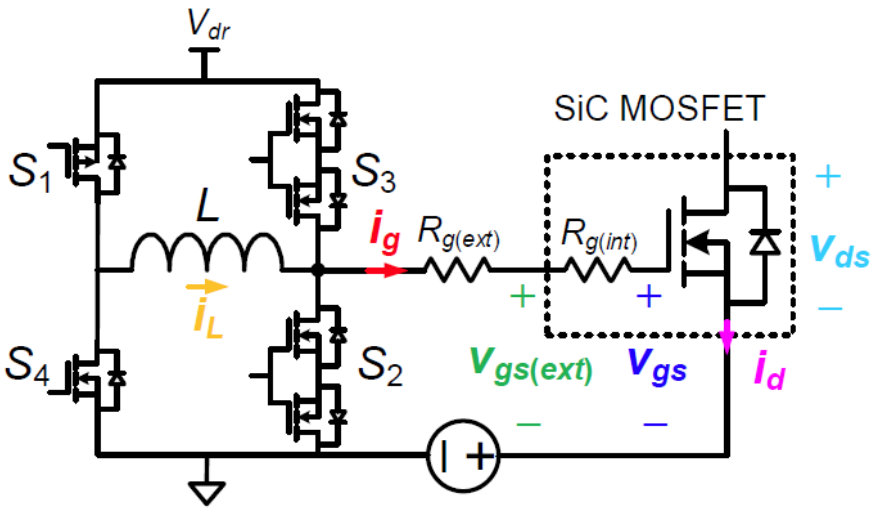
Requirements of CSG for SiC MOSFETs

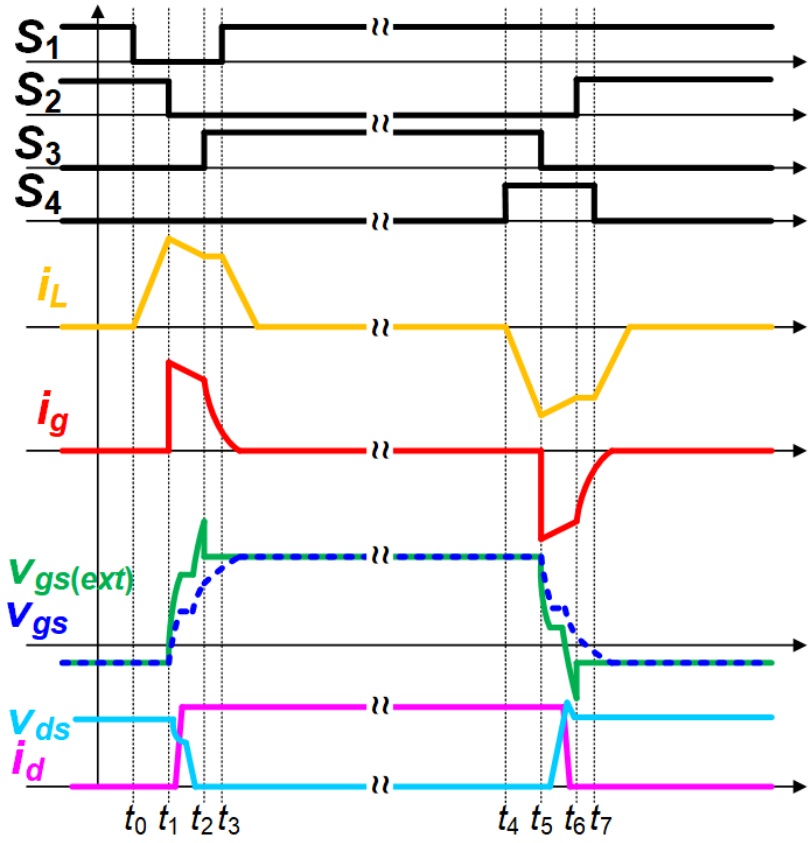




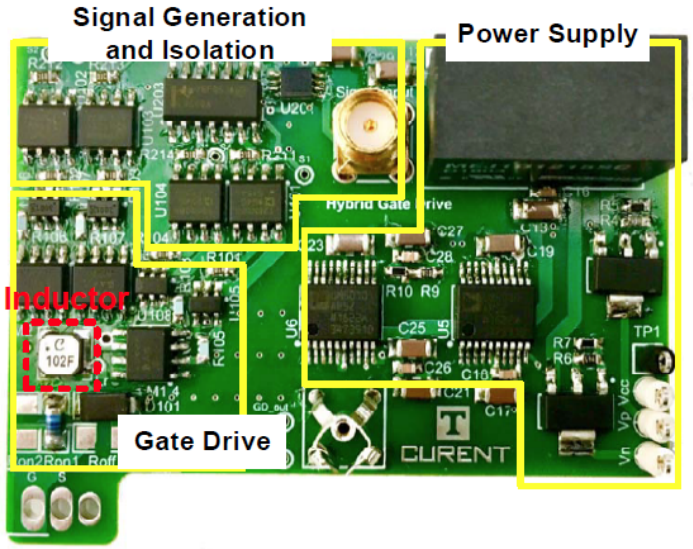
- During switching transient, CSG can keep constant current source (CCS) regardless of large internal gate resistance. External gate voltage can be higher than supply voltage.
- After switching transient, CSG can actively change to VSG to protect gate voltage from over-charging/ discharging.

Proposed CSG





Picture of Developed CSG

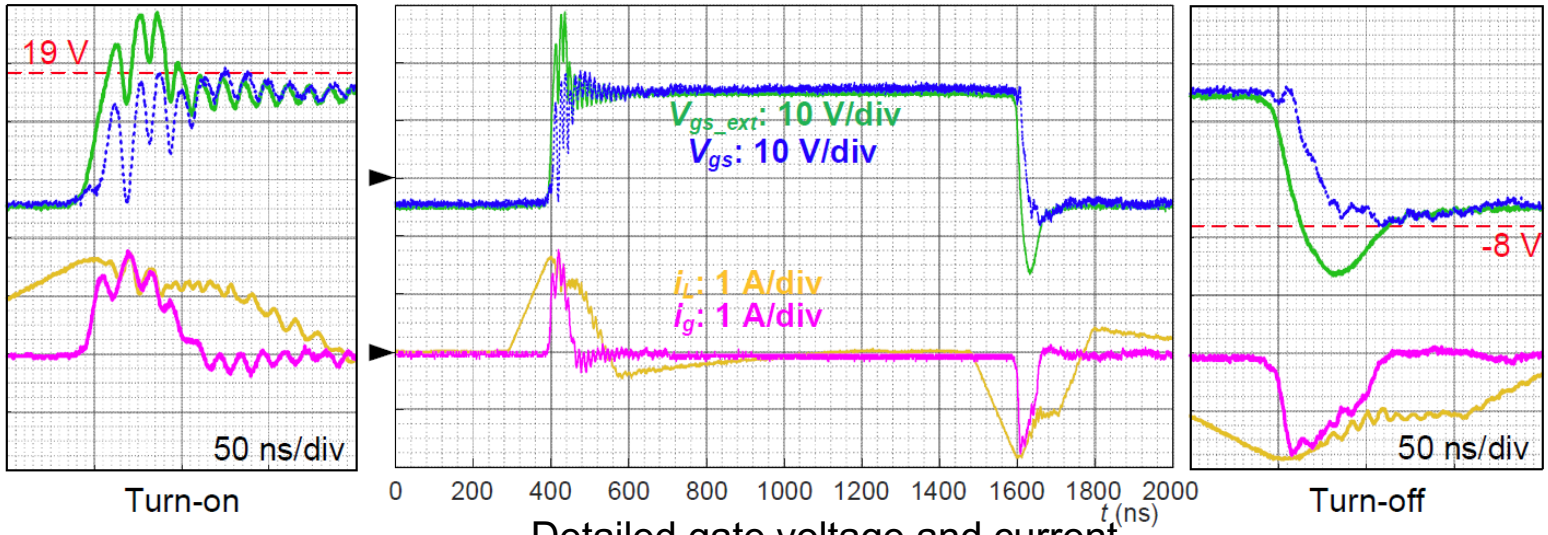


Device	1.2 kV, 30 A SiC MOSFET
Internal gate resistance	10.5 Ω
Initial gate current	1.4 A
DC bus voltage	500 V
Peak load current	30 A

- A classical VSG is tested for comparison
- Same bus voltage, load current, gate drive voltage and total gate resistance is adopted for two gate drives

Testing Waveforms

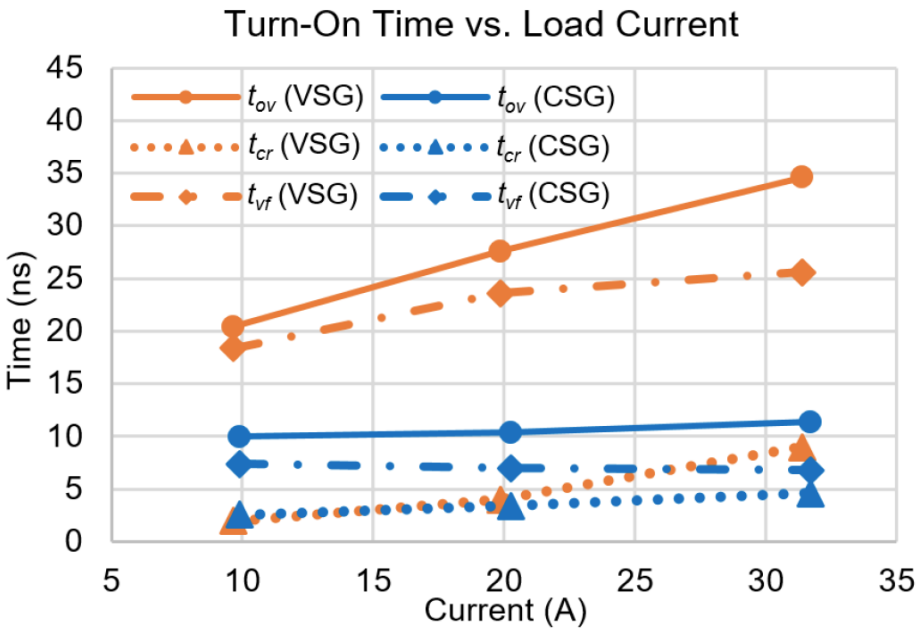
- 500 V DC bus, 30 A load current

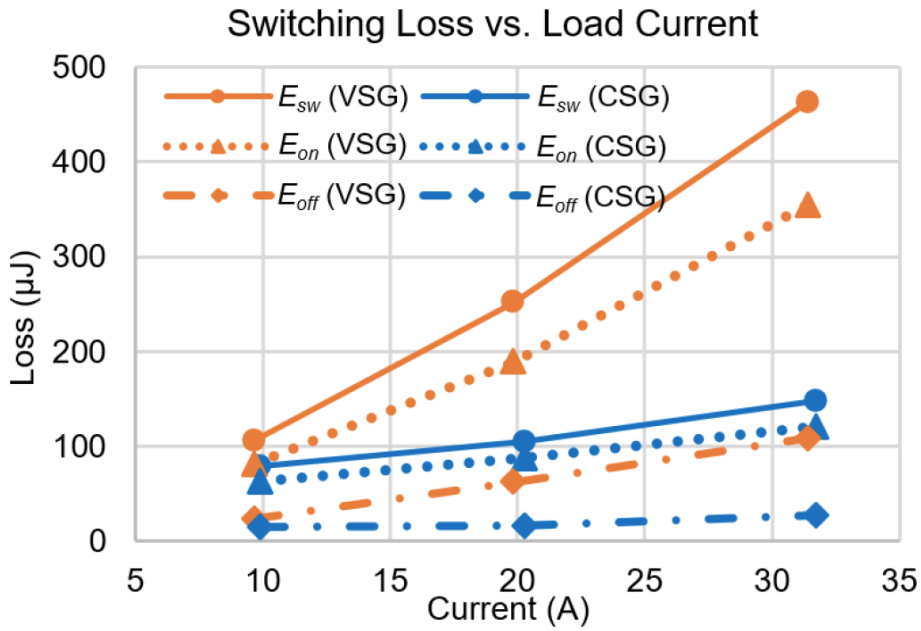


Detailed gate voltage and current

- External gate voltage is higher than gate drive supply voltage
- Internal gate voltage is very close to gate voltage limits, which requires accurate timing control to avoid over-voltage

Switching Time and Loss Comparison





- Both switching loss and turn-on time is significantly improved with proposed CSG

SiC MOSFET Gate Drive - Summary

- Small size and limited ruggedness of SiC MOSFETs requires fast protection schemes.
- High speed switching of SiC MOSFETs requires minimizing circuit parasitics.
- Full understanding of switching operation of devices enables design of gate drives that maximize devices' potential.
- Integrated gate drive can be designed to have multiple functions to take full advantage of high speed switching while limiting adverse effects on device and circuit.

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