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High Power Density and High Voltage: New Frontiers of Power Electronics Enabled by WBG Power Devices

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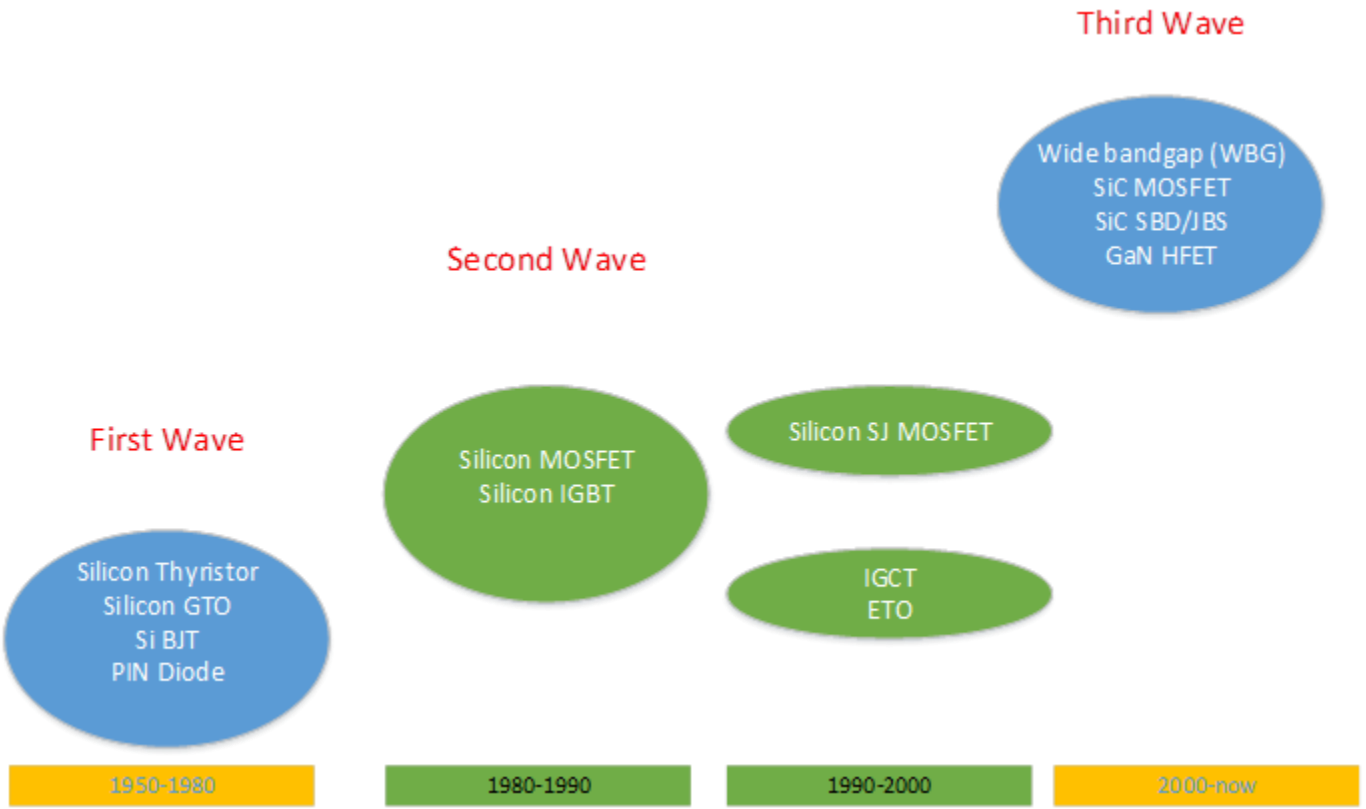
Outline

- Achieving Zero Switching Loss in Power Switch
  - Hard-driven concept
- High Density Power Electronics
- High Voltage (Medium voltage) Power Electronics
- Conclusions

Contributions by many current and formers students are gratefully acknowledged

Power Semiconductor Devices: Waves of innovations



Si device concepts are settled on several well established concepts

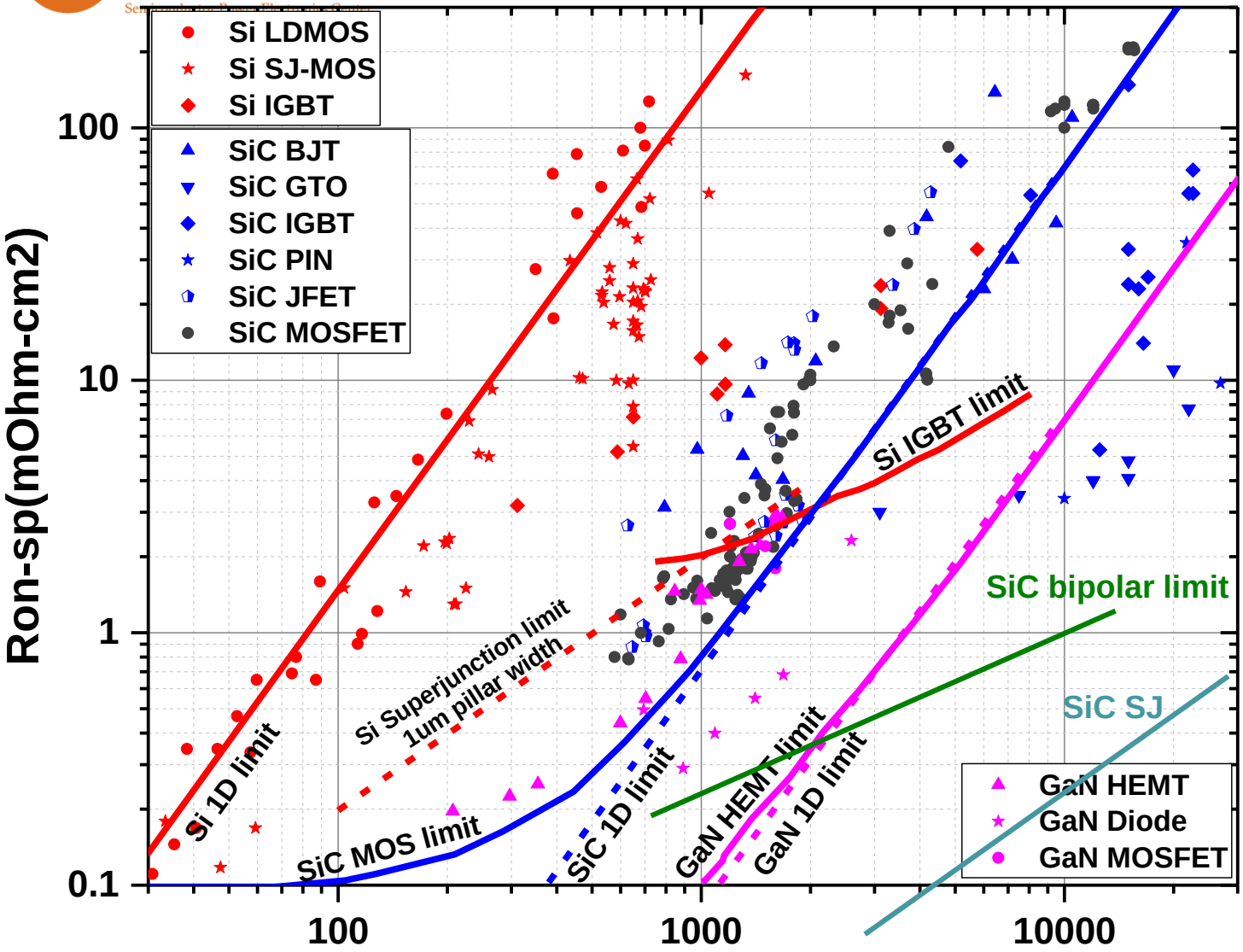
thyristor (symmetric and asymmetric, forced turn-off or line commutated)
IGBT
MOSFET (or other FET variations)
Schottky diode/PN junction diode

Next major trend: move from Si to WBG

MOSFET (or FET variations) is the dominant device concept

AQ Huang, "Power semiconductor devices for smart grid and renewable energy systems", Proceedings of the IEEE, 2017

Ron FOM Drives Chip Size Reduction



$$R_{on-sp} = \frac{4BV^2}{\mu\varepsilon E_c^3}$$

Ec(Si)=0.3MV/cm

Ec(SiC)=2.2MV/cm

$$R_{on-sp} = \frac{BV * C_p}{2\mu\varepsilon E_c^2}$$

SiC MOSFET: Achieved 100X reduction over Si and 10X over Si SJ

Not much improvement over Si IGBT

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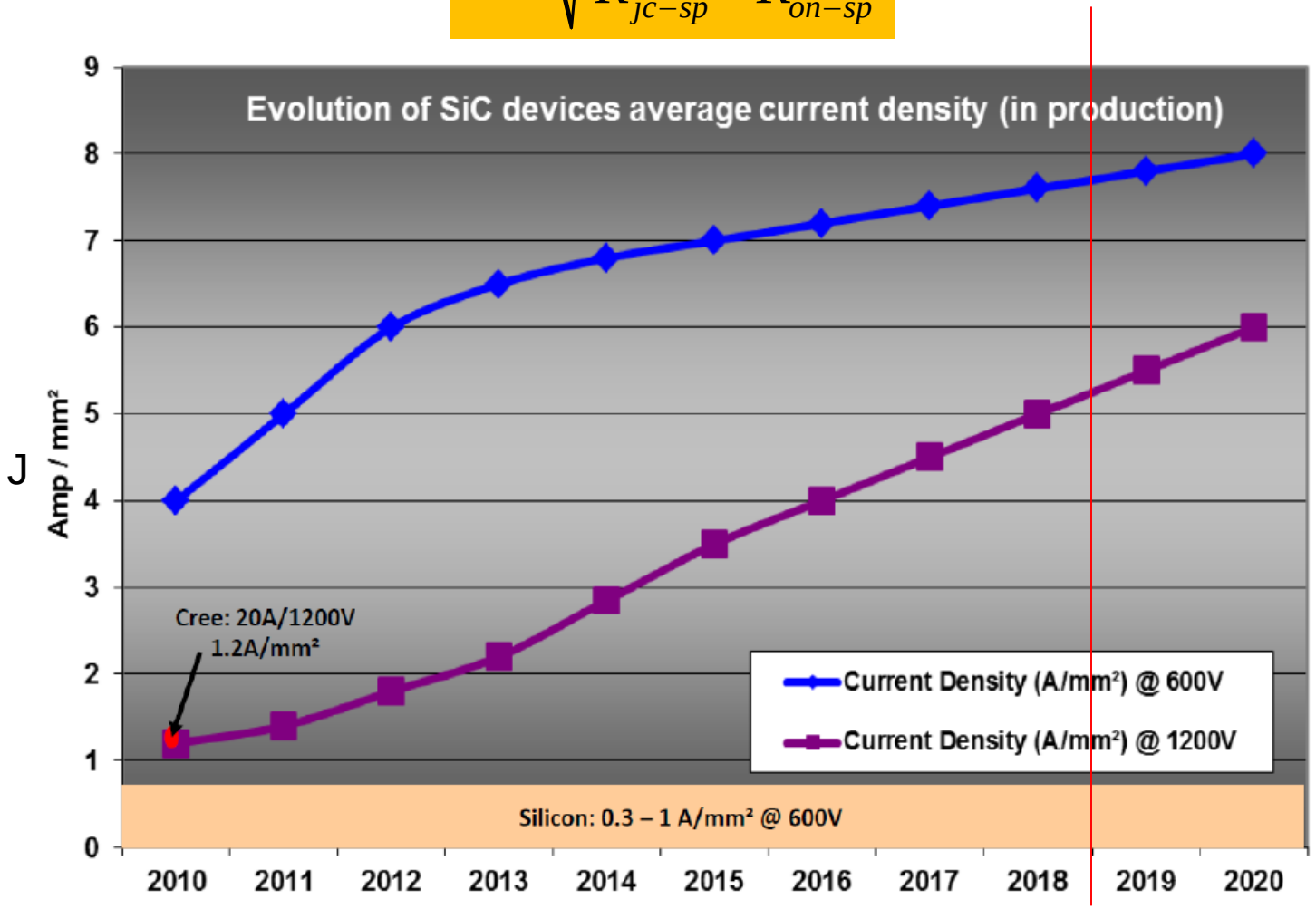
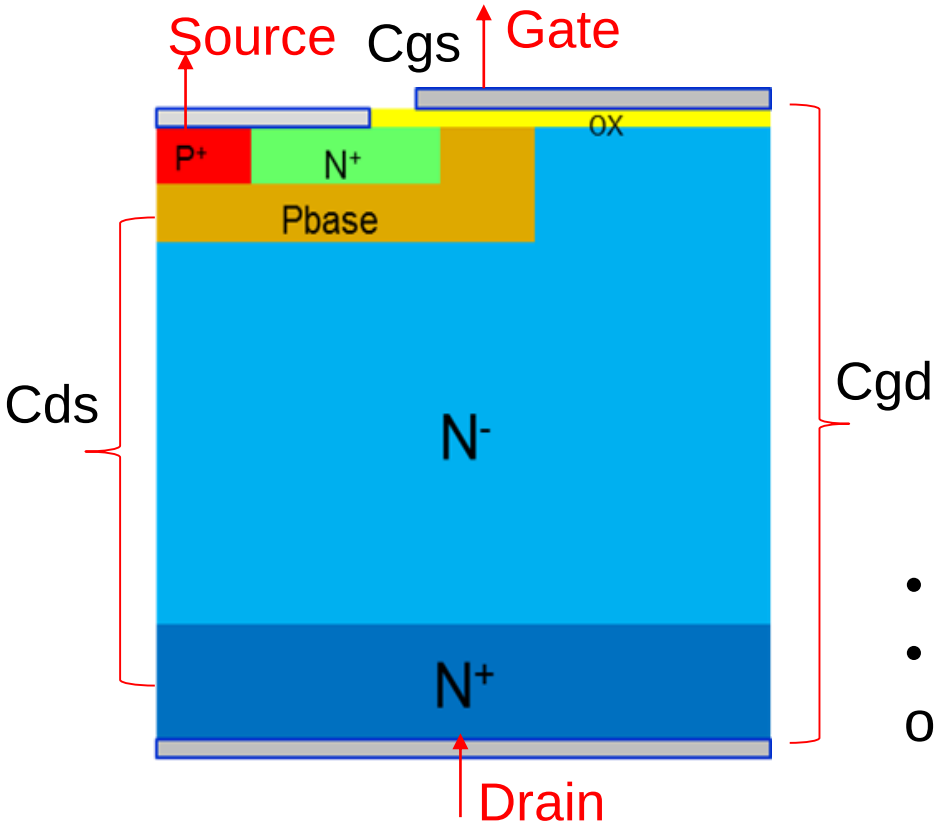
Current Density & Chip Size

$$J = \sqrt{\frac{\Delta T}{R_{jc-sp} * R_{on-sp}}}$$



Yole Developpement, 2012

Vertical SiC MOSFET



Device capacitance?

- Cgs ~ Cox*Achip
- Qoss ~ ε*Ec*Achip
- Coss ~ Ec

- Cgs decrease as Achip decreases
- Output capacitance is smaller

only if chip size is 10X smaller

Chip Size Reduction is the Key

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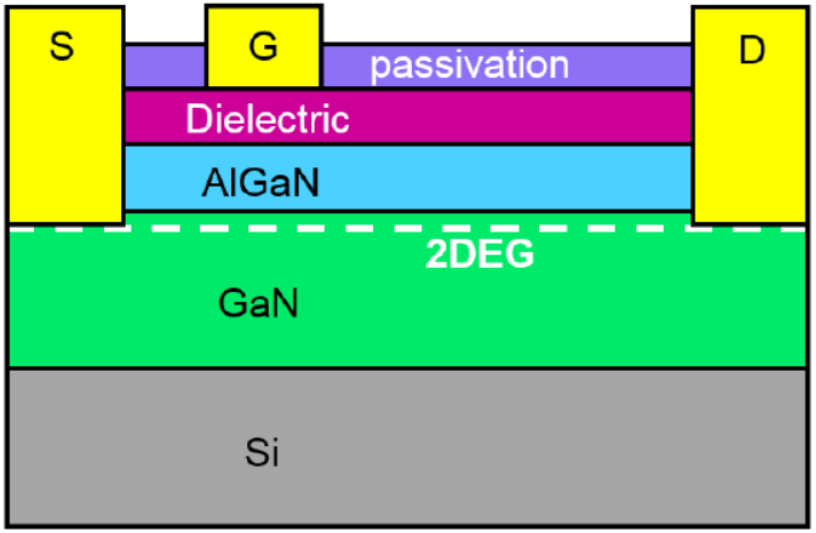
600V GaN HEMT/HFET Devices: Lateral Device Structure



Advantage over SiC

- ❑ High mobility 2DEG channel ($2x10^{13}/cm^2$, $1500cm^2/V\text{-}s$)
  - Enabled Lower channel resistance
  - Support even lower BV device (<100V)
- ❑ Even lower capacitance due to lateral structure
- ❑ Lower gate drive voltage
  - Low gate charge hence gate loss is low even in MHz
  - Cgs scale with feature size and chip size

A Closer Look at Ron, Capacitance, Qrr

600V Devices Compared

600V FETs	Ron (mohm)	Ciss (nF)	FOM 1 (Ron*Ciss)	Coss (nF)@400V	FOM2 (Ron*Coss)	Qrr(uC)	FOM3 (Ron*Qrr)
Si SJ	37	7.24	267	0.38	14	36	1332
SiC MOS	120	1.2	144	0.09	10.8	0.053	6.3
GaN HFET	25	.52	13	0.13	3.25	0.113	2.8

Si SJ: Infineon IPW65R037C6. SiC MOSFET: Rohm SCT2120AF GaN HFET: GaNSystem GS66516T

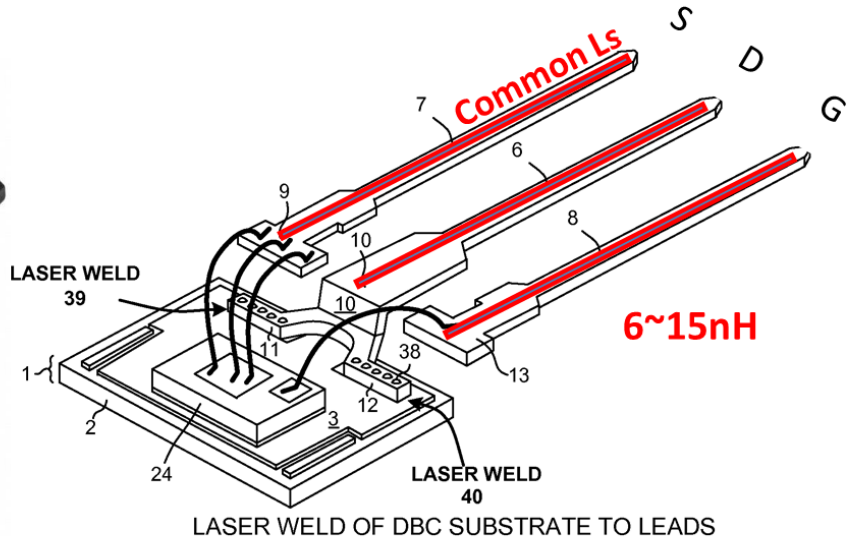
- Gate loop is getting faster & faster

Drain loop
dV/dt increase?
dV/dt ~ I/C=J/C_{sp}

Reverse recovery charge/loss
Basically eliminated in WBG devices

SiC Packaging Inductance Limiting the Speed

Need large Rg to damp the gate loop. Making it slower

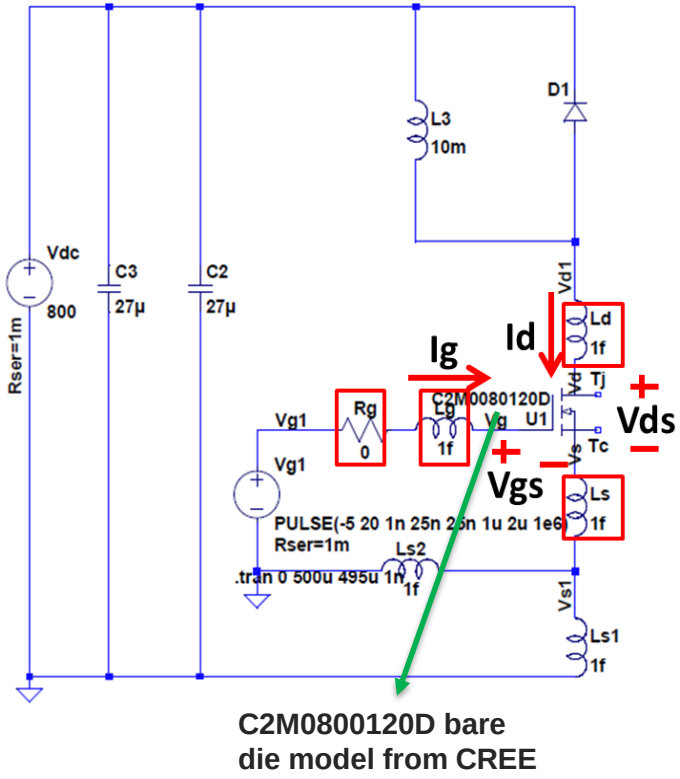


LASER WELD OF DBC SUBSTRATE TO LEADS

Conventional package (TO-247 or TO-220) can introduce stray inductance to the circuit in all three terminals.

US 20130175704 A1 Discrete power transistor package having solderless dbc to leadframe attach

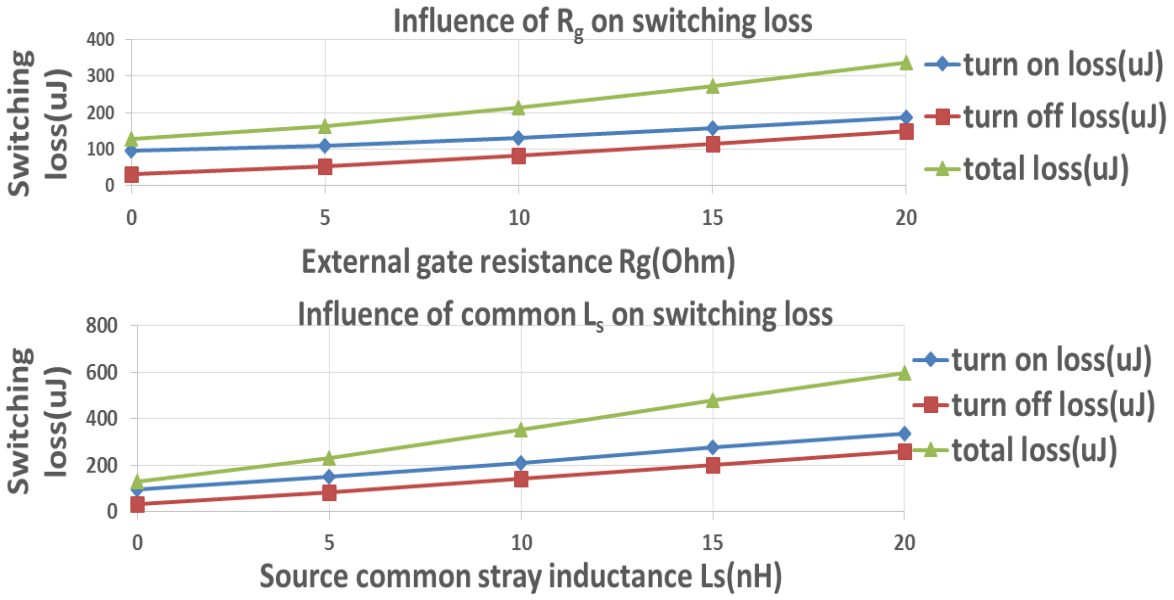
Speed Impacts Loss



C2M0800120D bare die model from CREE

Simulation condition:

Vgs = -5, 20V; Vds = 800, 0V; Id = 0, 20A.



All parasitic inductance need to be reduced to take advantage of a smaller die SiC switch

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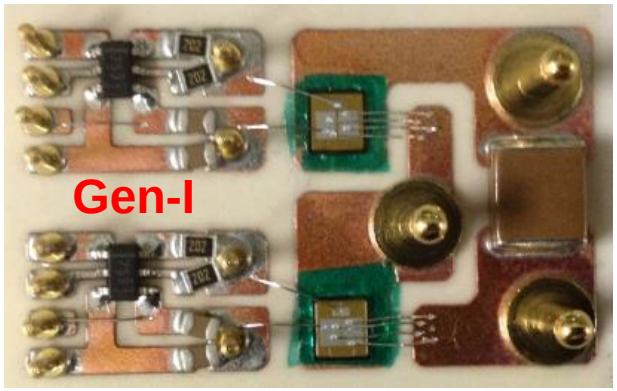
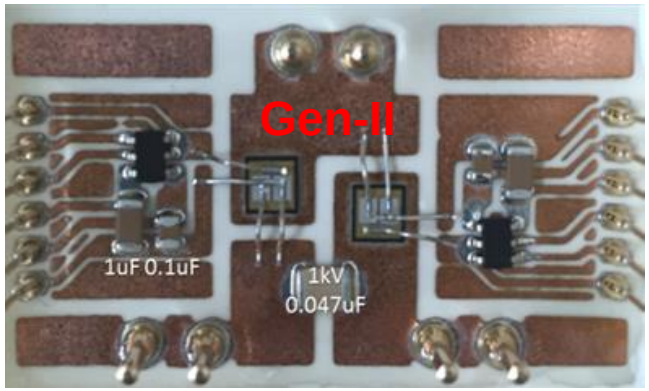
Reducing Lg and Id, Ls

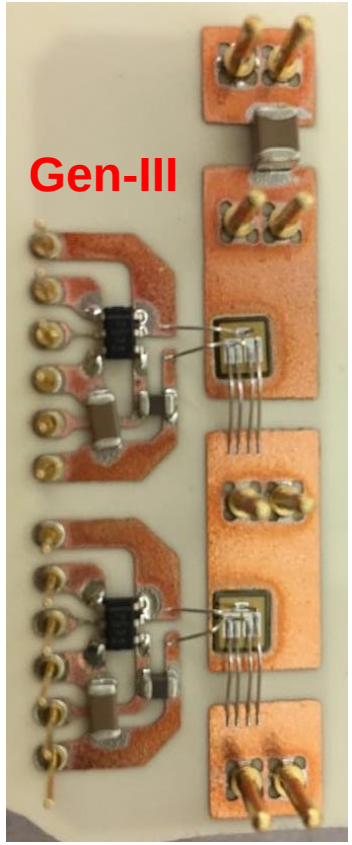
- Monolithic Driver + Power MOSFET Integration
- Module level integration

ANSYS Q3D Extractor

Design	Gen-I	Gen-II	Gen-III
Power Loop Inductance (nH)	11.3	7.3	3.4







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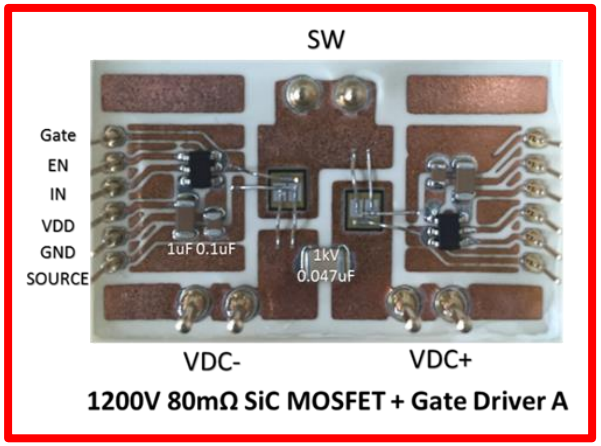
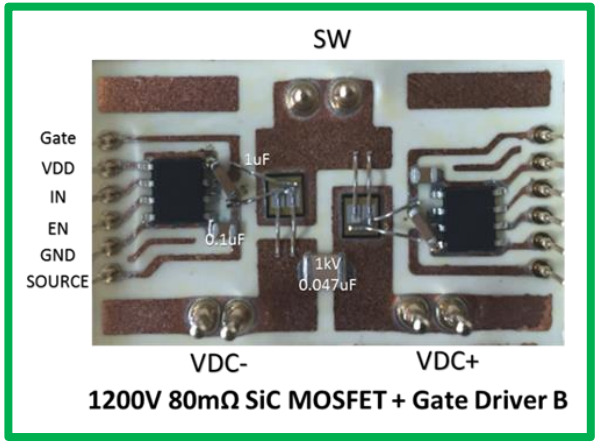
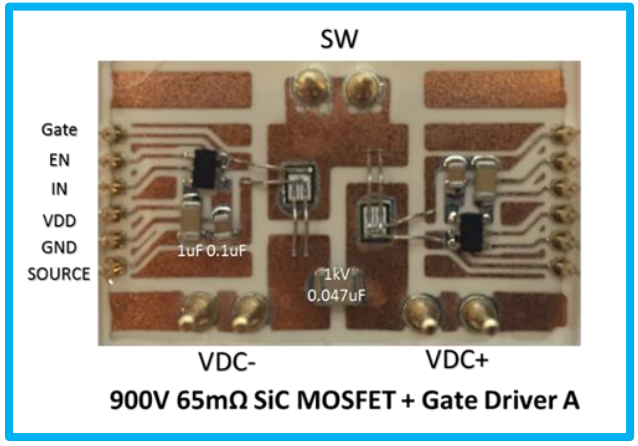
Gen-II Module Lg

ANSYS Q3D Extractor





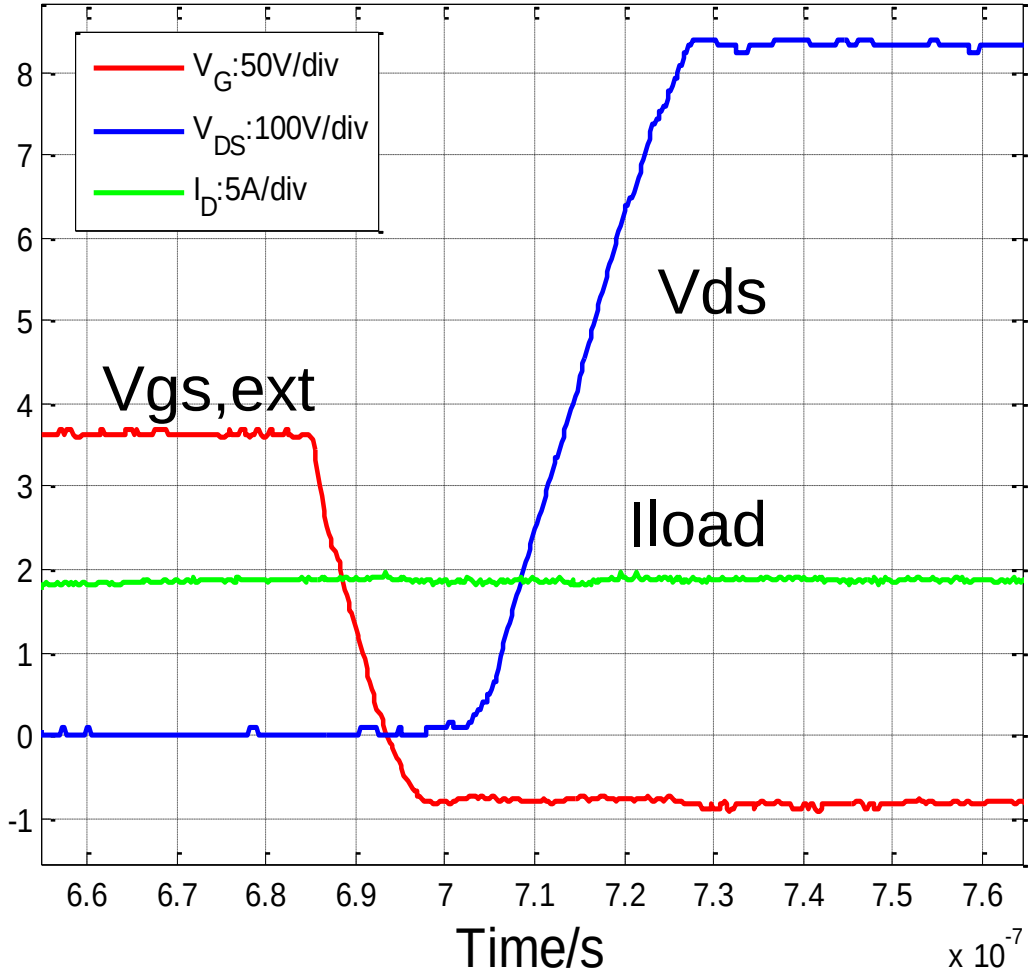


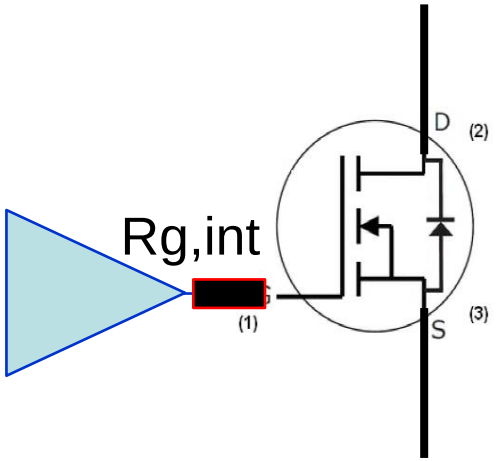
Module#	SiC MOSFET	Gate driver	Turn-on gate loop	Turn-off gate loop
1	1200V 80mΩ	A (2.5A/5A)	7.73 nH	6.07 nH
2	1200V 80mΩ	B (14A)	5.00 nH	5.69 nH
3	900V 65mΩ	A (2.5A/5A)	7.73 nH	6.07 nH

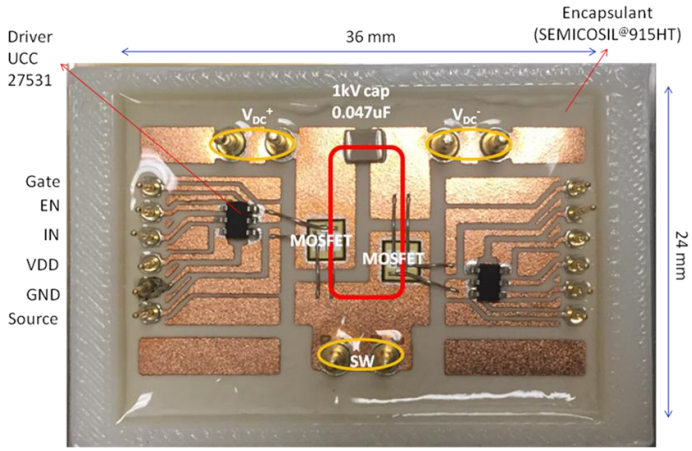
Room to further reduction

Zero Turn-off Loss (hard driven SiC)

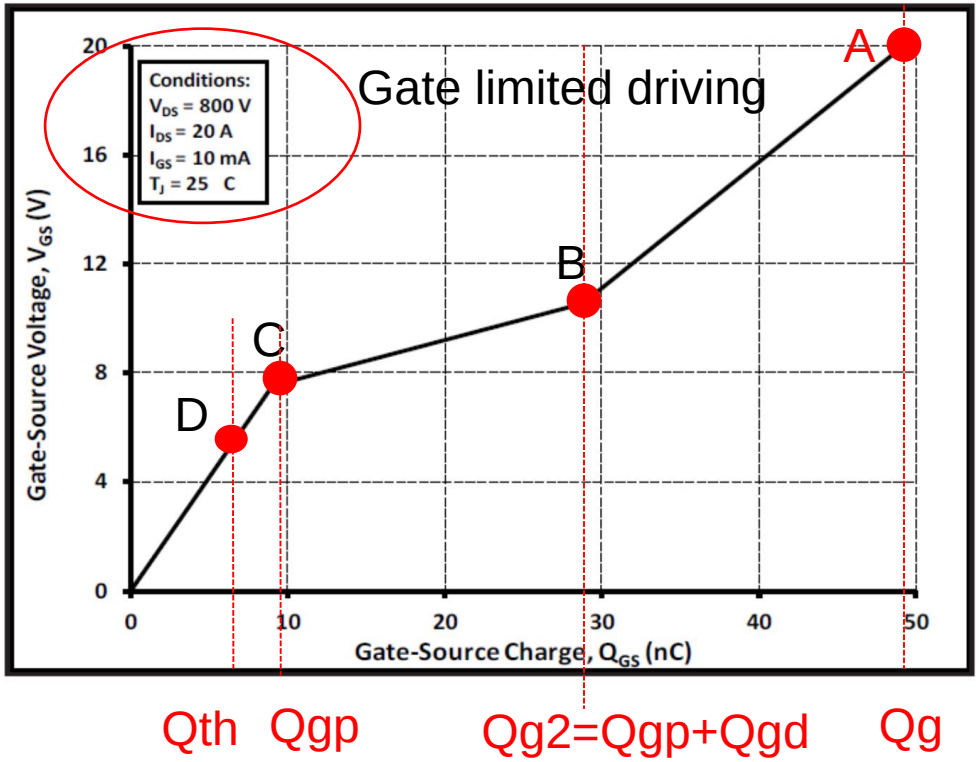
80 mohm 1200VC SiC MOSFET, Rg,ext=0, V=800V, I=10A



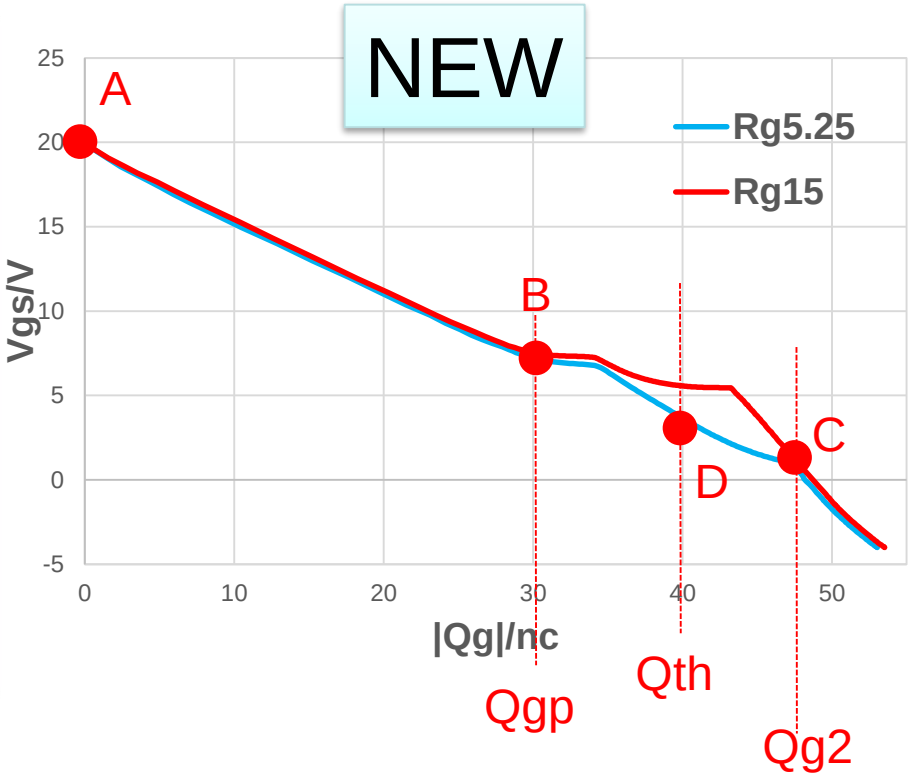




Condition for Zero Turn-off Loss



Qth Qgp Qg2=Qgp+Qgd Qg

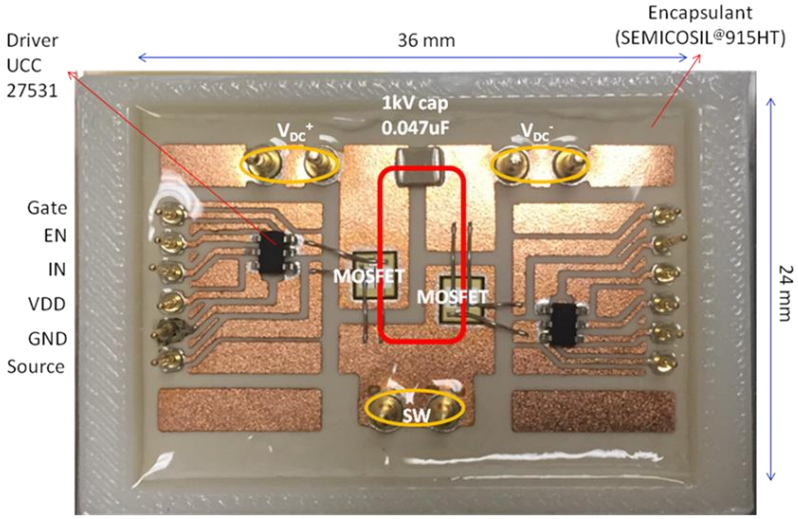


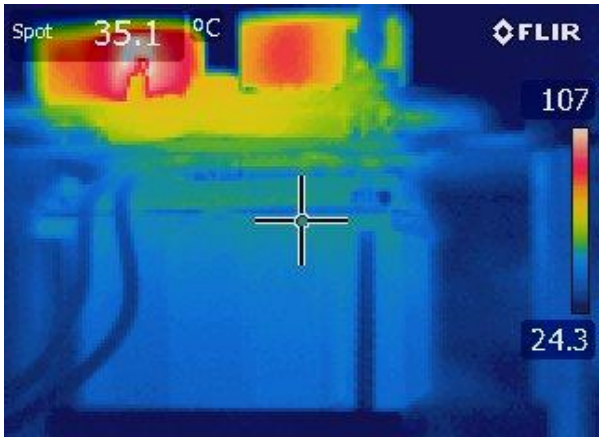
Qgp Qth Qg2

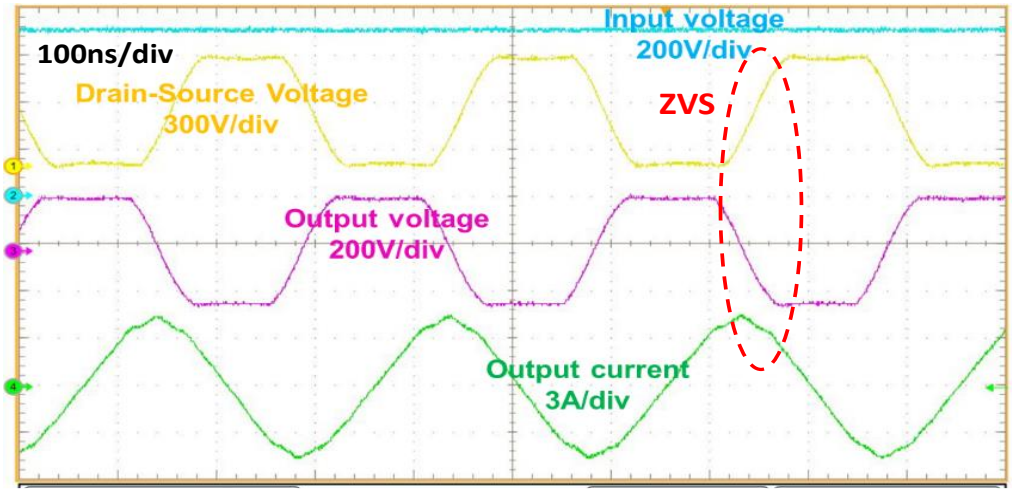
Traditional Qg plot with gate dominated by Qgd charging/discharging process
Turn-on and turn-off use the same Qg-Vgs plot

$$Iload * Rg \leq (Vth + Vg,min)\frac{(Coss + Cparasitic)}{Cgd}$$

3.38 MHz operation of 1200V SiC MOSFET (with ZVS turn-on)







Demonstrated almost zero switching loss

*Guo and Huang at WIPDA 2015

Achieving Zero Switching Loss

- Hard switching application

E_{on} $=E_{on}$(measured)+ E_{oss} + Eoss (diode + load cap)
E_{off} $=E_{off}$(measured) $-E_{oss}$ ~ 0 within ZTL region
$E_{total}=E_{on}+E_{off}=E_{on}$(measured) + E_{off}(measured)+ Eoss (diode + load cap)
Gate drive loss ~ fs*Vg*Qg (favors GaN)

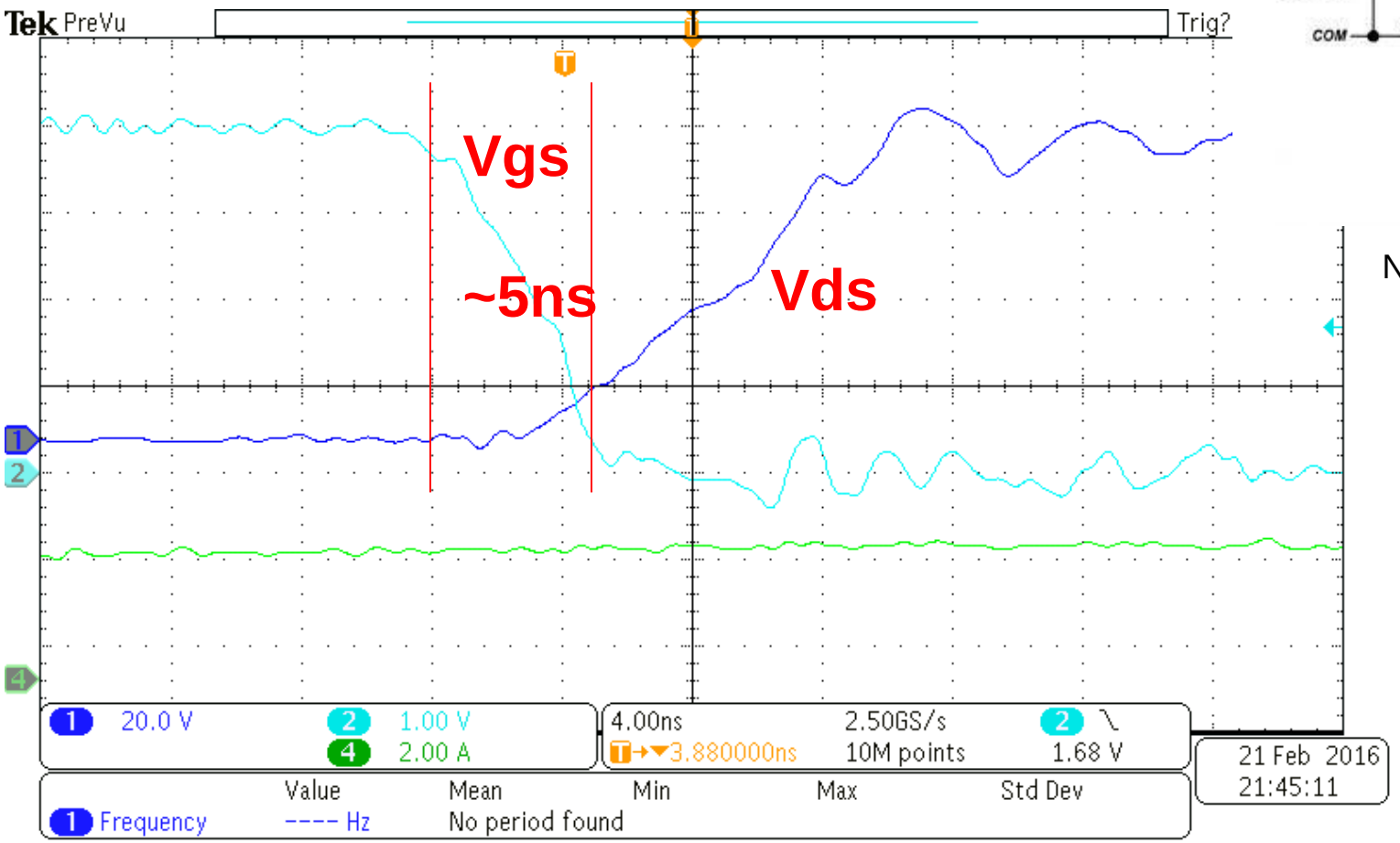
- ZVS soft switching application

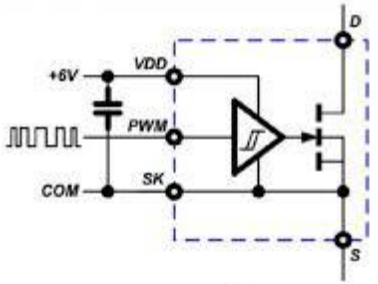
E_{on} ~ =0
E_{off} = E_{off} (measured) $-E_{oss}$ ~0 within ZTL region
$E_{total}=E_{on}+E_{off}$ = 0
Gate drive loss ~ fs*Vg*Qg (favors GaN)

- **Switching frequency is less or no longer a constraint**
- **Ron can go down so RMS current less a concern (FOM=$*mohm)**

Integrating Driver With the GaN (hard driven GaN)

650V GaN turn-off waveform





Navitas GaN

- Zero Turn-off Loss (ZTL) can be achieved in hard-driven GaN
- Turn-on loss can be eliminated by Zero Voltage Switching (ZVS)

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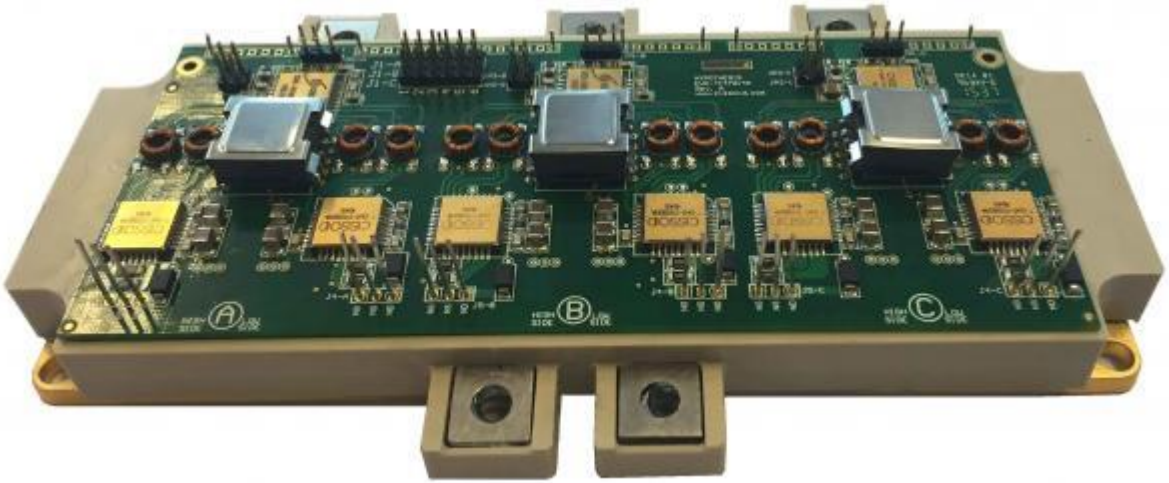
Motivation: Increasing Power Density



- Power density=PD=Po/Volume
- Rja ~ 1/(useful surface area) = 1/[K*Volume]
- Ploss = (Tjmax-Ta)/Rja= (Tjmax-Ta)*K*Volume
- So PD=[Po/Ploss] *K* (Tjmax-Ta)

Reducing losses (Conduction & Dynamic)

Packaging?

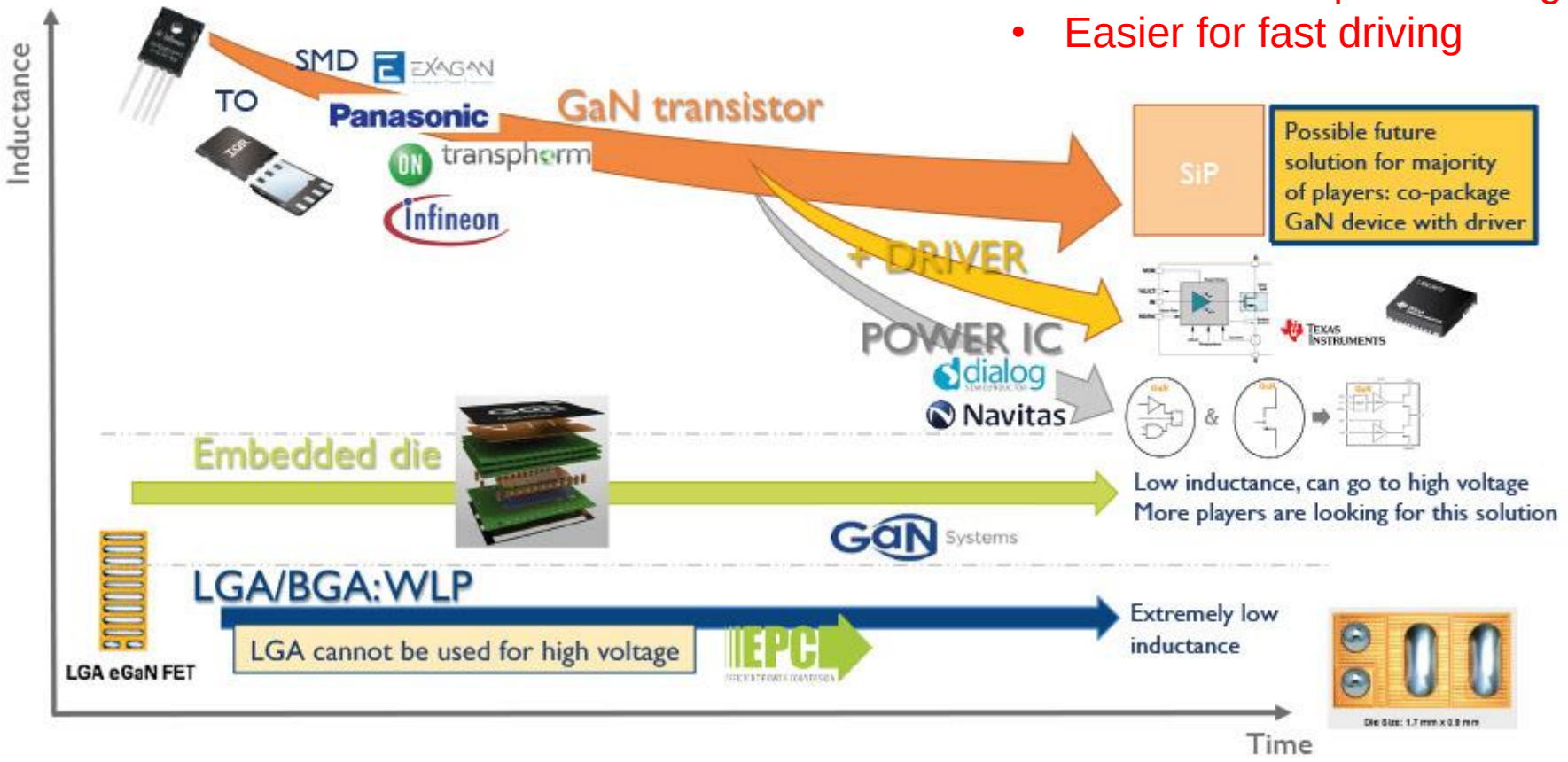
Increasing junction temperature

GaN Packaging Advantage for High Density

Power GaN packaging roadmap

(Source: Power GaN 2017: Epitaxy, Devices, Applications, and Technology Trends 2017 report, Yole Développement, October 2017)

- Easier for low parasitic layout
- Easier for low profile design
- Easier for fast driving



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Topside Cooling GaN

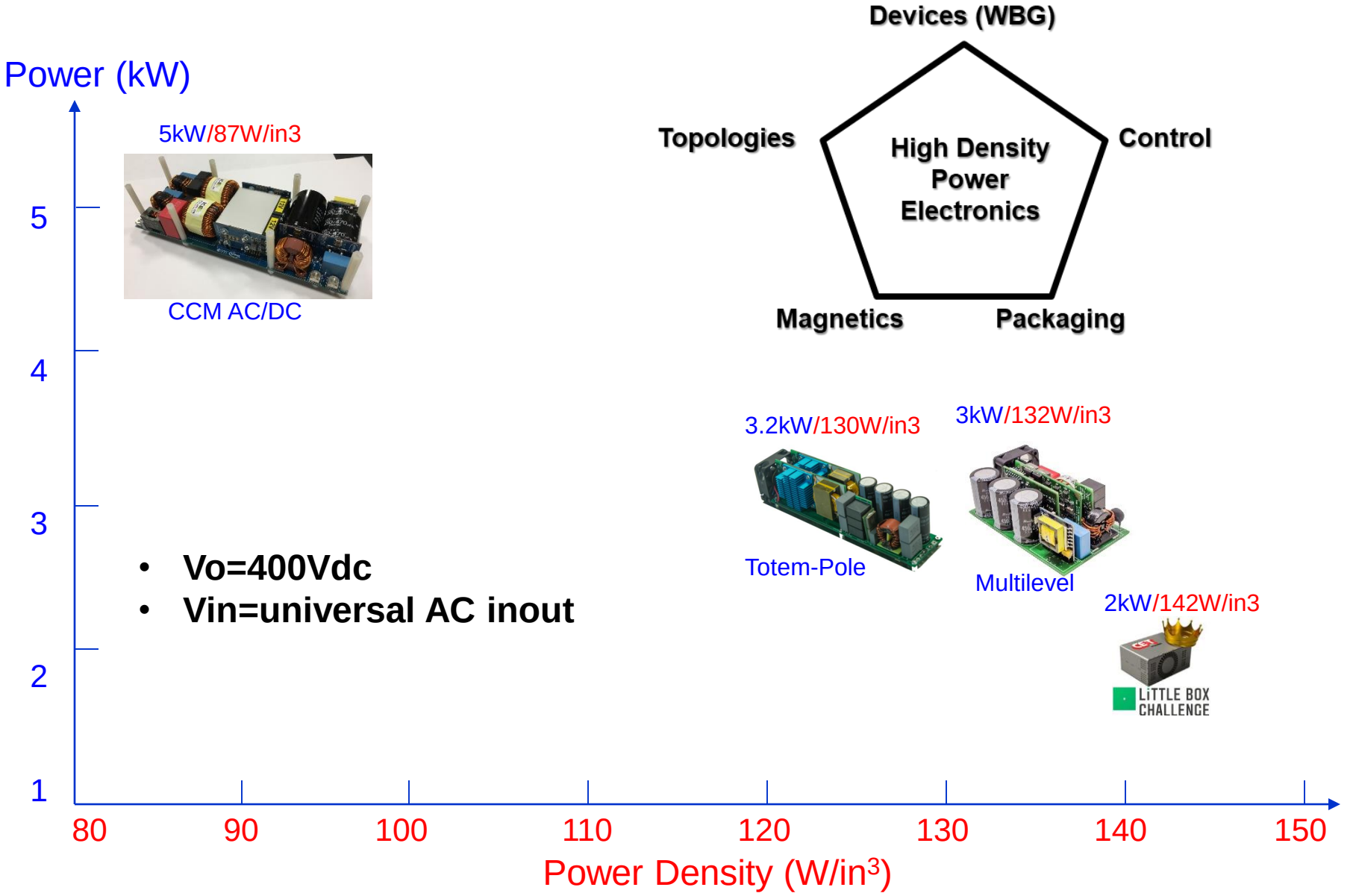
ALL Switch GaN Power Switch - DAS-02265-001
V22N65A

Key Performance Parameters

Parameter	Value
V_{DS} (V)	650
$R_{DS(ON)}$ (mΩ)	22
Q_G (nC)	41
$I_{D,pulse}$(A)	180
I_D (A)	80

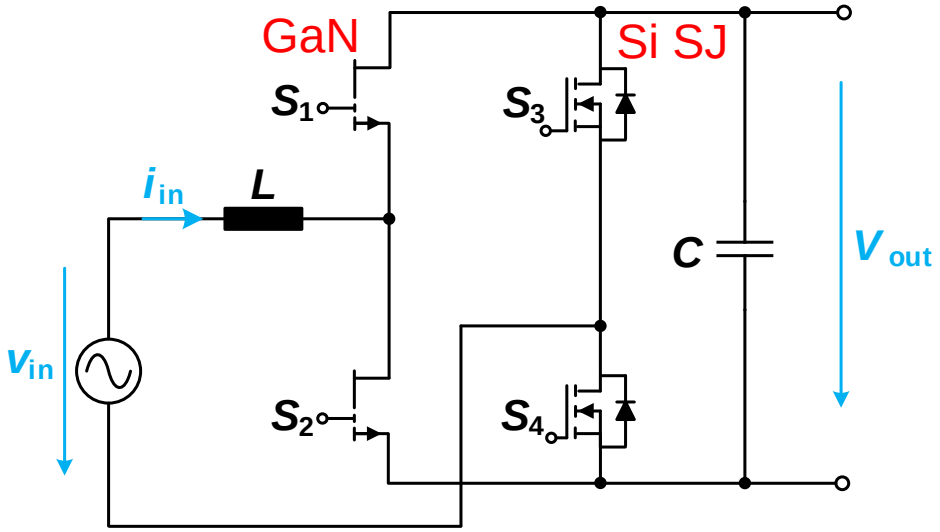
VisIC Technologies

HDPE Example: AC-DC Power Conversion



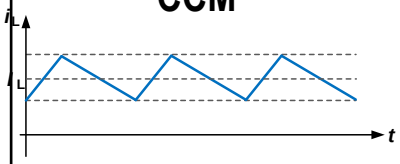
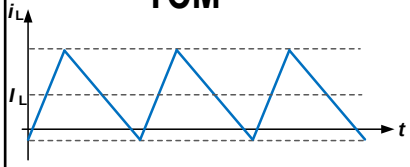
Bridgeless Totem-Pole PFC

- Reverse recovery issue of Si Super-Junction MOSFETs is the major concern for hard-switching operation of this topology.
- Soft-switching significantly increases the control complexity and the reliability is also a concern.
- With GaN or SiC devices, this topology can work under hard-switching conditions.
- Hybrid GaN/Si solution lowers cost!



J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase AC supplies and using either single or split DC rail voltage outputs," *Proceedings of APEC'95*, Dallas, TX, USA, 1995, pp. 473-479 vol.1.

CCM (Hard Switching) vs TCM (Soft Switching)

	CCM	TCM
		
Conduction Loss	Low	High
Switching loss	higher (hard switching)	Very low (soft switching)
Switching frequency	Low (around 100kHz)	High (100kHz~3MHz)
Efficiency	High	High
dv/dt noise	High	Low
EMI filter size	Medium (Easy to predict)	Small (Hard to predict)
Density	Medium	High
Control Complexity	Low	High

- TCM has more potential for high density

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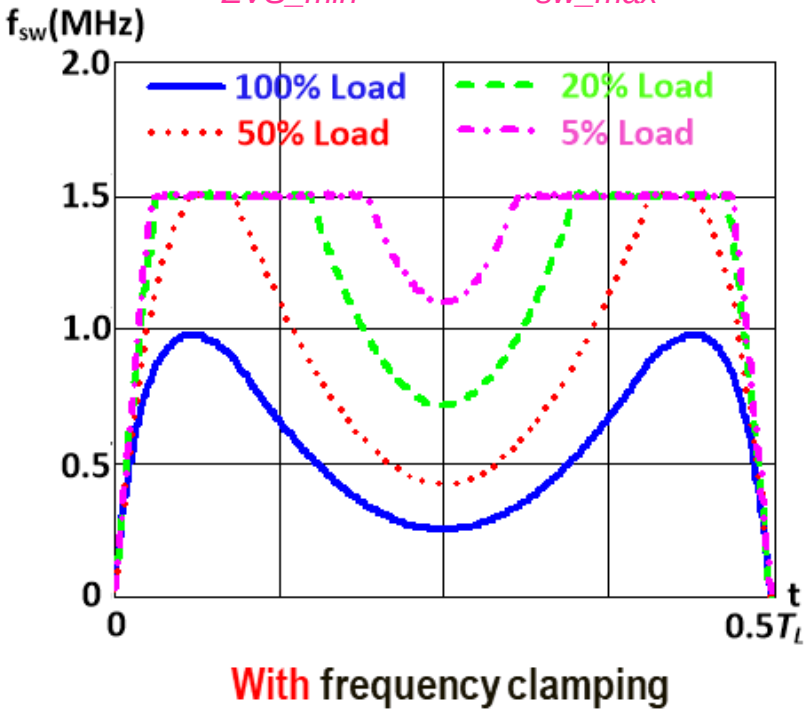
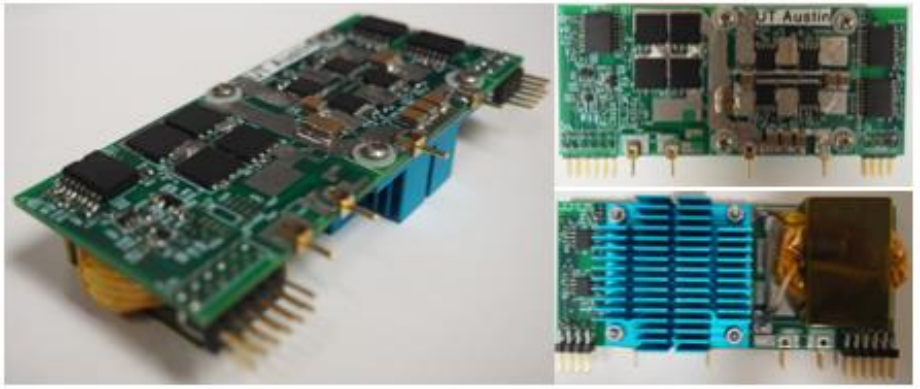
PFC Hardware Implementation (3.2 kW TCM Totem-Pole PFC)

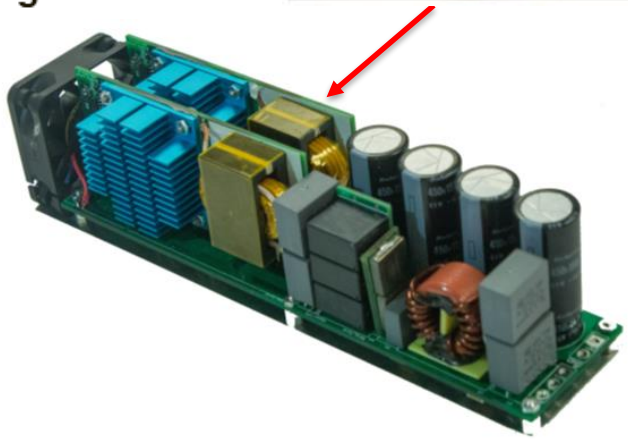
- Parameters: L= 9.5μH, C_{oss}=120pF, V_{in}=240V/AC, V_o=400V, T_{ZVS_min}=30ns, f_{sw_max}=1.5MHz. P=1.6kW for each phase; 2-Phases



With frequency clamping

- Modular GaN PFC power stage
- Each phase: 3.7 x 1.6 x 0.7inch^3 or 386 W/in^3





Navitas

- NV6117, 650V, 120mohm
  - ✓ 7.9x1.8x1.8inch^3, 130W/inch^3

*APEC 2018

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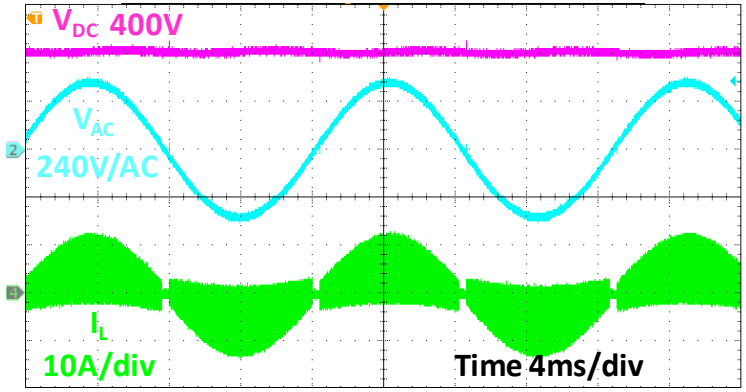
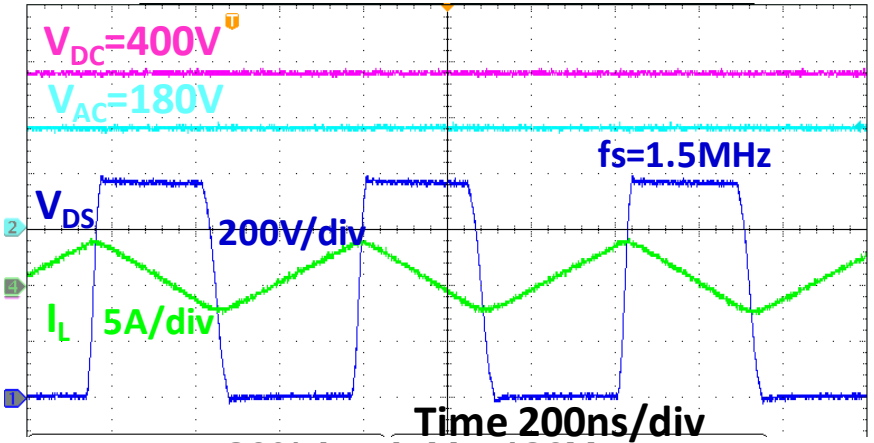
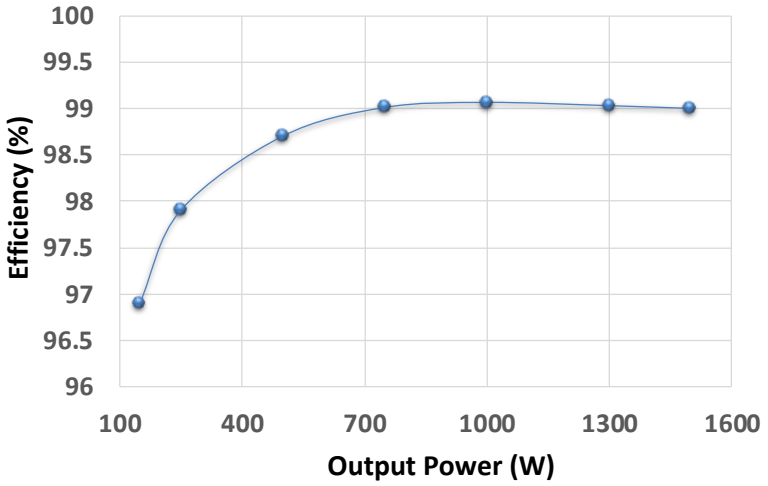
99% PFC Efficiency Achieved

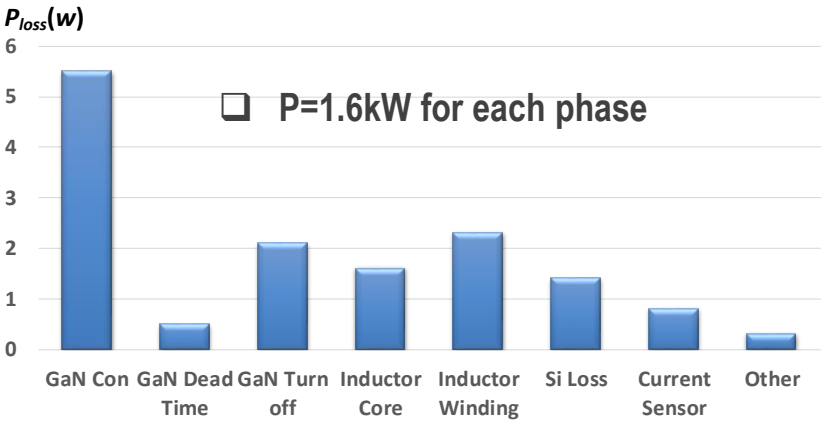
- Parameters: L= 9.5μH, C_{oss}=120pF, V_{in}=240V/AC, V_o=400V, T_{ZVS_min}=30ns, f_{sw_max}=1.5MHz. P=1.6kW for one phase





20% load, V_{in}=180V.





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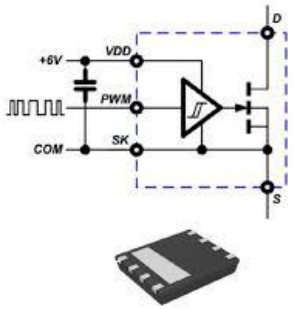
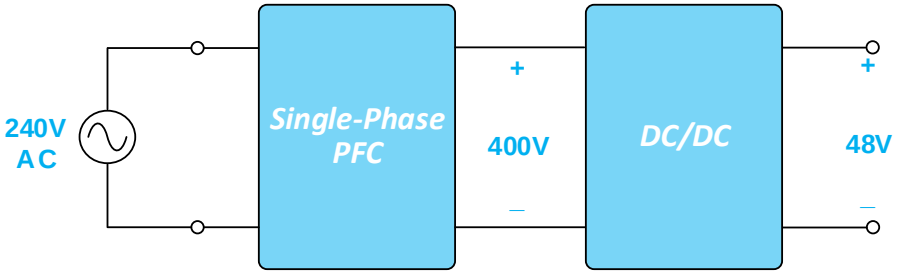
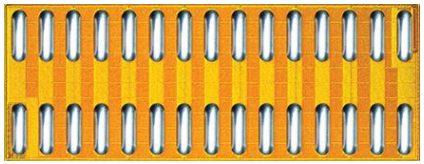
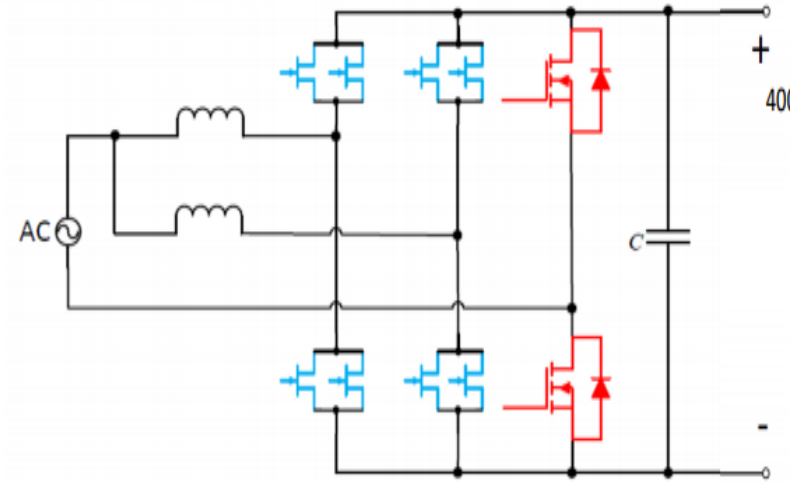
All GaN 3.2 kW power supply unit

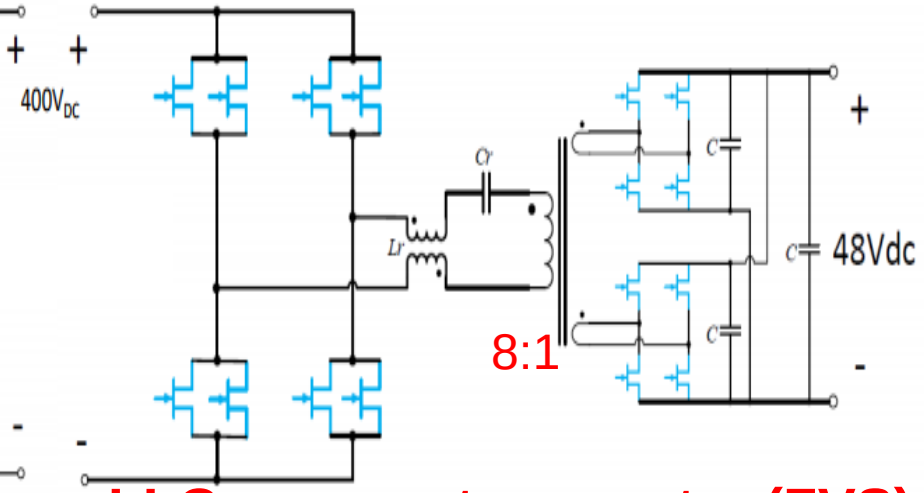








Totem Pole PFC (ZVS)

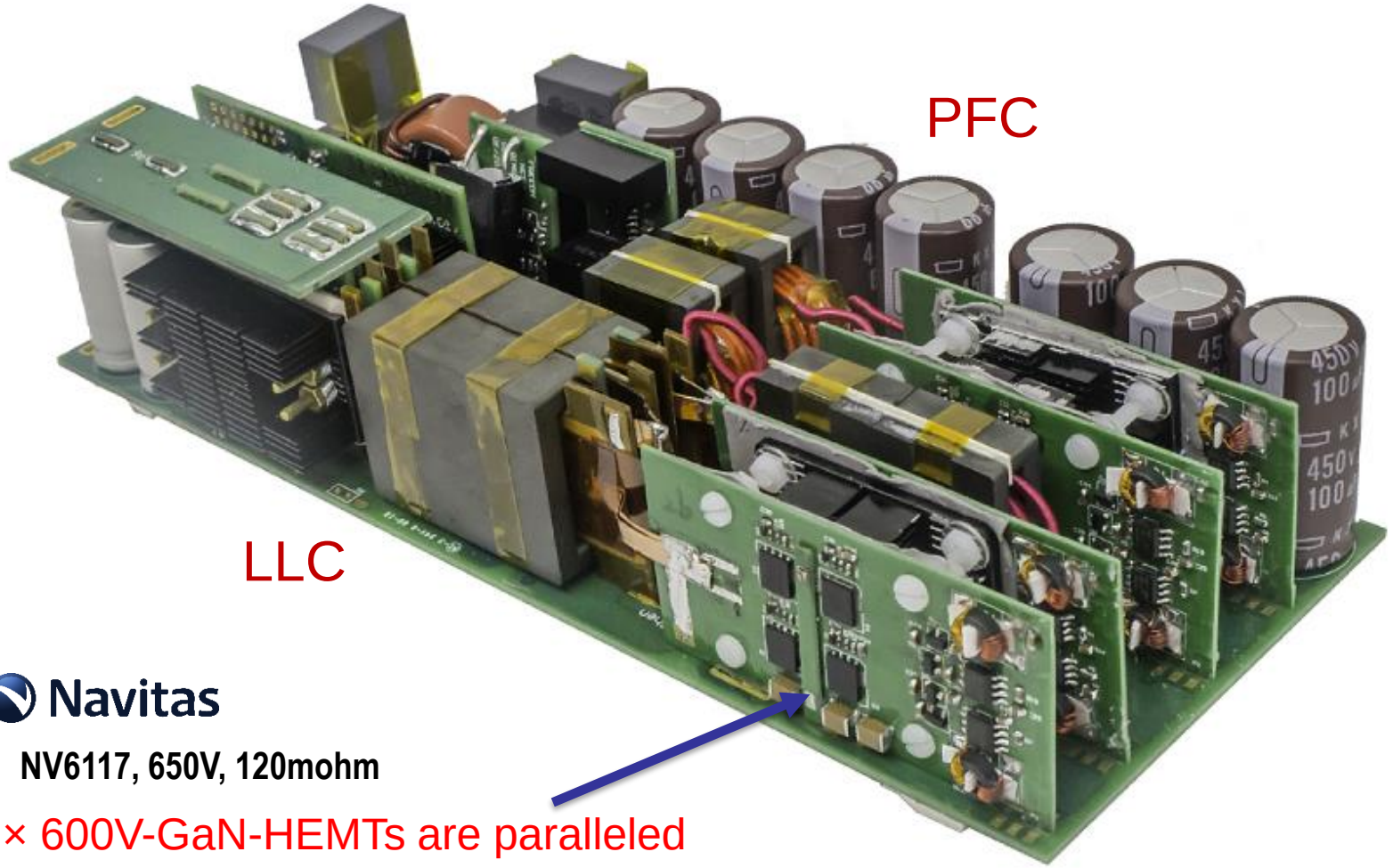


LLC resonant converter (ZVS)

- Achieving high power by device parallel /multiphase
- Achieving low loss by ZVS and ZTL
- Frequency fsw becomes a design variable for power density

▪ 3.2 kW All-GaN Power Supply Unit (PSU)

- Vac=240V, Po=3200W, Vo=48V, Power Density=60W/in^3



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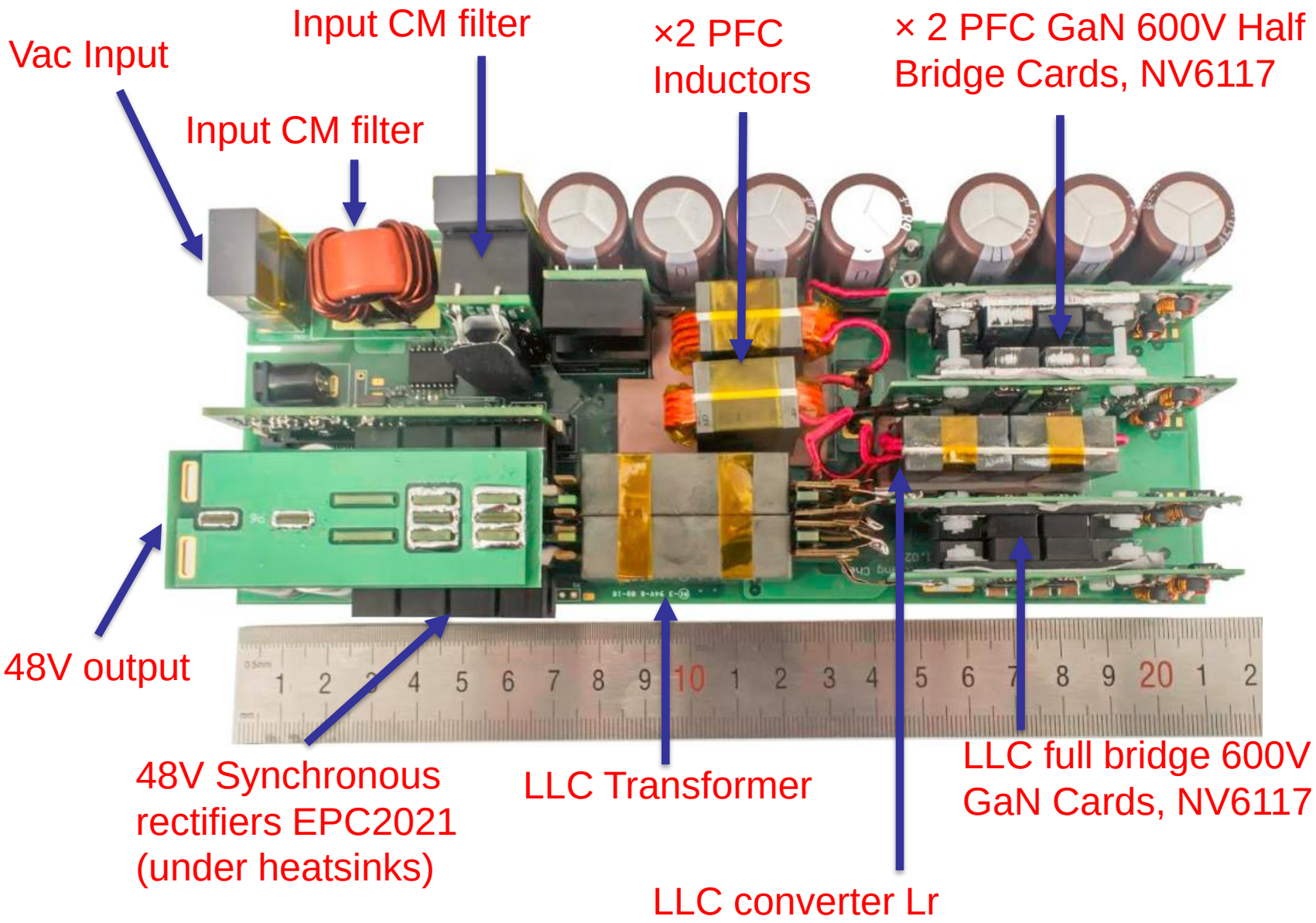
▪ 3.2 kW All-GaN Power Supply Unit (PSU)



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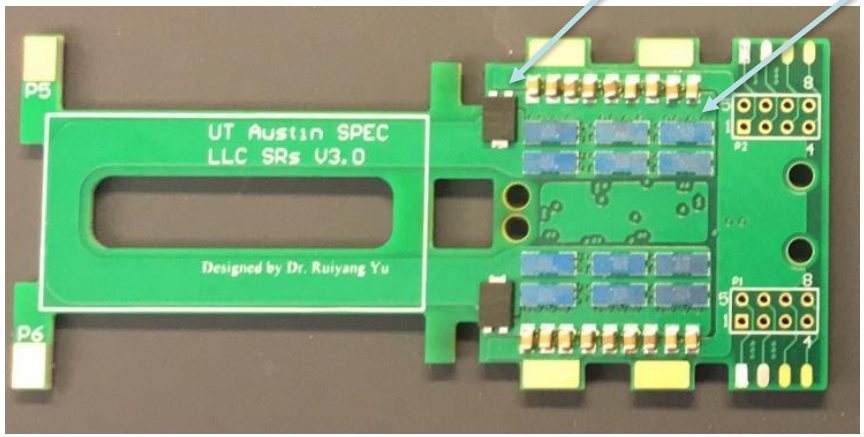
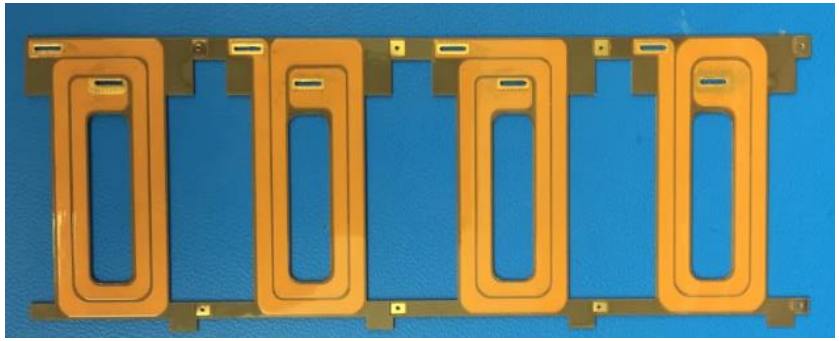
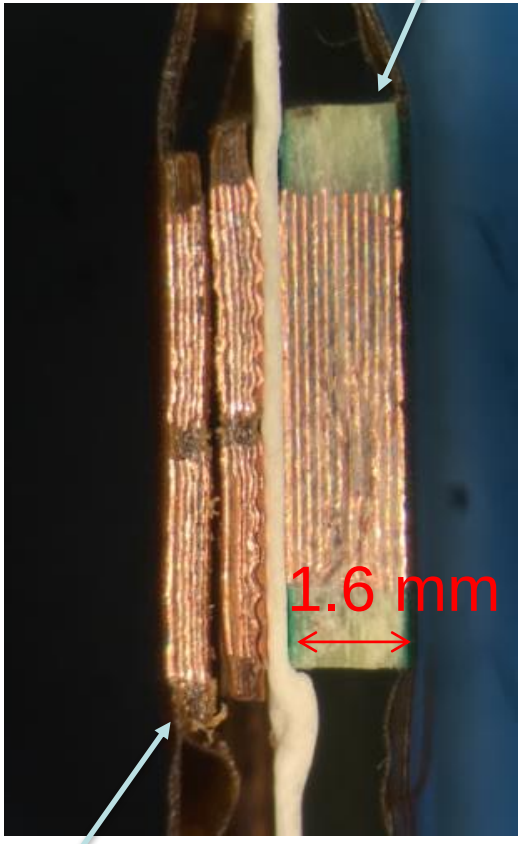
Transformer design



1 turn transformer secondary winding and 80V GaN SRs (Ipk=100A)



8 turns transformer primary windings



Cp=60pF

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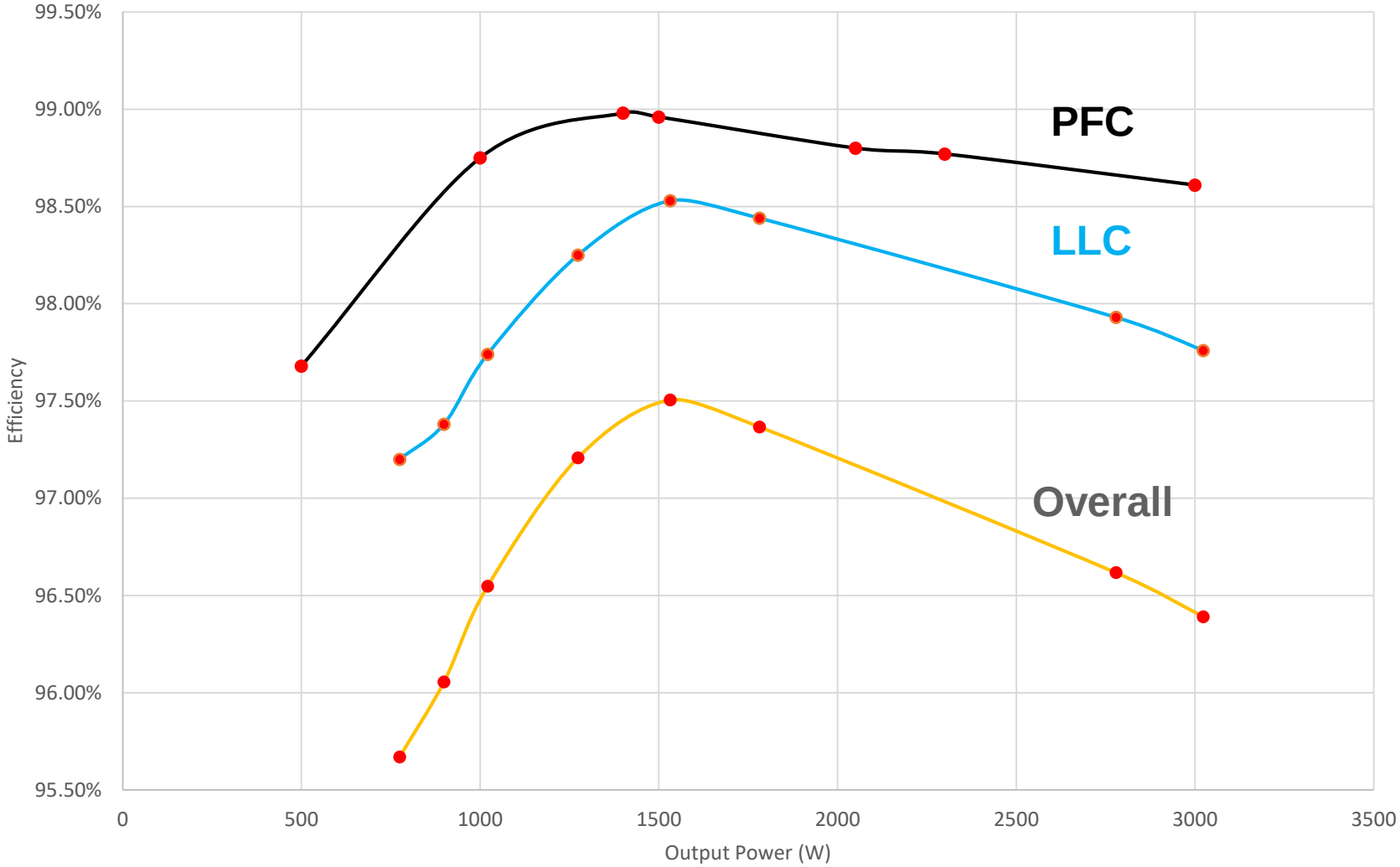
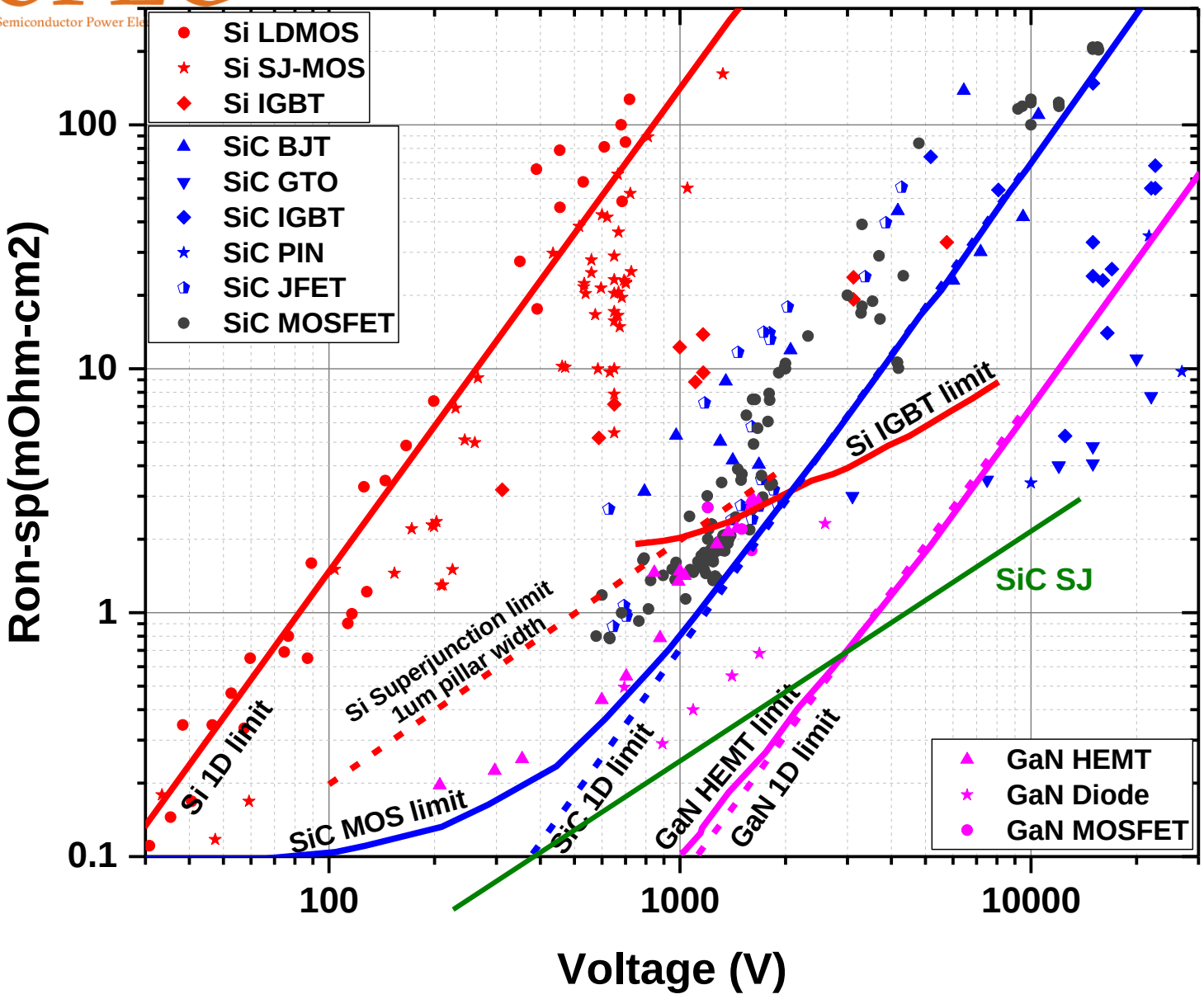
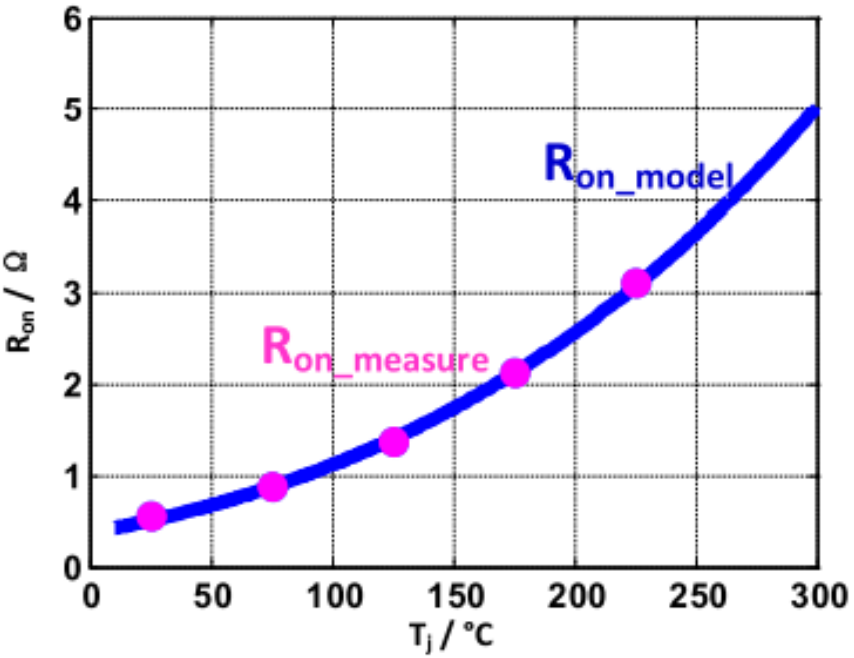
Efficiency Summary of 3.2kW GaN Power Supply



How about HV SiC MOSFET



15kV SiC MOSFET: 10-20X Higher in BV

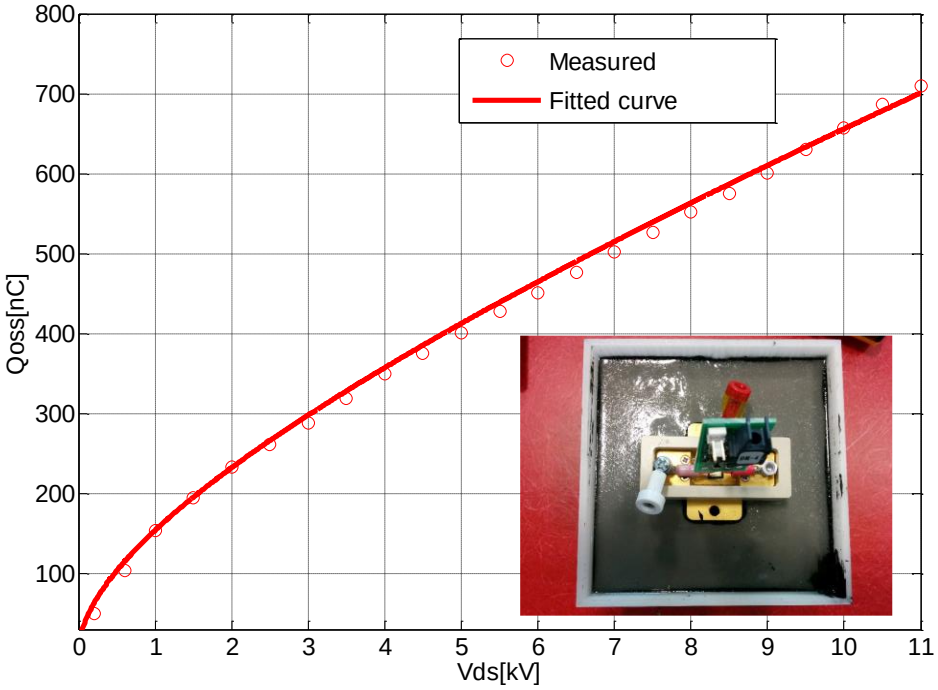


$$R_{on} = R_0(\frac{T_j}{T_0})^2$$

$$R_0 = 0.875\Omega \quad T_0 = 348.16K$$

$$Q_{oss} = 4.08 \cdot 10^{-9}\sqrt{V_{ds}} + 24.8 \cdot 10^{-12}V_{ds}(\text{nC})$$

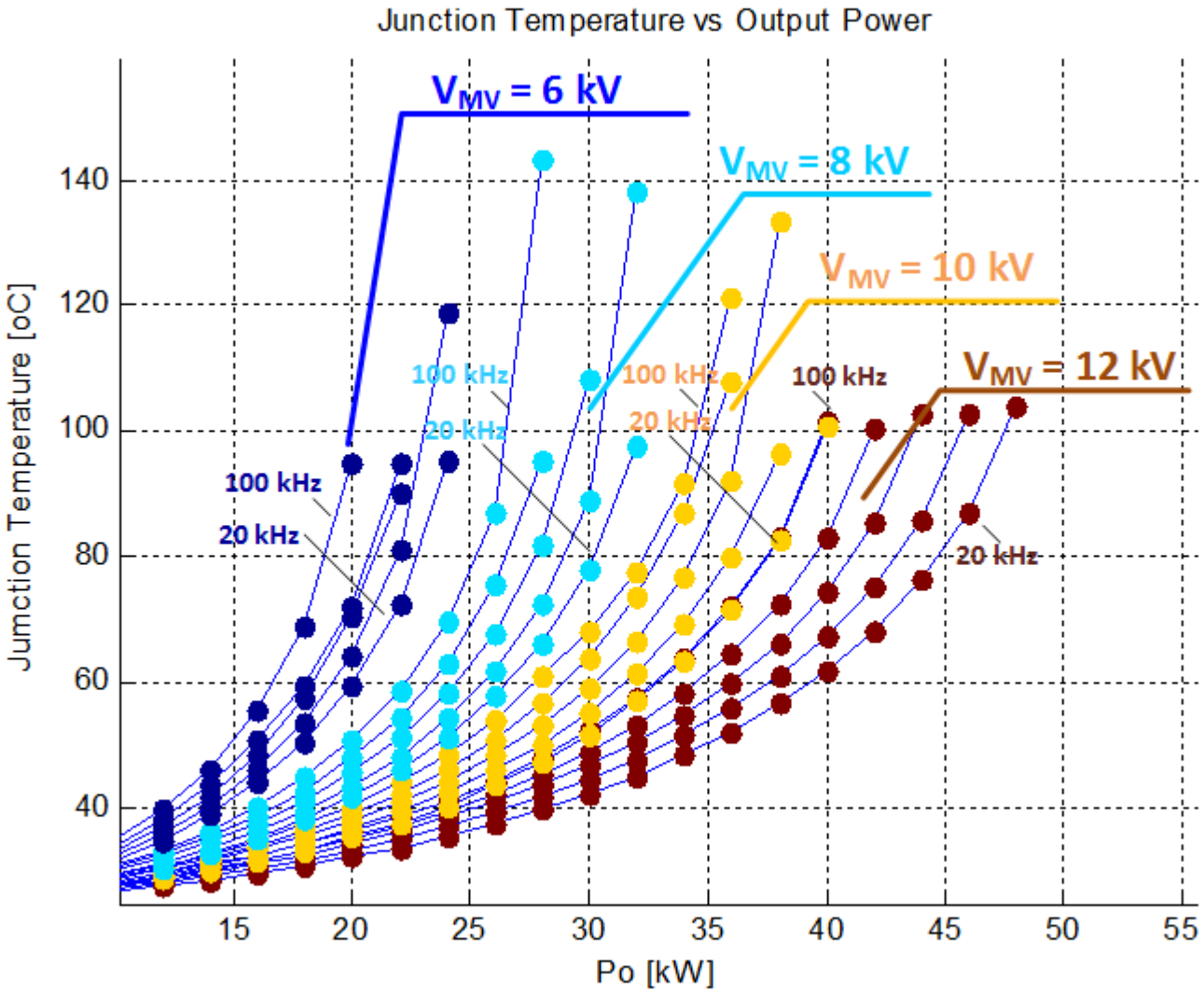
Output Charge of 15kV SiC MOSFET & JBS



Li Wang, Qianlai Zhu, Wensong Yu, Alex Q. Huang ,"A Study of Dynamic High Voltage Output Charge Measurement for 15 kV SiC MOSFET," ECCE2016

15 kV SiC MOSFET @20khz-100kHz

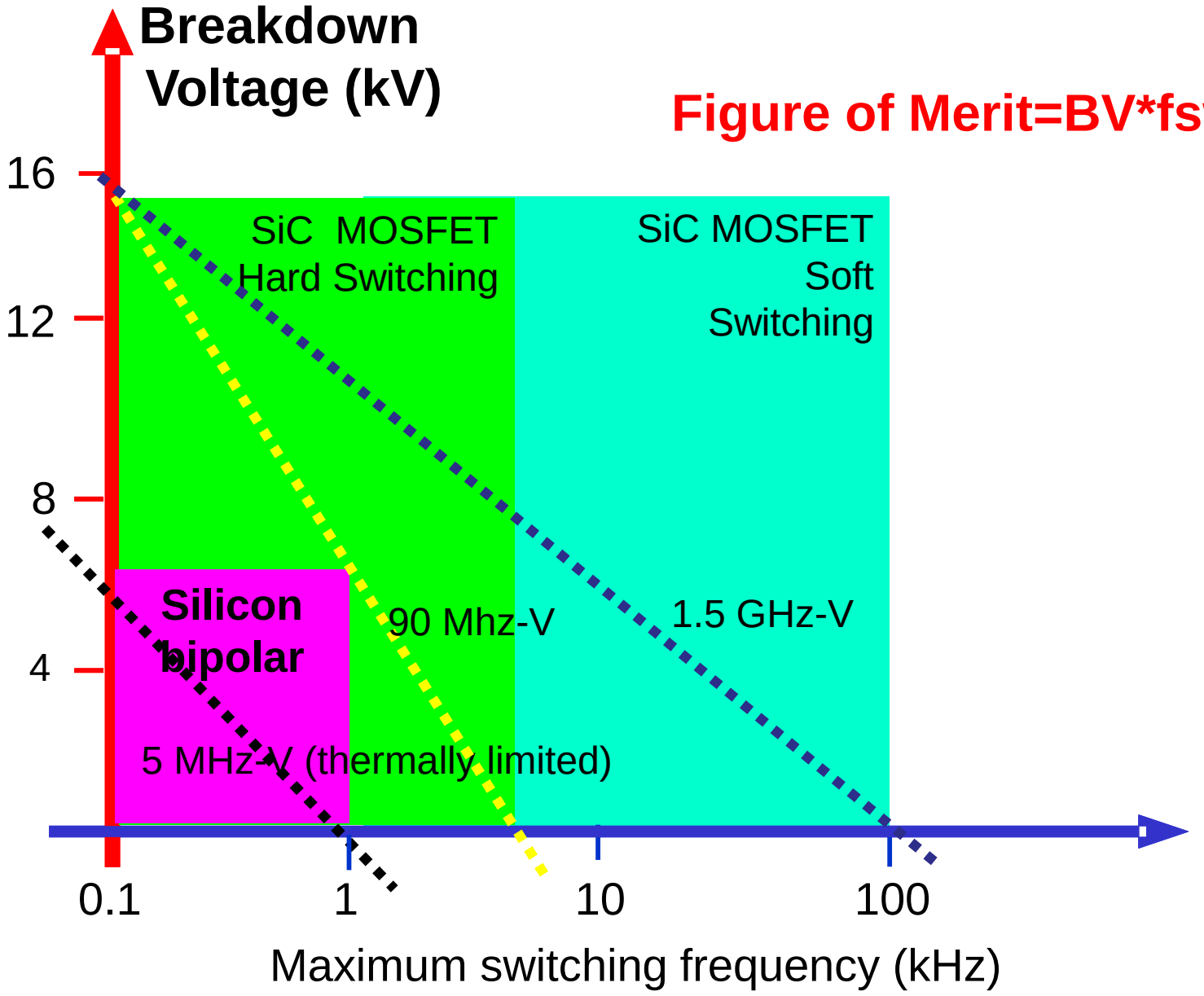
Higher DC link voltage, Better device utilization



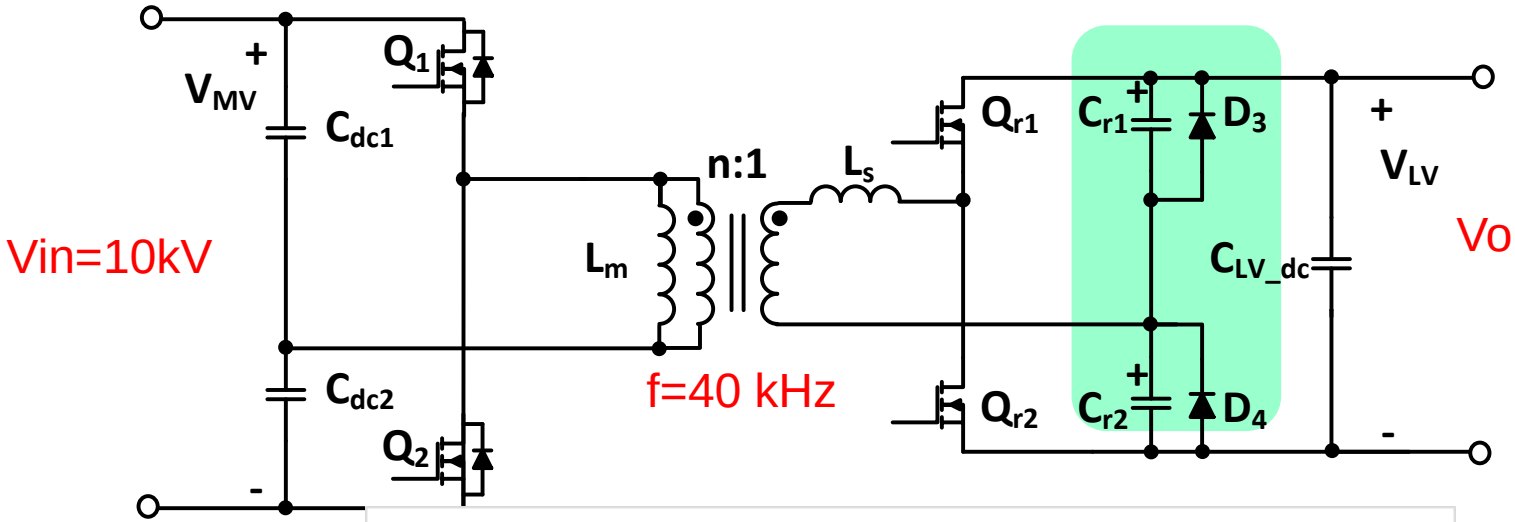
Half Bridge/ZVS/Only two 15 kV MOSFET used

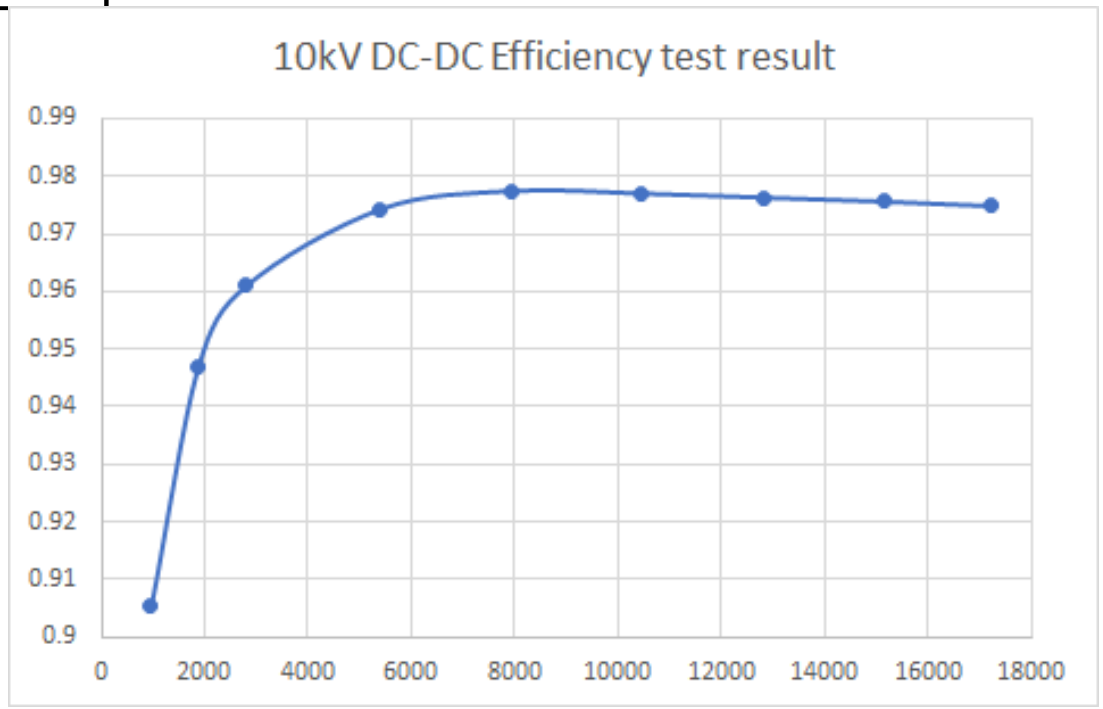
Total SiC die size=2 cm^2

15 to 300 X improvements in FOM



10 kV DCX: Two 15 kV SiC MOSFETs





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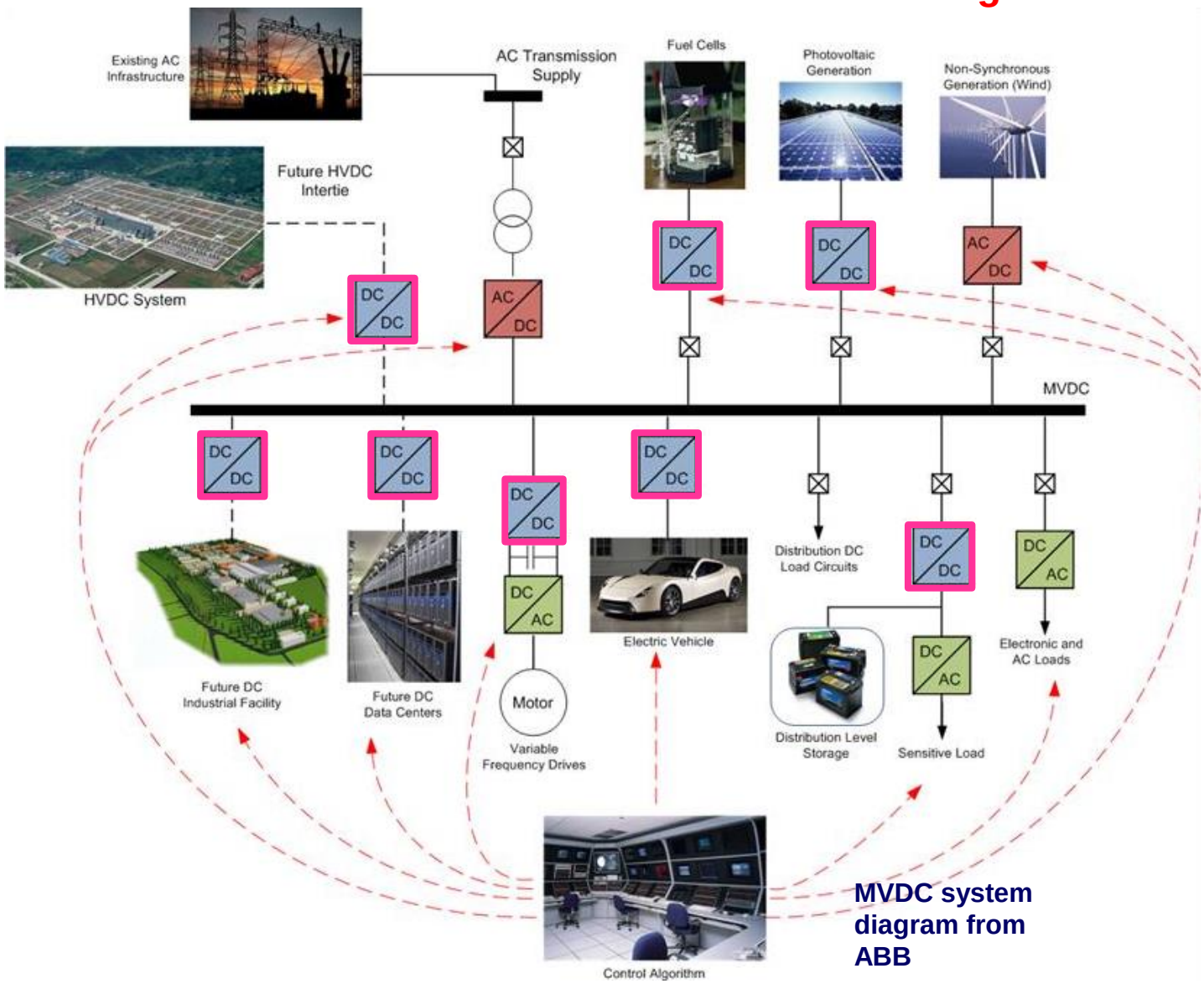
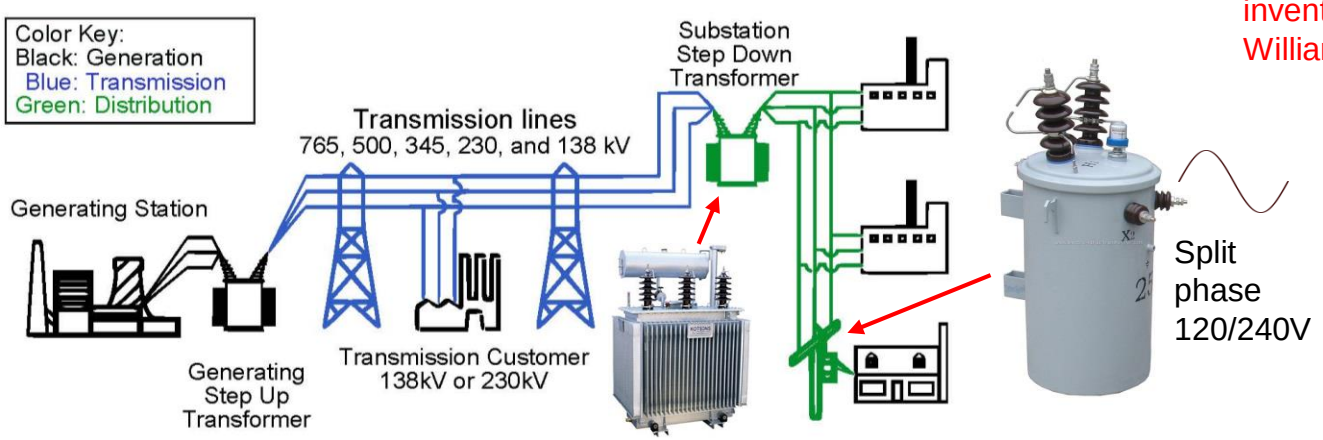
MVDC Application

MVDC Voltage: 10 to 20 kV



MVDC system diagram from ABB

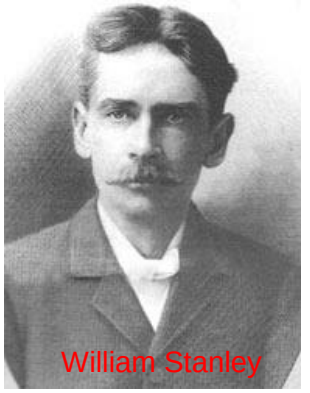
Grid Edge Control Challenge



Electricity grid in North America. Source: [1]

Transformer History: invented in 1886 by William Stanley

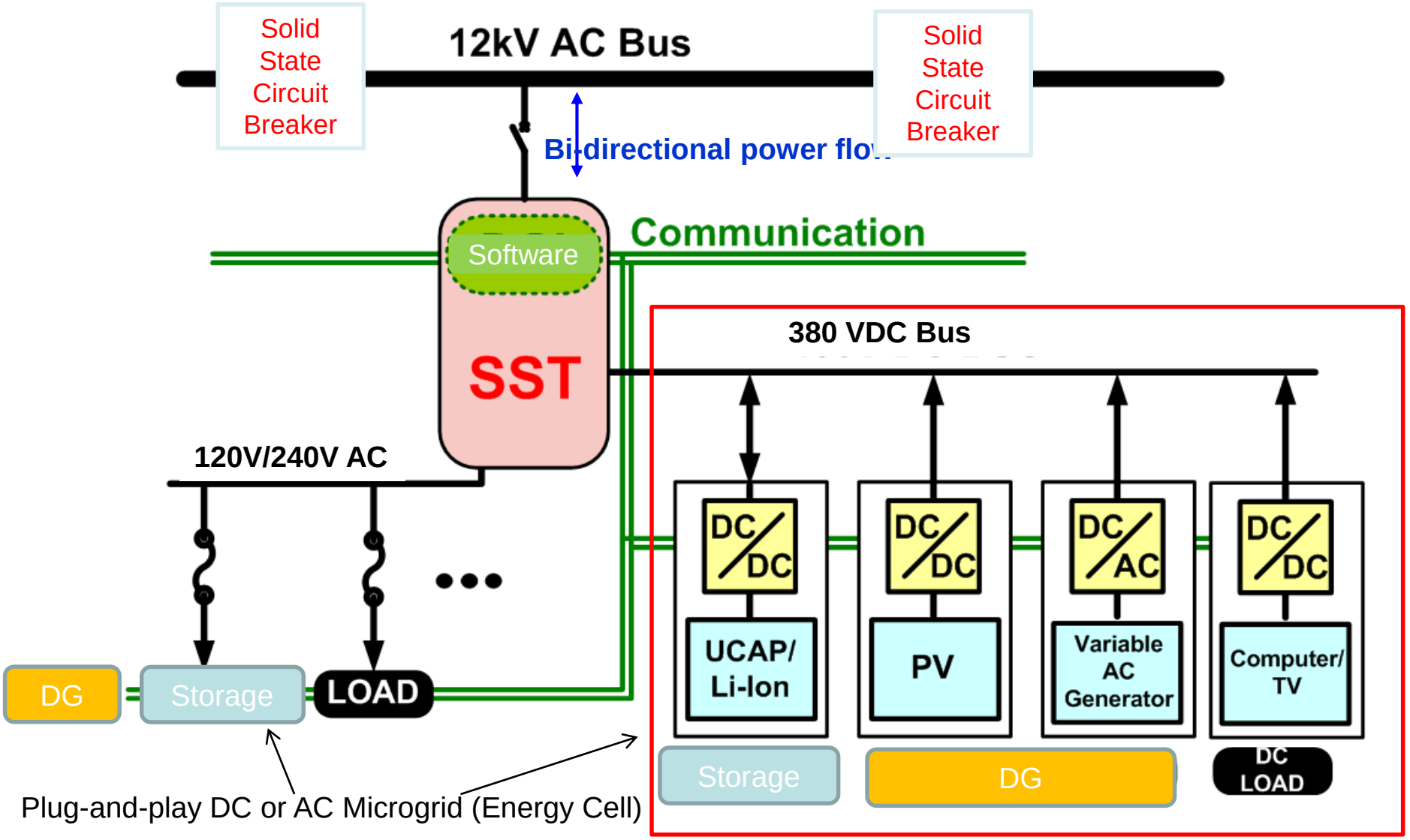
Distribution grid transformer (pole mounted)



- Designed for unidirectional power flow and century-old transformer technology with little controllability
- Requires a wide spectrum of products for power quality improvement (SVC, active filter, voltage regulator, DVR, etc.)
- Strong coupling and won't isolate harmonics/other disturbances
- Not friendly for integration of renewable energy source (DC-typed sources need more conversion stages, synchronization), EV, electronic load

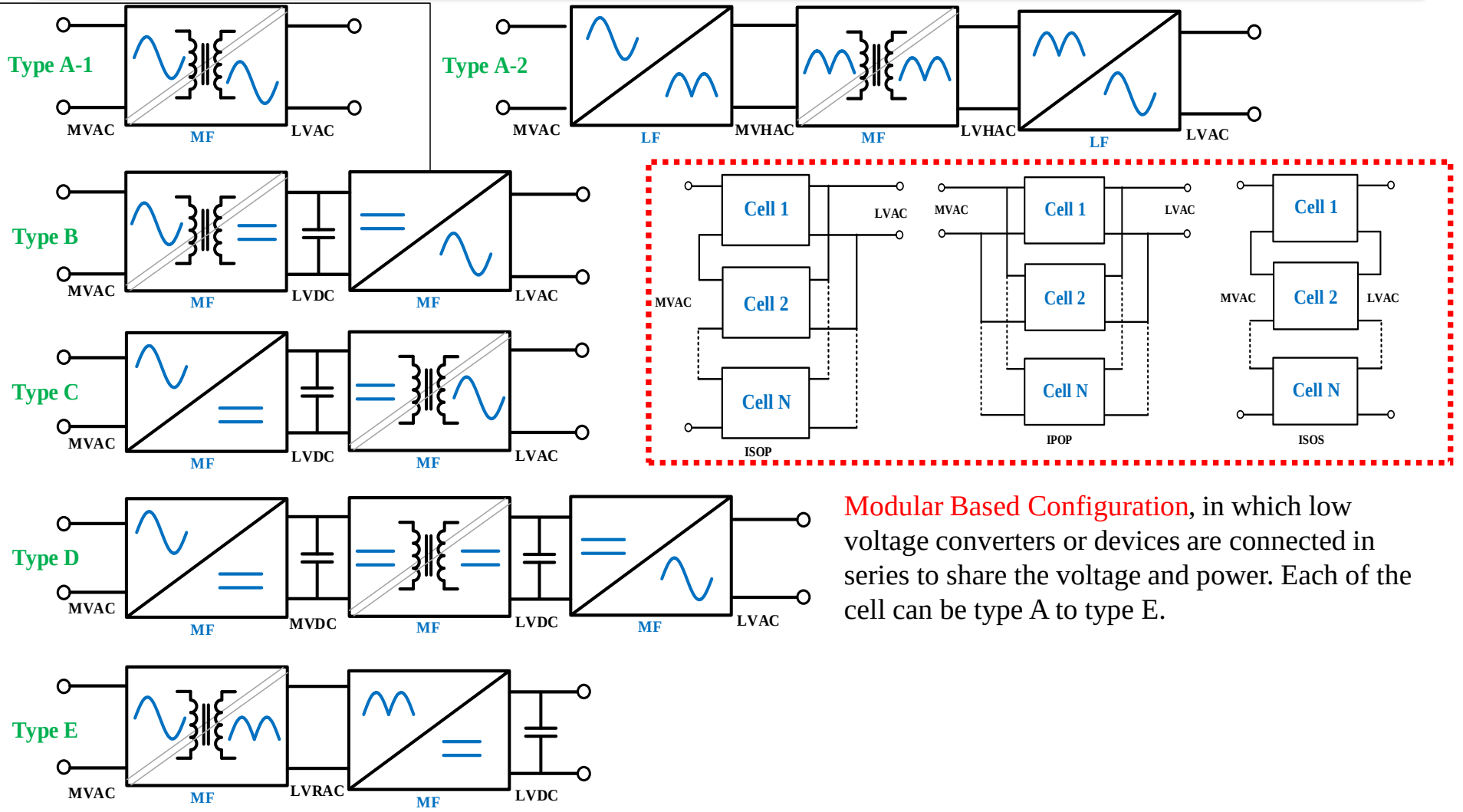
[1] Electricity grid simple- North America" by United States Department of Energy, SVG version by User:J Jmesserly - http://www.ferc.gov/industries/electric/indus-act/reliability/blackout/ch1-3.pdf Page 13 Title:"Final Report on the August 14, 2003 Blackout in the United States and Canada" Dated April 2004. Accessed on 2010-12-25. Licensed under Public domain via Wikimedia Commons http://commons.wikimedia.org/wiki/File:Electricity_grid_simple-_North_America.svg#mediaviewer/File:Electricity_grid_simple-_North_America.svg

SST enabled distribution architecture



- **FREEDM System: Core concept behind NSF's ten-year ERC investment**

Power Electronics Solutions

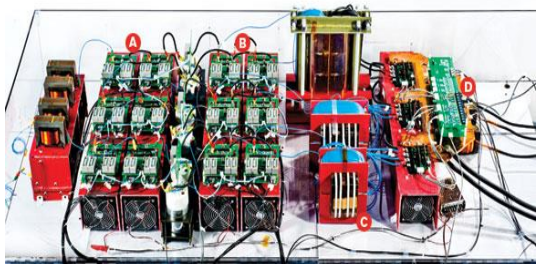


Modular Based Configuration, in which low voltage converters or devices are connected in series to share the voltage and power. Each of the cell can be type A to type E.

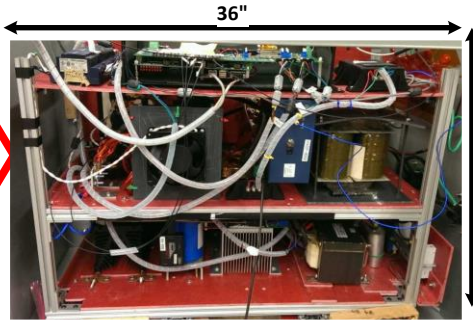
Xu She, Alex Huang, "Review of Solid state Transformer in the Distribution system: From components to Field application," in Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 4077-4084.

Solid State Transformer Prototypes

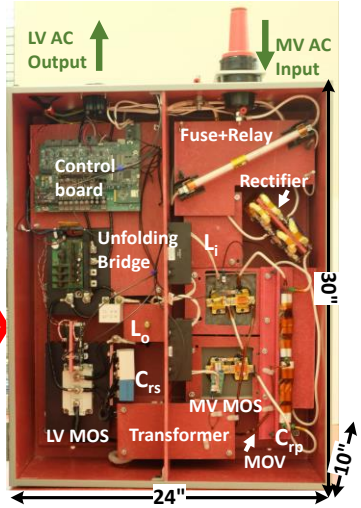
60Hz Transformer



Gen- 1 SST: Si-based (6.5 kV IGBT 3kHz)



Gen- 2 SST: SiC-based (15 kV SiC MOSFET 10 kHz)

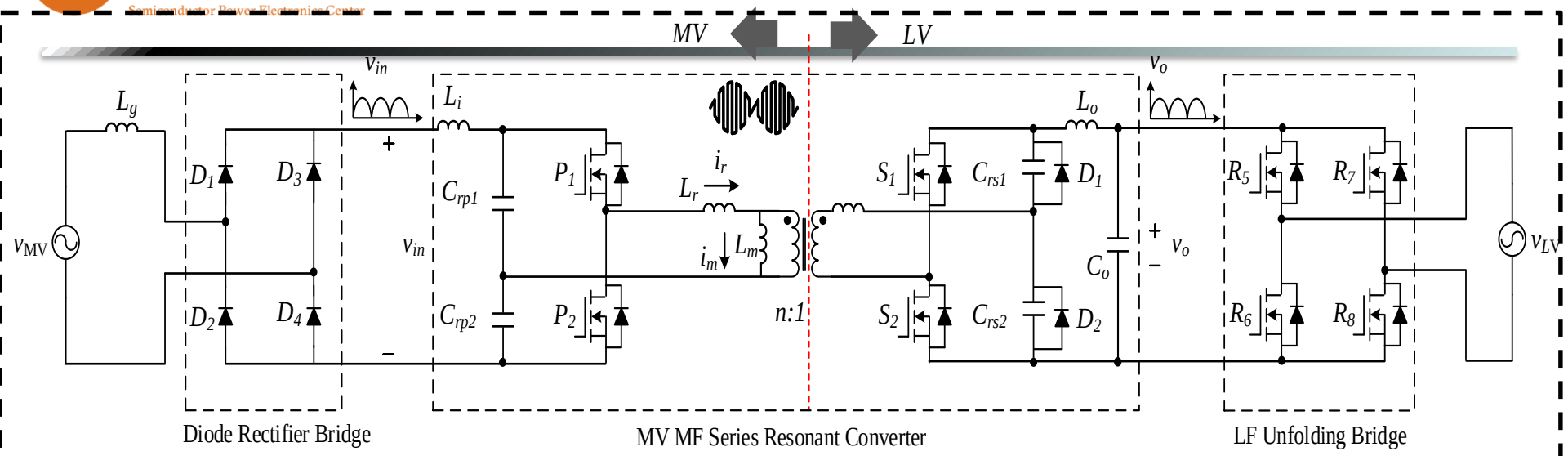


Gen- 3 SST: SiC @ 40 kHz

Controls **Topology /magnetics** **Wide Bandgap Devices**

- 7.2 kV single phase transformer for distribution system
- Numerous advanced features and smart functions

Gen-III SST: Direct AC-AC Conversion (Type A-2)



Type A-2: (Uni-directional)

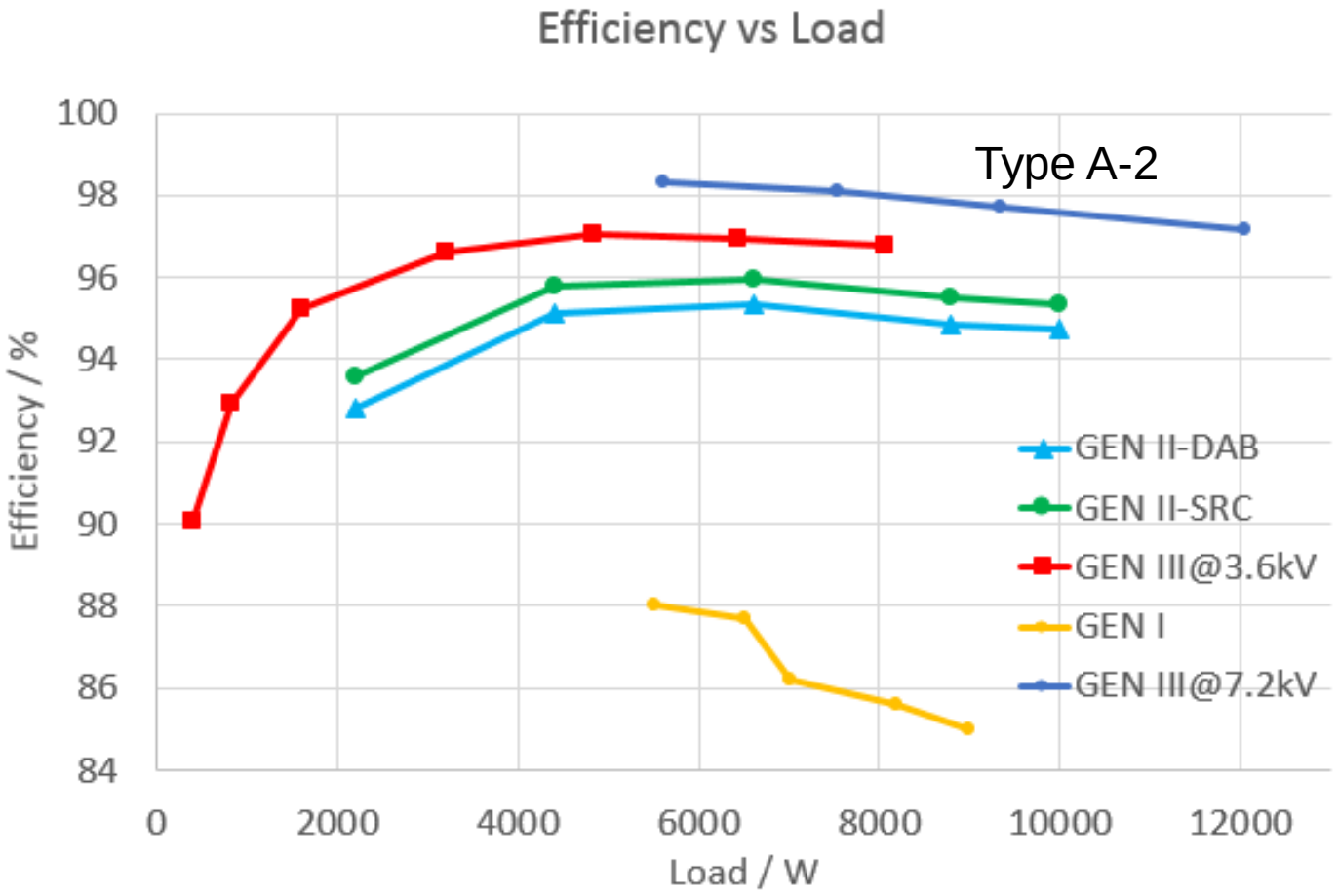
- Use diode bridge to replace MOSFET bridge: cost effective if only unidirectional power flow is needed. Only two HV SiC MOSFETs needed

Advantages

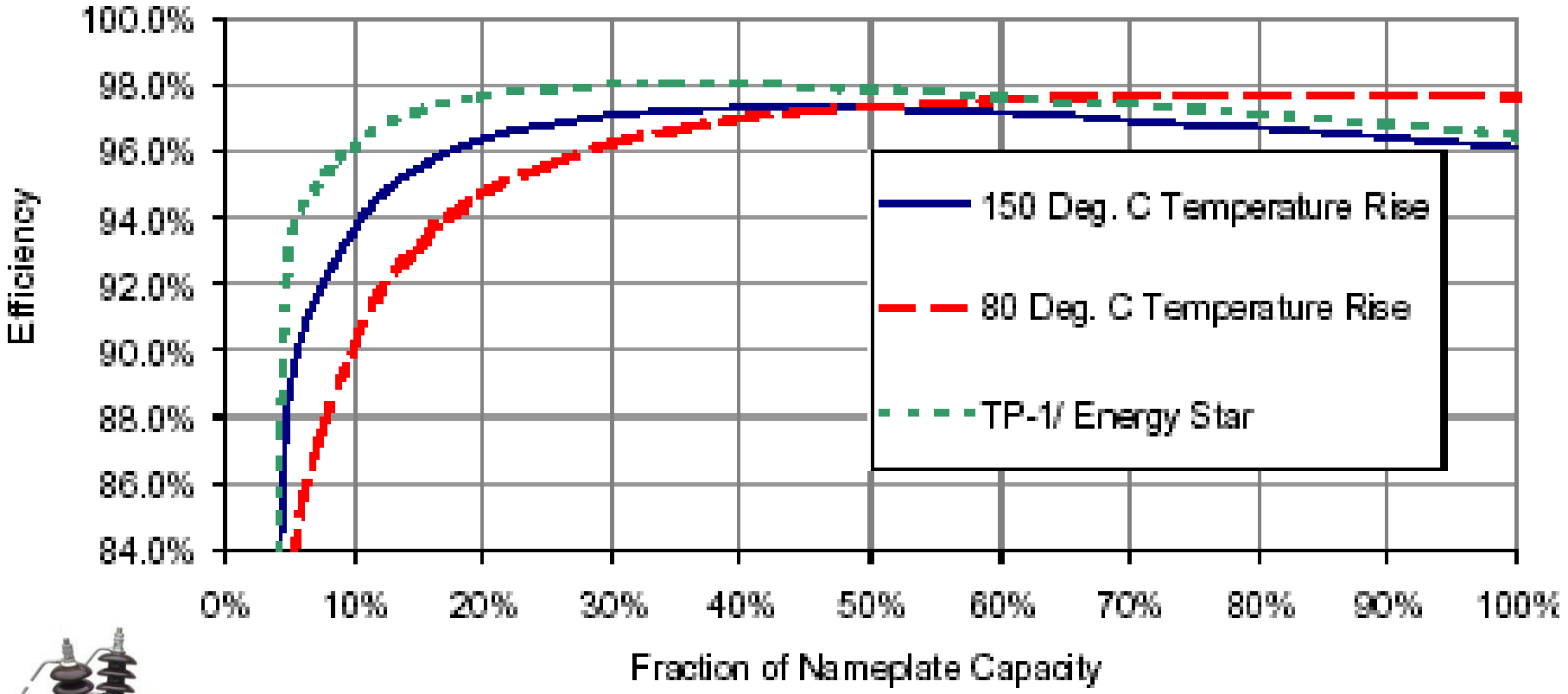
- ❑ **High efficiency: one stage of high frequency power conversion** → **Efficiency**
- ❑ **High power density: 40kHz~100kHz+no dc capacitors** → **Power Density**
- ❑ **Only two MF MV MOSFETs and ZVS guaranteed** → **Reliability + Efficiency**
- ❑ **Current limit capability under over load conditions** → **Functionality**
- ❑ **Minimized system stored energy** → **Safety**

Q. Zhu, L. Wang, A. Huang, K. Booth and L. Zhang, "7.2 kV Single Stage Solid State Transformer Based on Current Fed Series Resonant Converter and 15 kV SiC MOSFETs," in *IEEE Transactions on Power Electronics*.

Measured Efficiency (MV AC- LV AC)



60 Hz transformer efficiency



Conclusion: SST is approaching similar efficiency!

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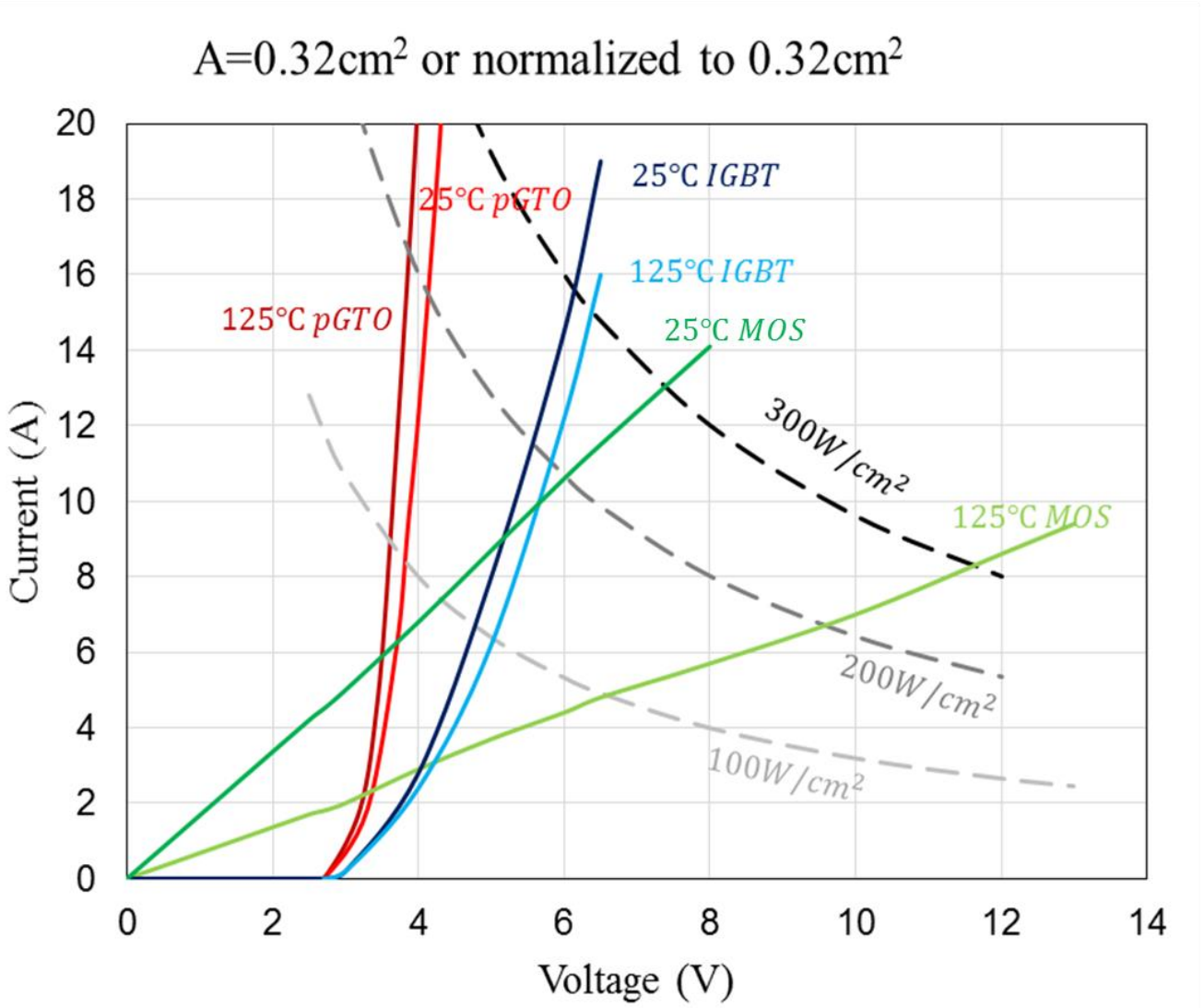
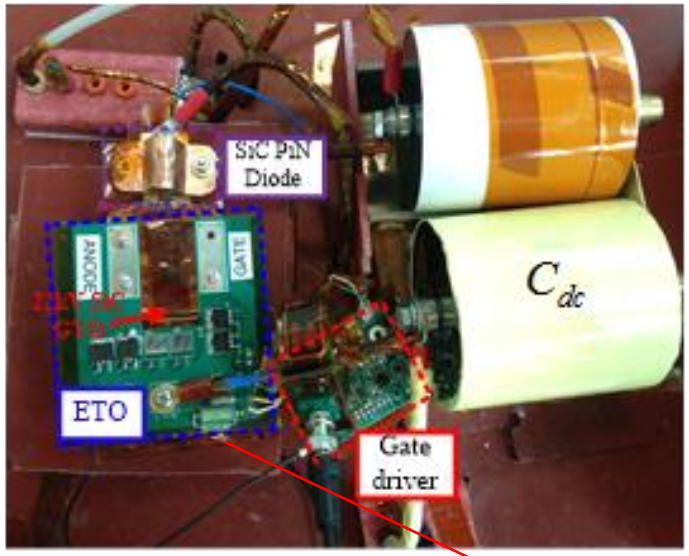
15kV SiC GTO, n-IGBT and MOSFET

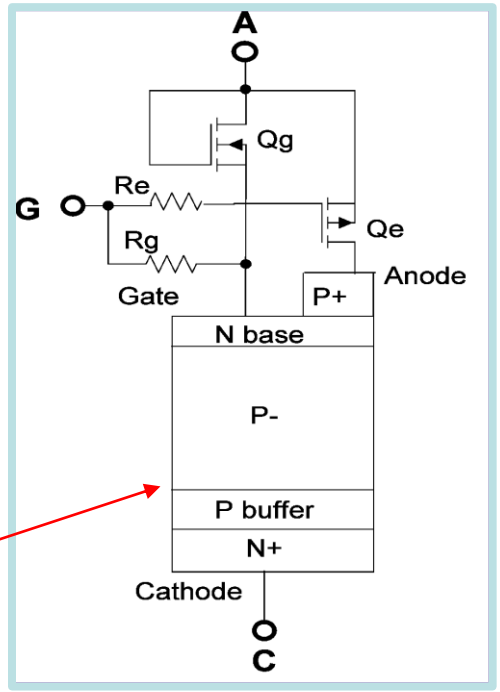


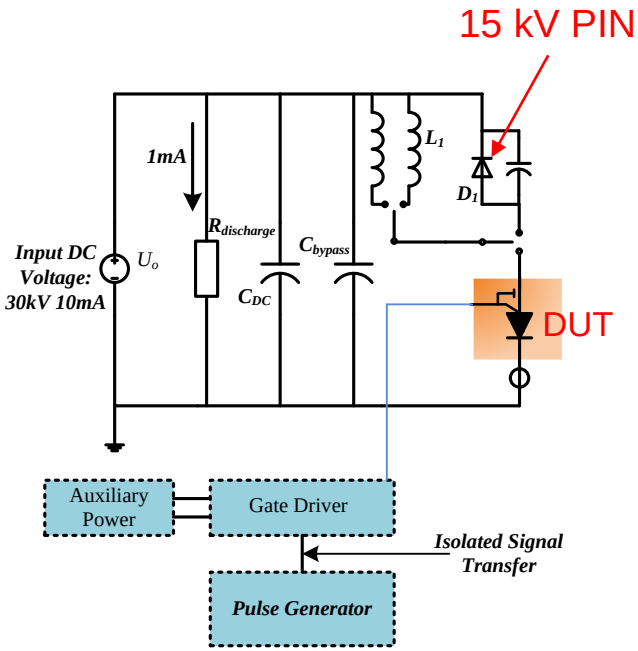
SiC bipolar devices are more suitable for high power and high temperature operation

22 KV P-GTO AND P-ETO



- **Based on 22 kV p-GTO**
- **(three terminal device with voltage controlled turn-off and current controlled turn-on (Ig still required)**

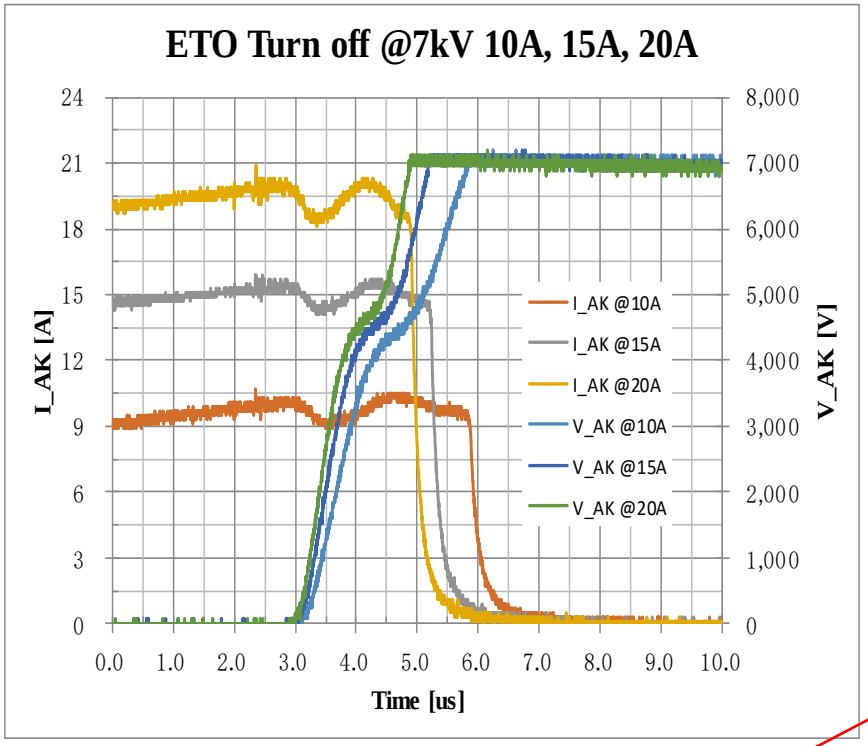


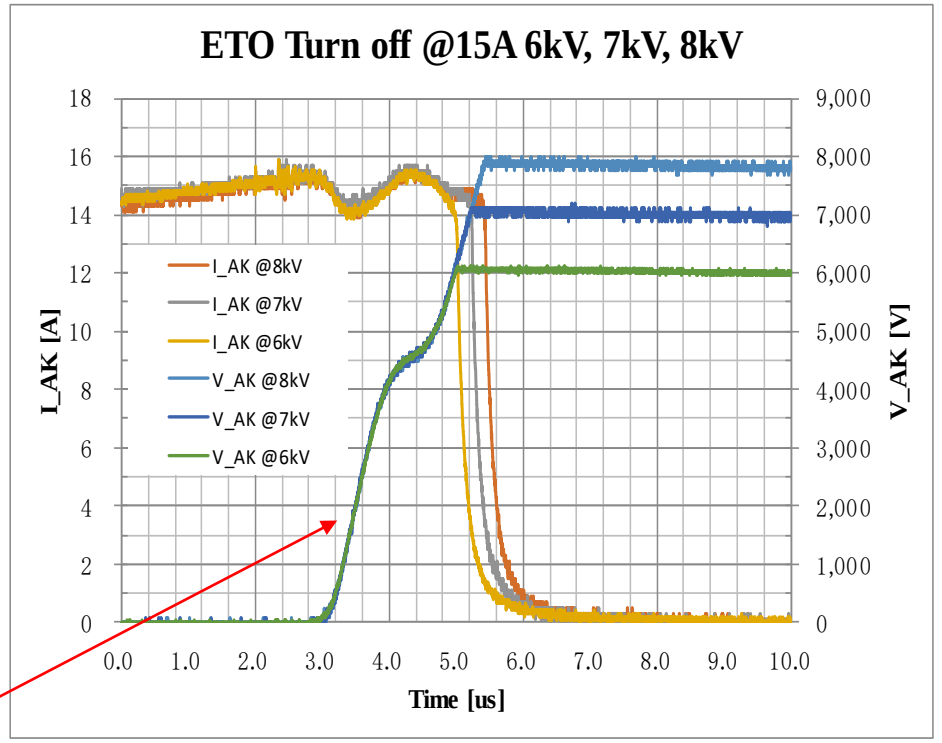


Ultra High Voltage Dynamic Tester

HV Snubberless Turn-off (p-ETO)

Excellent and Robust Turn-off Demonstrated





Slow first phase voltage rise
(Reason: NPN gain > PNP Gain)

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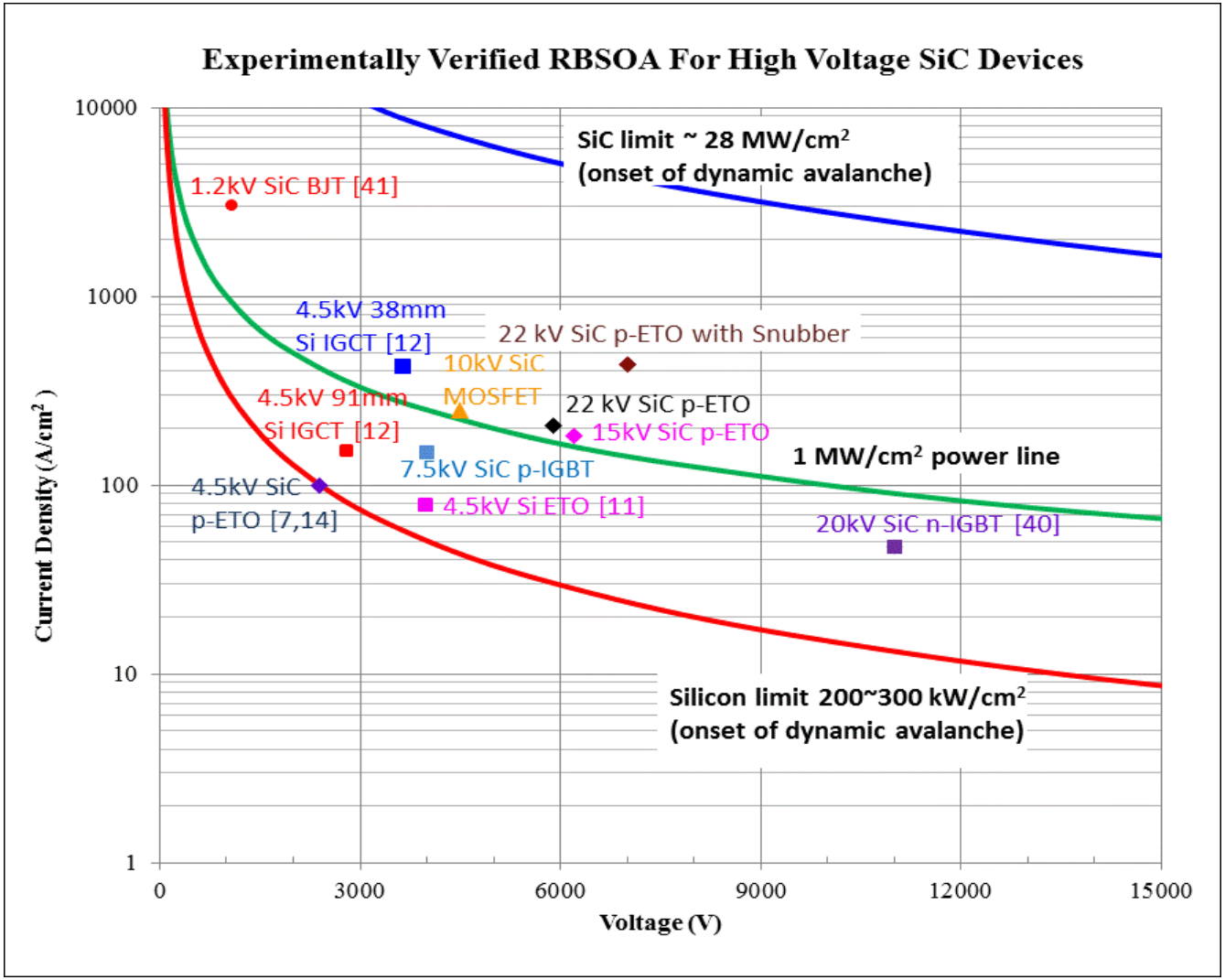
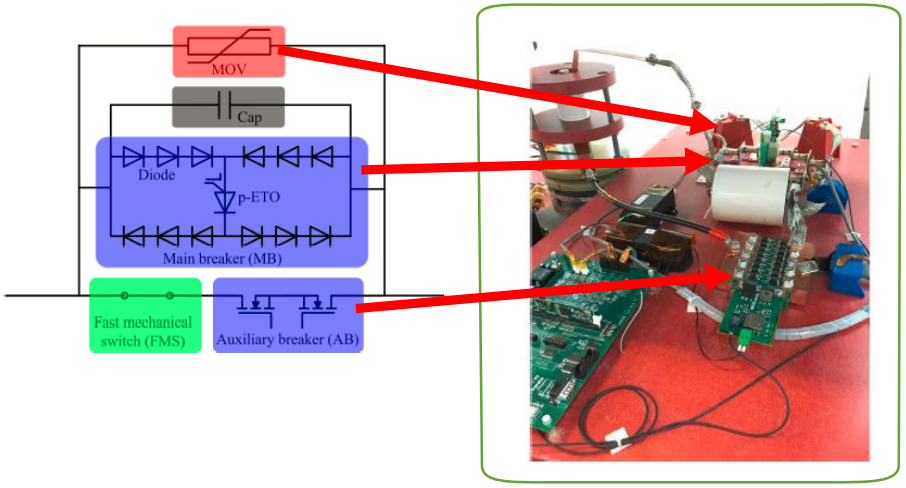
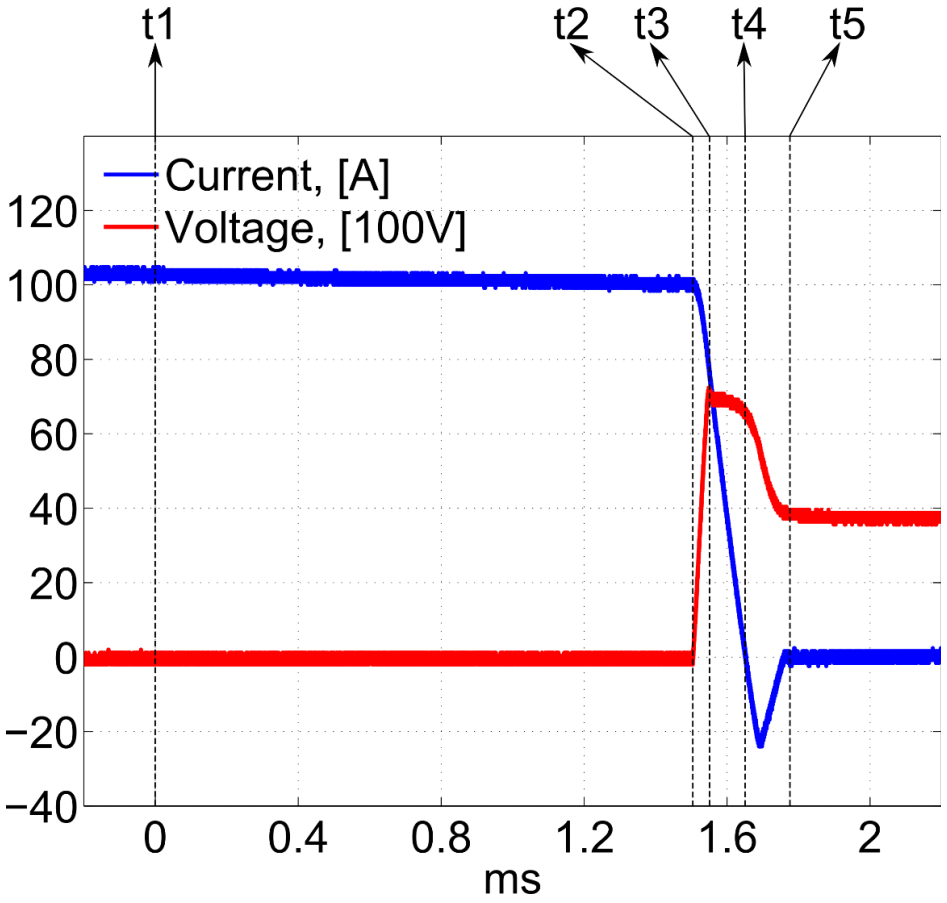
Opportunity: Circuit Breaker

1000A/cm² turn-off capability (>20X time improvement over silicon) is possible



Solid state or hybrid circuit breaker





<2 ms interruption time

- **t1 – t2: mechanical switch delay: 1.5 ms;**
- **t2 – t3: cap limited dv/dt (100A/0.5 uF~200V/us) rise b/c, ~40 us;**
- **t3 – t4: MOV clamped at 7 kV, drives current to zero, ~105 us:**
- **t4 – t5: diode reverse recovery and oscillation, ~100 us.**

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Conclusions

- **SiC/GaN both are promising for high power density/high frequency applications.**
  - GaN: low power application (<10 kW) at 600V or below utilizing unique packaging and small capacitance
  - SiC (600V to 1700V) with improved packaging, driving and soft switching, and high temperature (>200^{o}C) will push the high dentistry boundary to higher power applications (10-100 KW)
- **SiC MOSFET can scale to ultra high voltage (>10 kV)**
  - Solid state transformer (SST) for grid edge, transform the century old grid into an active controlled power electronics grid
  - Other MV grid applications such as MVDC, MV charger, MV solar and storage etc. are emerging
- **SiC bipolar devices (IGBT and GTO/ETO) can scale to ultra high voltage (>10 kV) and high temperature (>200^{o}C) impacting**
  - Solid state circuit breaker
  - HV pulse power application
  - MV Motor Drive
  - MMC HVDC