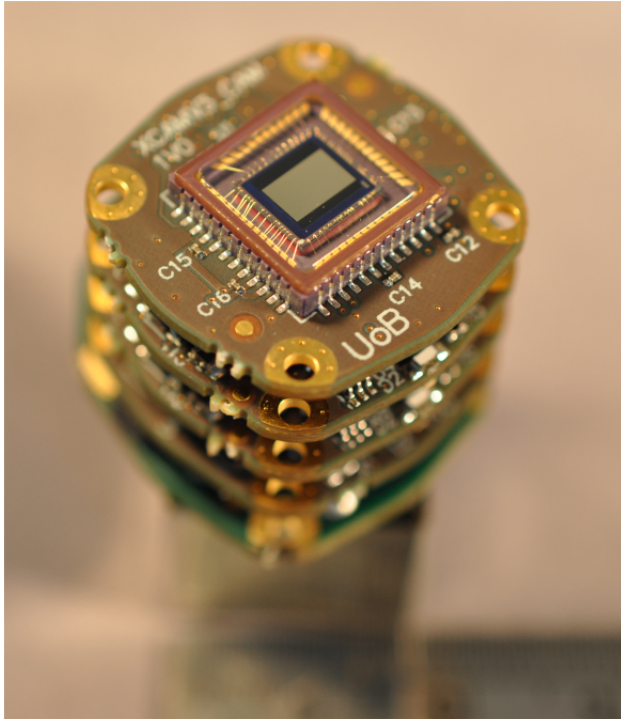


# AVSS

## Adaptive Visual Sampling System

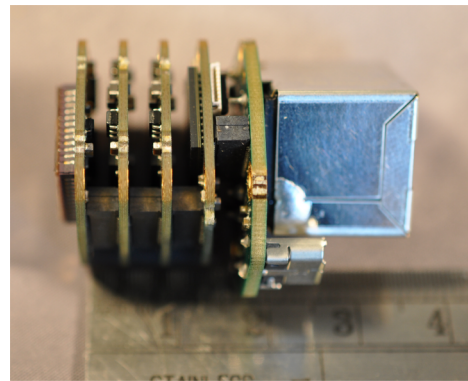
Designed at the University of Bristol within the Visual Information Laboratory, a state-of-the-art low latency adaptive visual sampling system; **a high frame rate computational camera.**



The latest version now supports the E2V sensors with up to 1600x1200 pixels. The sensor board includes 9 degree of freedom motion sensing; gyroscope, accelerometer and magnetic compass. Each processor board includes a dual core, 8 thread XMOS processors delivering 1000 MIPS. A binocular configuration is possible and includes GPIO for fast motor control and interfacing with other external devices. Additional modules can be designed and integrated with ease and at low cost.

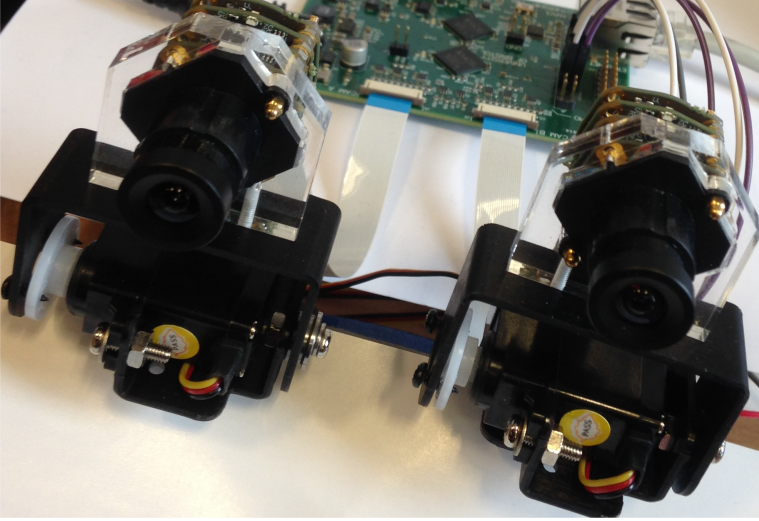
A two processor configuration with ethernet weighs less than 25grams and includes temperature sensing.

The low size, weight and power (SWAP) modular design consists of interchangeable monochrome or colour sensors directly connected to the concurrent XMOS microprocessor architecture. Additional processors can be added to the stack as required. A wide range of output boards is possible, e.g. ethernet, USB, wireless, etc.



1000fps region-of-interest,  
close-to-sensor processing  
with low latency sensor  
programming

The concurrent architecture enables parallel pixel read-in, pixel processing, data transmission and sensor programming within a single core. Pixels can be processed as they are read in; redundant pixels can be discarded at source. Spatio-temporal regions of interest are processed in a bidirectional pipelined architecture. Spatio-temporal regions that contain notable changes are further processed to determine what those changes might be. Variable resolutions can be used to track objects and stabilise vision algorithms.



A two camera coupling motherboard allows a binocular pair to be configured. Two camera stacks with their own motion sensors and processing pipelines are coupled by the motherboard. Depth from vergence is implemented as a demonstrator; the motherboard has GPIO for pan/tilt motor control to be coupled with high ROI framerate visual tracking of the cameras.

The system is designed as a pipeline architecture which can interface with external devices. The pipeline can be programmatically reconfigured to accommodate different modes of visual processing; the system can adapt to visual change.

The fundamental concept behind the technology is that most pixels contain little or no useful information; pixel processing at readout allows these redundant pixels to be discarded close-to-sensor, reducing the expense of transmission bandwidth and memory.

The architecture is extendible and designed to enable complex application specific image processing. The ability to reconfigure the pipeline to a specific task offers multiple application potential from a single design.

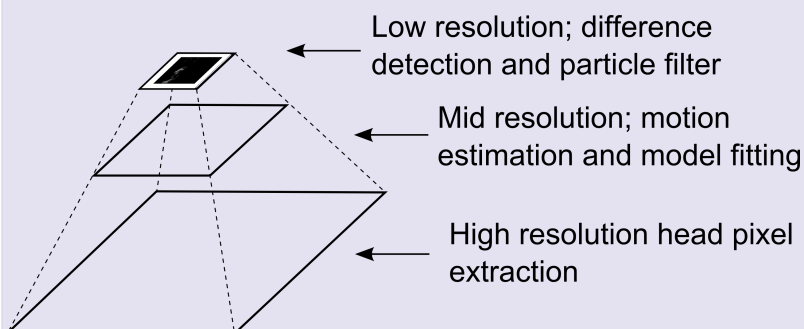
designed to offer a cost effective, high frame rate computational camera

A key advantage of this innovation is a highly programmable, adaptive interface between image capture and high-level processing. As such size, weight and power constraints on image capture and low-level object tracking have been greatly reduced, as well as cost. The system is particularly well suited to real-time filtering and extraction of specific target areas of visual interest; many such areas can be transmitted at much lower data rates than whole images.

## Applications:

### A compact surveillance camera with embedded intelligence

Unlike a standard camera trap, detection and tracking is processed close-to-sensor to determine the presence of a valid/interesting target.



Variable space-time resolution sampling and processing

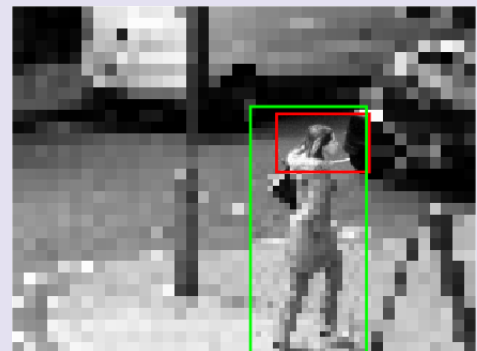
### Other application areas:

UAV control and navigation

Robotic vision

Machine and industrial vision

Only head pixels are transmitted to the operator



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