Power-Efficient DPD Linearization

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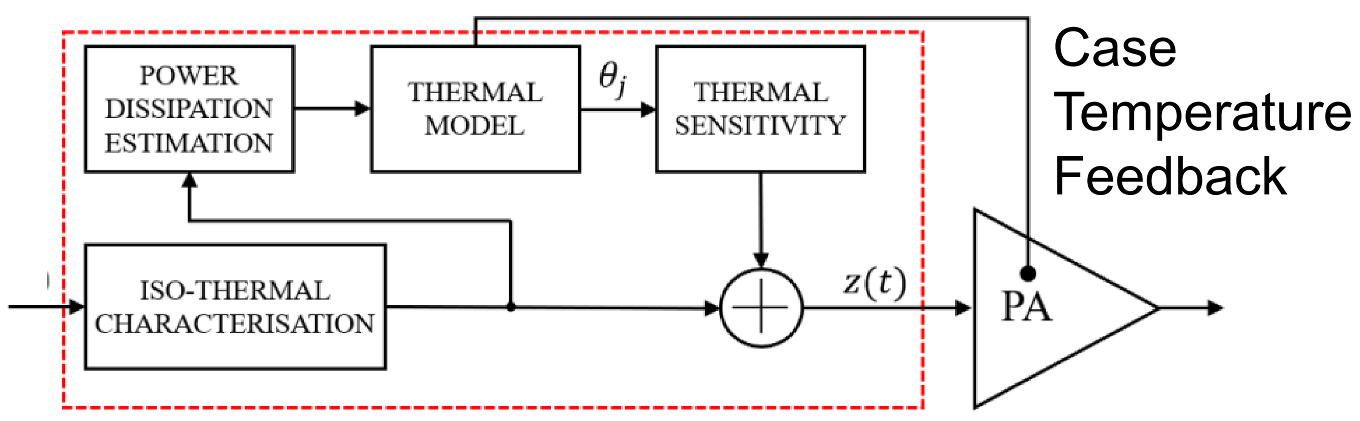
Aim: Provide simple, low power, and effective solutions for the linearization of RF transmitters and power amplifiers.

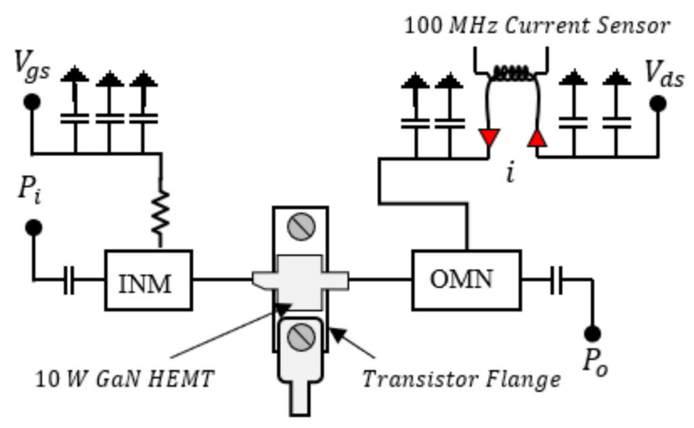
Low-Complexity DPD with Temperature Feedback

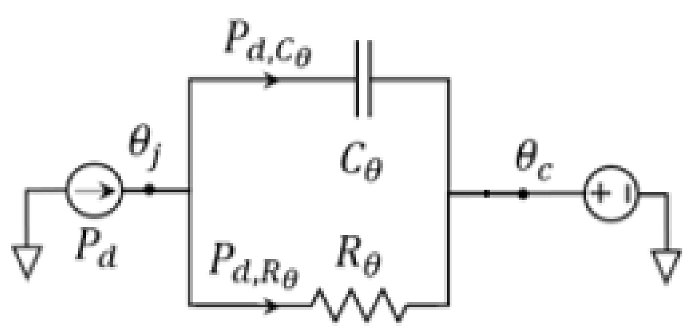
DPD and Hardware Architecture

- The DPD is based on a conventional memory-less polynomial correction with the thermal memory removed successively.



- PA with current sensing and thermal network:





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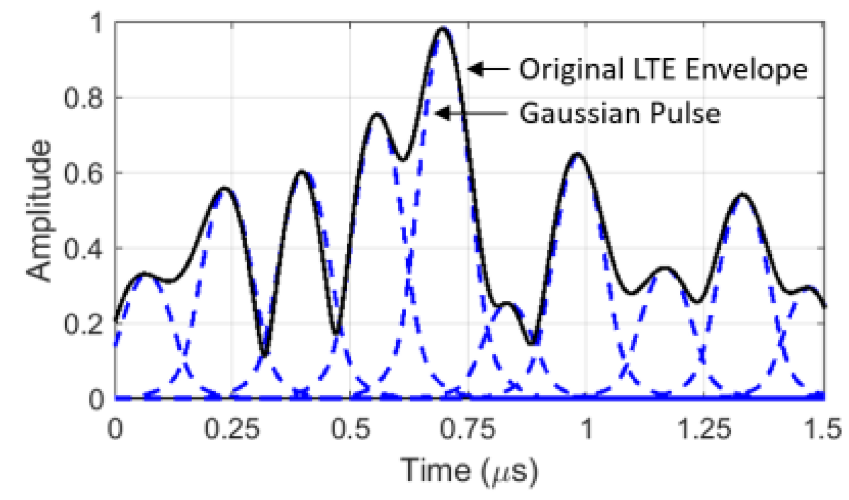
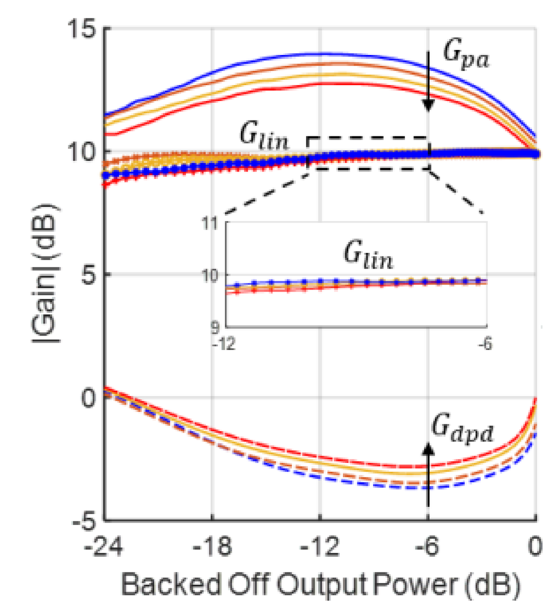
PA Pre-Characterization & Methodology

- A high-PAPR signal is decomposed in a train of amplitude-modulated time-shifted Gaussian pulses.



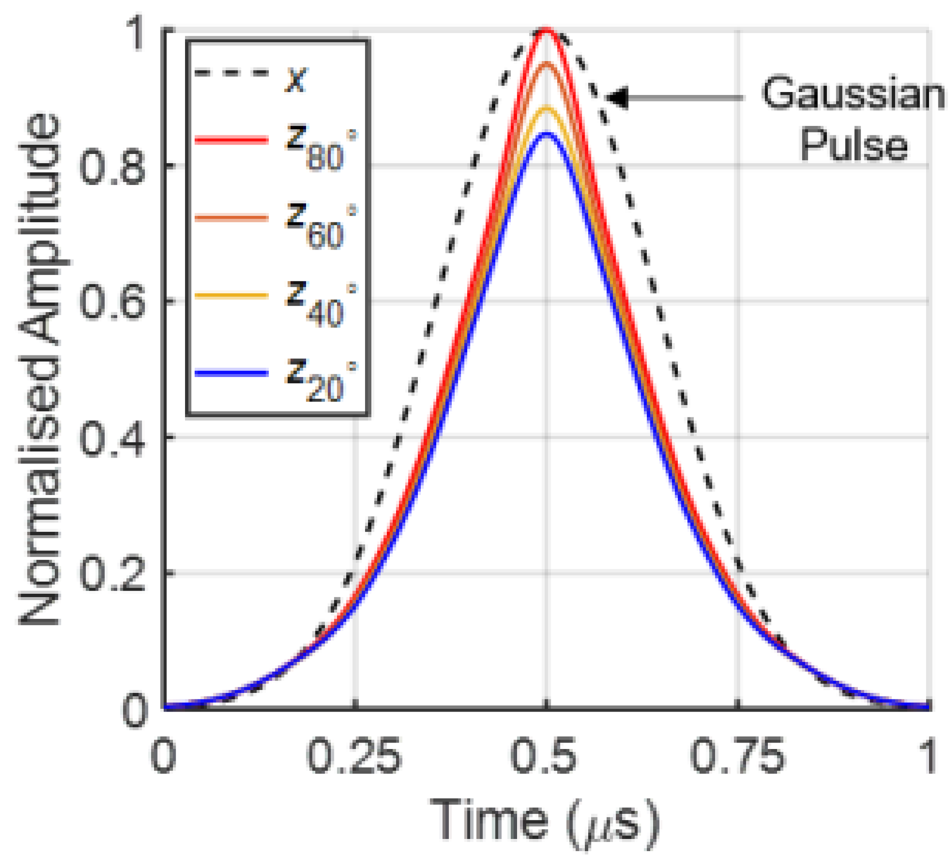
$$T_P \cong \frac{1}{BW_{-3dB}}$$

- These Gaussian pulses are then used to characterise the DPD at different temperatures.

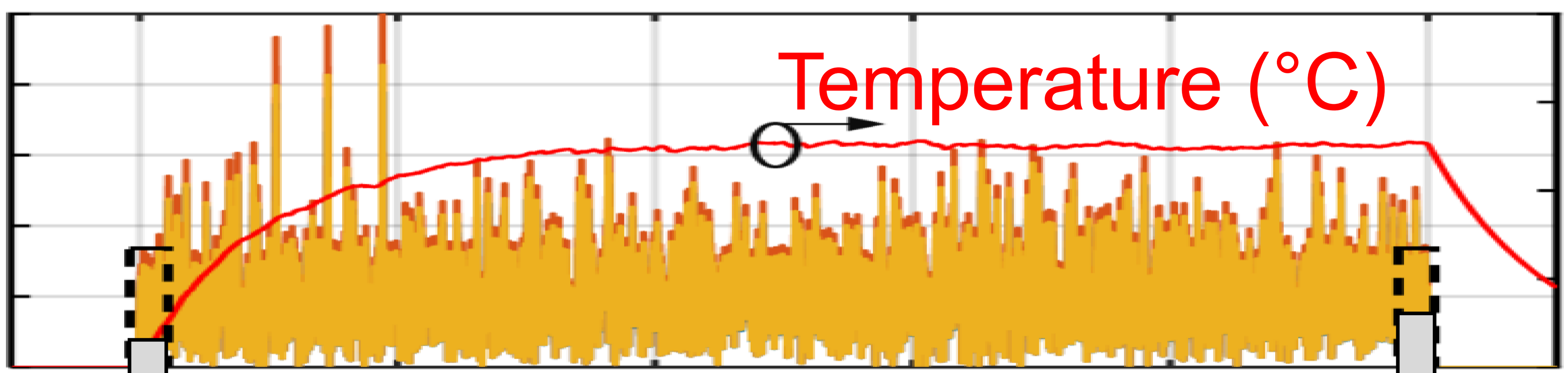


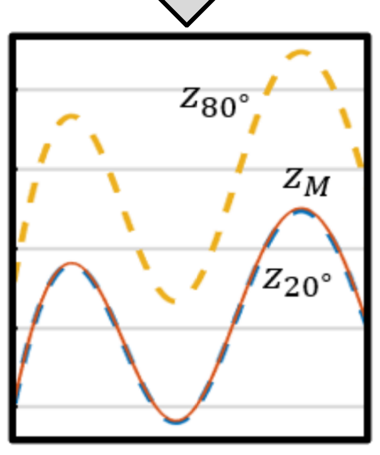
DPD Operation in the Time Domain

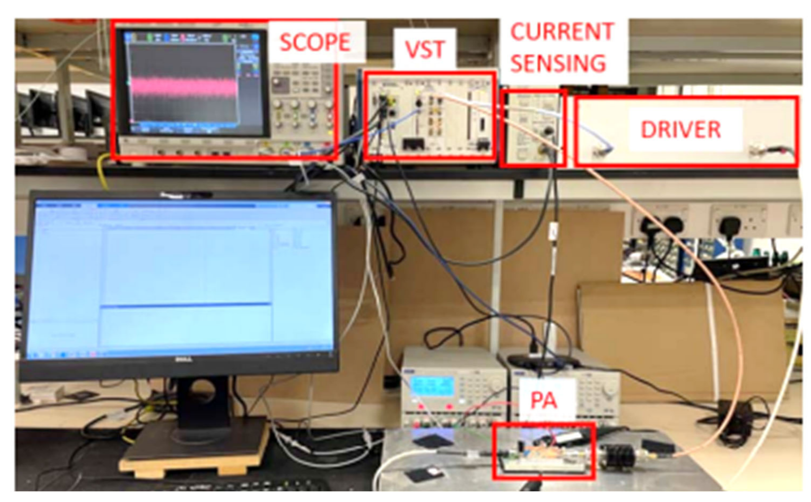
The DPD architecture dynamically adapts the PA input to maintain a fixed linear gain G_{lin}.

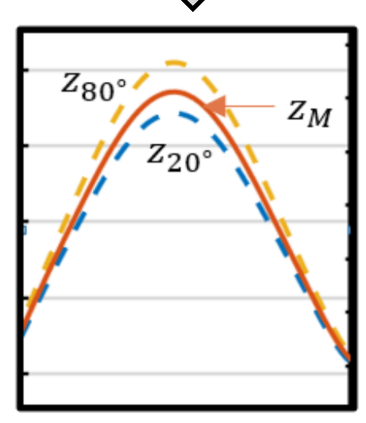


Transistor temperature $\theta_j(t)$ scales the input signal.





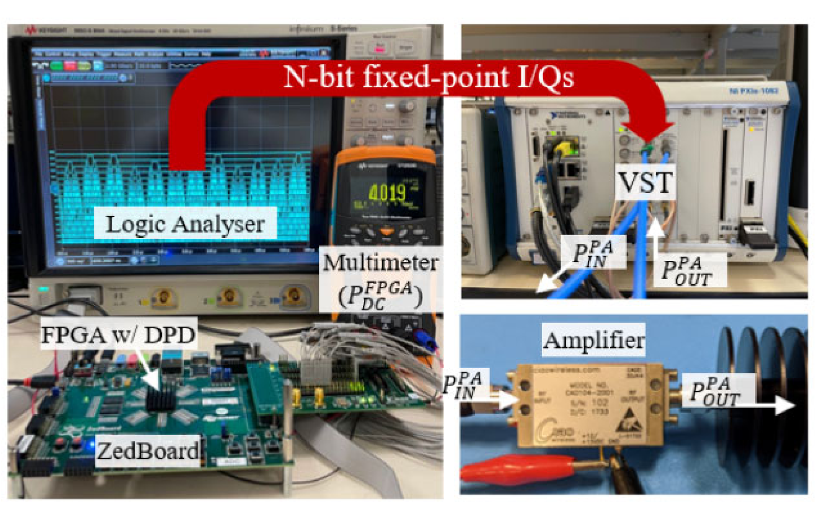




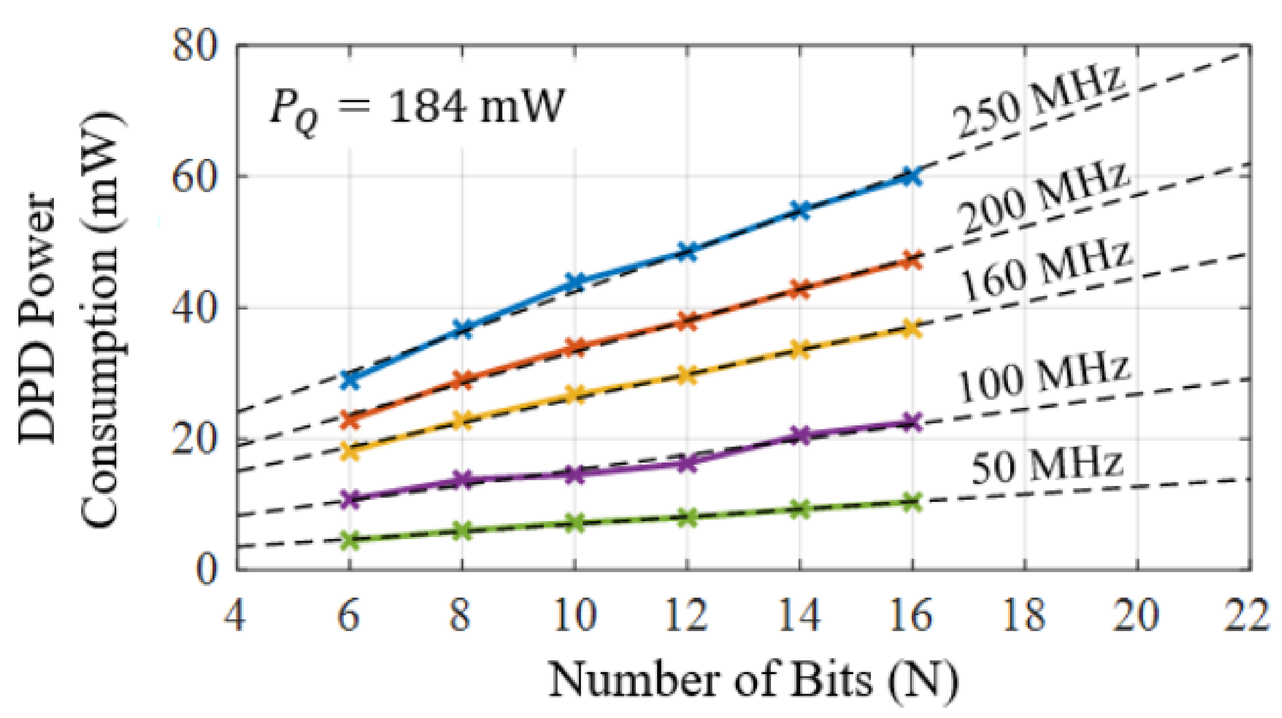
$$G_{dpd}(|x|,\theta_j) \cong G_{dpd}(|x|,\theta_j^*) + g_{dpd}(|x|)(\theta_j - \theta_j^*)$$

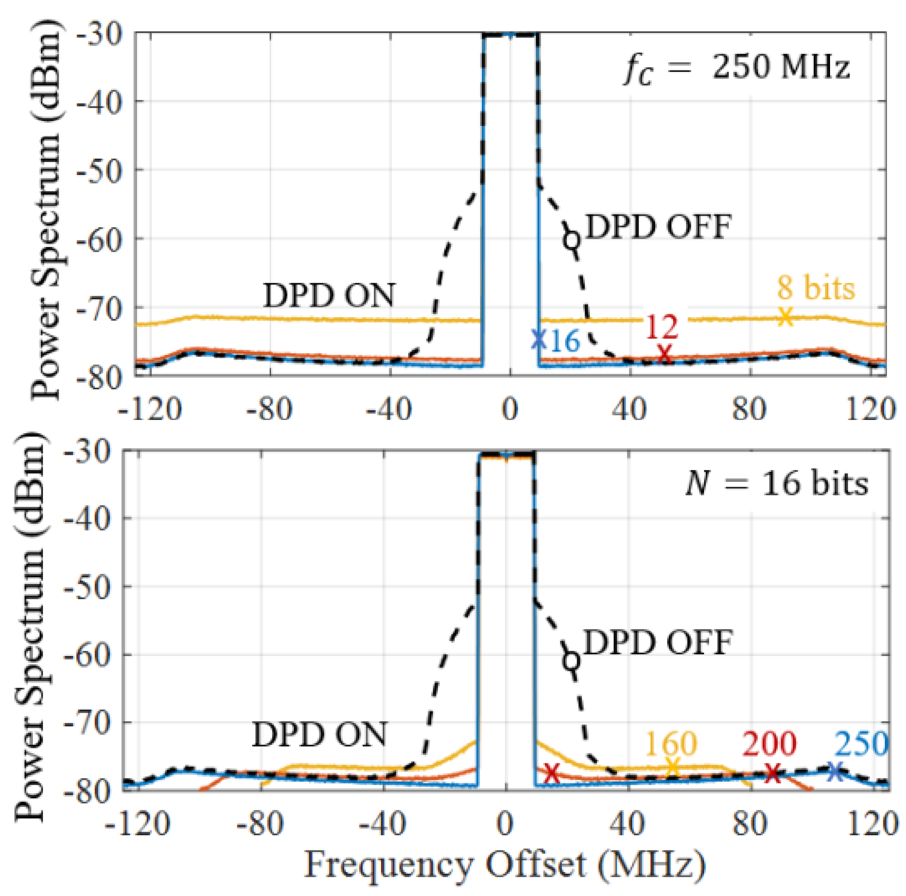
DPD Power Consumption

- DPD mapping on FPGA
- PA + DPD linearity charact.



- DPD power characterization vs. number of bits and clock frequency





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