SECURE WIRELESS AGILE NETWORKS

Multi-bit Digital Power Amplifier

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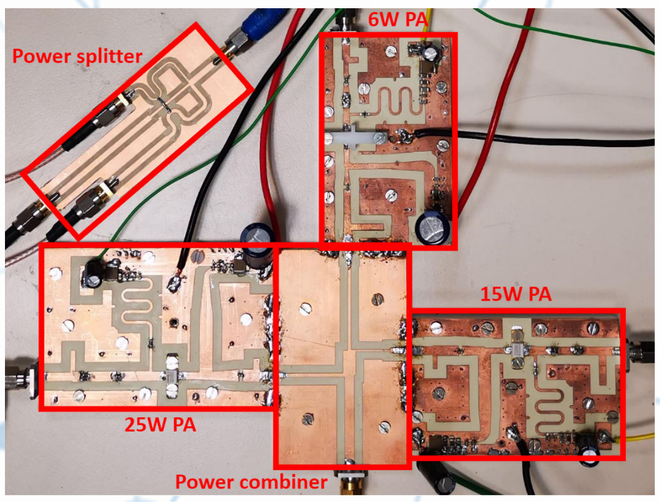
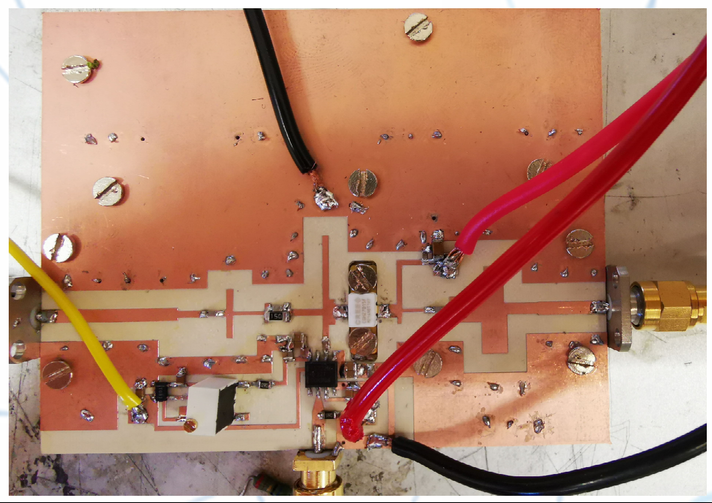
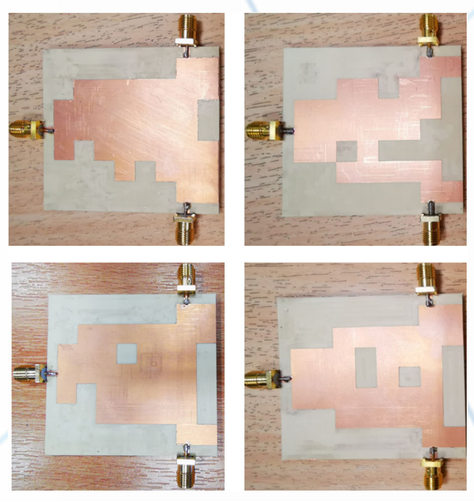
Aim: Design a highly efficient and linear multi-bit digital power amplifier (DPA) for the emerging communication system. Its agile characteristic is promising to be used for the SWAN transmitters.

Introduction

- A systematic three-bit DPA architecture has been proposed by combining three different transistors;
- Each switching-mode PA works only at peak efficiency region or completely off;
- The input OFDM signal is quantised as the modulated signal and control the ON-OFF states of each PA;
- The output network leverages the load modulation to improve the system efficiency;
- Machine learning techniques are investigated to the design of the output power combiner.

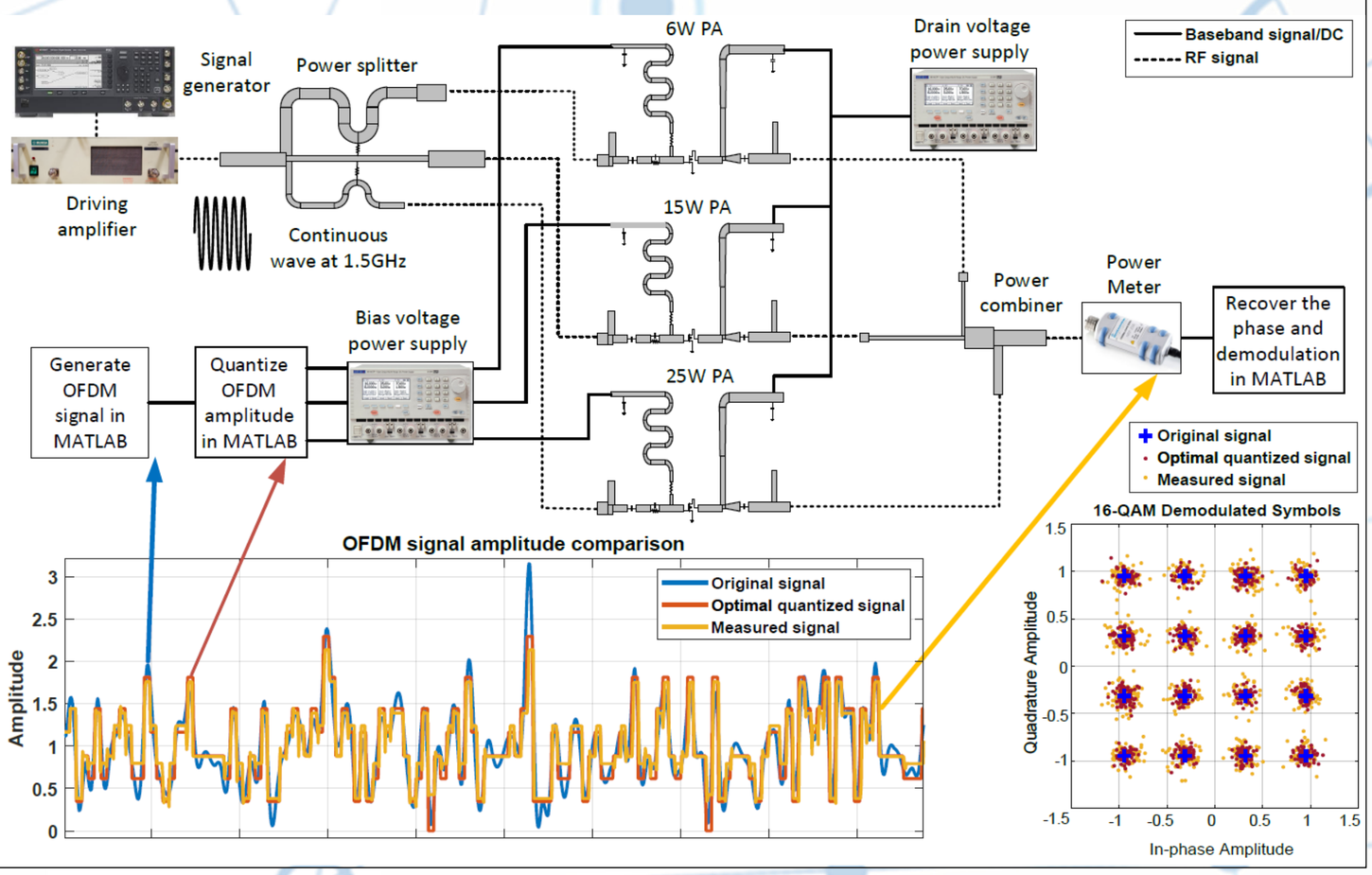






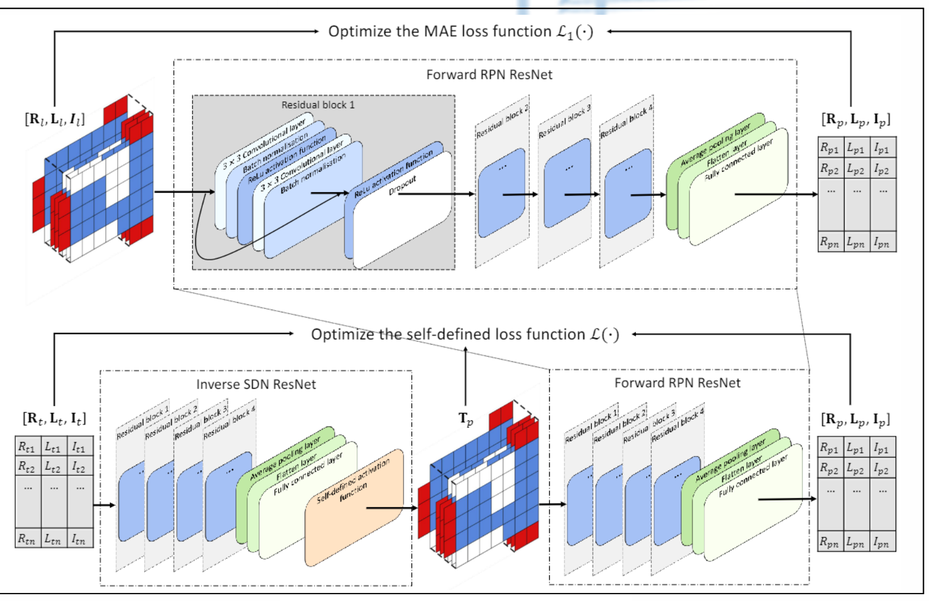
Three-bit DPA performance

- We proposed approaches to minimise the EVM taking consideration of the OFDM signal distribution;
- Multiple output combining networks were investigated and we designed and fabricated the whole DPA architectures;
- A systematic OFDM testbed was used to measure the performance of the three-bit DPA. The result shows our proposed DPA works efficient without losing linearity;
- A high-speed switching PA was fabricated to be implemented in DPA system.



Machine learning approach to design the combining network:

The output power combiner is one of the most important components for multi-bit DPA performance. we proposed a new machine learning approach to design the proper power combiner structures.



Conclusion:

- We derive the optimal output power levels for OFDM signal linearity in multi-bit DPA;
- A three-bit DPA prototype was fabricated. The OFDM testbed is implemented to test the performance;
- A learning-based approach to design the power combiner was proposed and validated through the fabrication.

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